

Comlinear suggests the use of evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. The 730043 and 730046 evaluation boards are designed to aid in the characterization of the CLC431 dual op amp with disable.

- 730043 - DIP packages
Uses all through-hole components
- 730046 - SOIC packages
Uses all surface mount components

Both boards have identical circuit configurations and are designed for non-inverting gains. Inverting gains or other circuit configurations can be obtained with slight modifications to the boards.

Basic Operation

Figures 1 and 2 show the schematics used for both boards. The input signal is brought into the board through SMA connectors to the non-inverting inputs of the CLC431. The resistors R_{in1} and R_{in2} are used to set the input termination resistance to the op amp. The non-inverting gain is set by the following equation:

$$\text{Non-inverting Gain: } 1 + \frac{R_f}{R_g}$$

The value of the feedback resistor, R_f , has a strong influence on AC performance. (Feedback resistor selection is addressed in the following section.) The output of the op amp travels through a series resistance, R_{out} , and then leaves the board through an SMA connector. The series resistance, R_{out} , is provided to obtain adequate back matching of a load or isolate the output from capacitive loads.

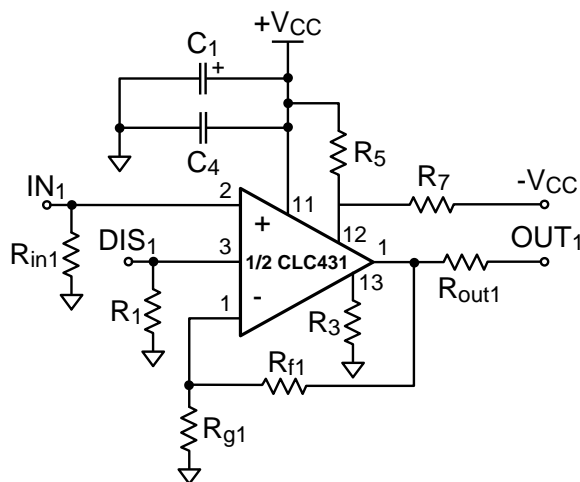


Figure 1: Channel 1 Configuration

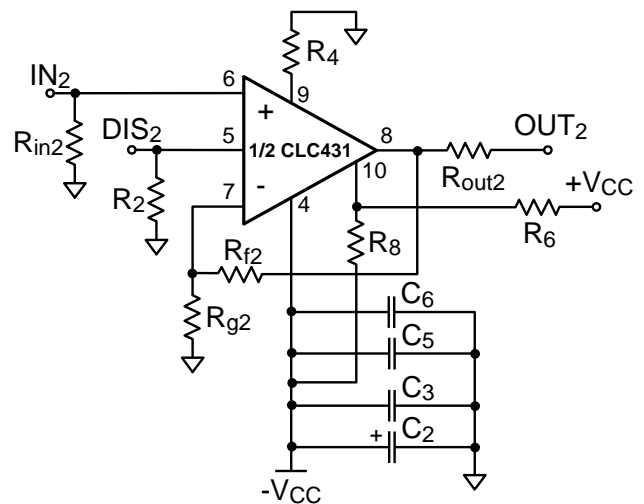


Figure 2: Channel 2 Configuration

When evaluating just one of the CLC431's channels, the unused channel can cause adverse effects if not properly biased. Complete the following, on the unused channel:

- Install R_f and R_g
- Ground the input through R_{in}
- Load the output through R_{out}

Feedback Resistor Selection

Optimum performance of the CLC431, at a gain of +2V/V, is achieved with R_f equal to 866Ω. The frequency response plots in the typical performance section of the CLC431/CLC432 data sheet illustrate the recommended R_f for several gains. Within limits, R_f can be adjusted to optimize the frequency response. Increase R_f to roll-off frequency response and compress bandwidth. As a rule of thumb, if the recommended R_f is doubled, then the bandwidth will be cut in half.

Disable Features

A detailed discussion of various disabling logic families can be found in the CLC431/CLC432 data sheet. The evaluation boards are designed to accommodate all schemes mentioned in the data sheet.

There are 3 pins associated with the disable function for each of the CLC431's op amps:

- DIS - pins 3 and 5
- $\overline{\text{DIS}}$ - pins 12 and 10
- V_{ttl} - pins 13 and 9

The CLC431 is guaranteed to be enabled if all of these pins are left "open", unconnected.

The following is a brief description of R1 through R8 (refer to Figures 1 and 2):

- R1 and R2 are used to set input termination on the disable inputs (DIS).
- R3 and R4 are inserted when it is necessary to ground V_{rttl} .
- R5 and R6 connect each \overline{DIS} pin to $+V_{CC}$.
- R7 and R8 connect each \overline{DIS} pin to $-V_{CC}$, when desired.

The addition of R3 and R4 protect the disable circuit from accidental shorts to the power supply during evaluation. There are 2 diodes between \overline{DIS} and V_{rttl} , therefore setting R3 and R4 to $2k\Omega$ will limit the current and protect the circuit from damage.

Isolation

For maximum isolation between channels, proper power supply decoupling is required. Isolation performance is significantly affected by the location of the bypass capacitors' ground point. If these ground connections are located near the ground connections of R_g and R_{in} , then the channel-to-channel coupling will increase. To avoid this, the CLC431 evaluation boards have been designed with a " $-V_{CC}$ plane" under the part. This allows the negative supply to be bypassed symmetrically near the outputs.

- When maximum isolation is desired, use C3, C5, and C6 leaving C4 open.
- When isolation is not critical, use C3 and C4 leaving C5 and C6 open.

The bypass capacitors, C1 and C2 should always be included. The use of good quality capacitors also helps to achieve better isolation performance.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. When designing your own board, use the evaluation board as a guide and follow these steps as a basis for high frequency layout:

1. Include $6.8\mu F$ tantalum and $0.1\mu F$ ceramic capacitors on both supplies.
2. Place the $6.8\mu F$ capacitors within 0.75 inches of the power pins.
3. Place the $0.1\mu F$ capacitors less than 0.1 inches from the power pins.
4. Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.

5. Minimize all trace lengths to reduce series inductances.
6. Do not use sockets. If absolutely necessary, use individual flush-mount sockets.

Measurement Hints

If 50Ω coax and $50\Omega R_{in}/R_{out}$ resistors are used, many of the typical performance plots found in the CLC431/CLC432 data sheets can be reproduced.

When SMA connectors and cables are not available to evaluate the CLC431, do not use normal oscilloscope probes. Use low impedance resistive divider probes of 100 to 500Ω . If a low impedance probe is not available, then a section of 50Ω coaxial cable and a low impedance resistor may be used. Follow these 3 steps to create a "cable/resistor" probe:

1. Connect one end of the coax's center to a test measurement box terminated in 50Ω .
2. Connect the other end of the cable's center conductor to the low impedance resistor. (The open side of the resistor is now a probe.)
3. Connect the ground shield of the cable to evaluation board ground and test box ground.

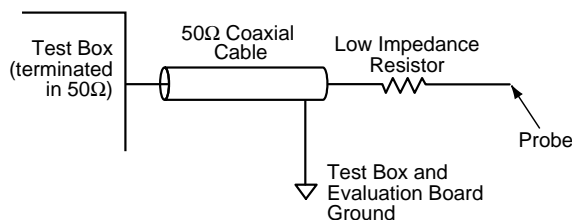


Figure 3: "Cable/Resistor" Probe Configuration

This "cable/resistor" probe shown in Figure 3, forms a voltage attenuator between the resistor and the 50Ω termination resistance of the test box. This method allows measurements to be performed directly on the output pin of the amplifier.

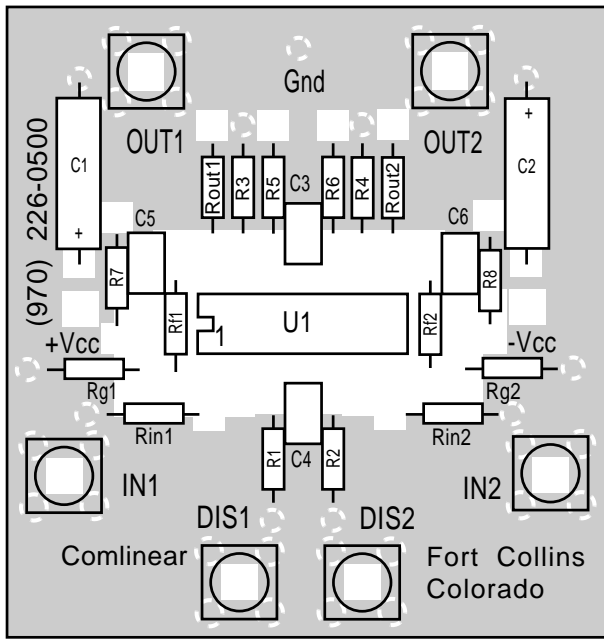
Power Supplies

The recommended power supply for the CLC431 is $\pm 15V$. However, the voltages can be taken down to $\pm 5V$ with slightly degraded performance.

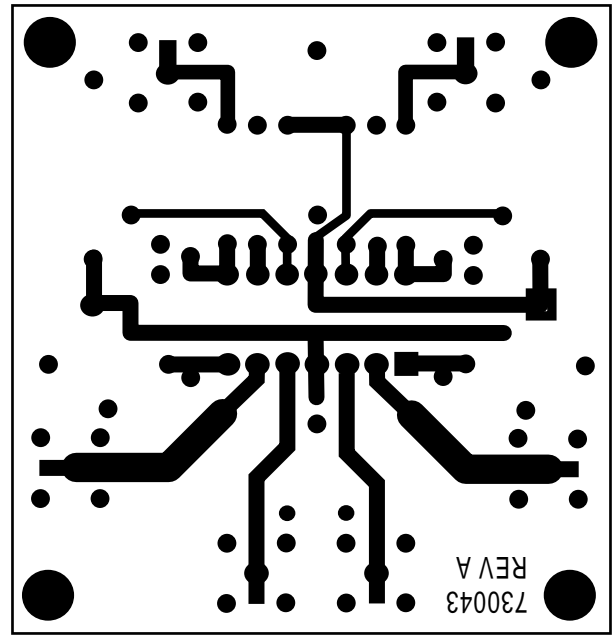
Component Values

- Use the CLC431/CLC432 data sheet and the evaluation board sheet to select resistor values.
- C1, C2 - $6.8\mu F$ tantalum capacitors
- C3, C4, C5, C6 - $0.1\mu F$ ceramic capacitors

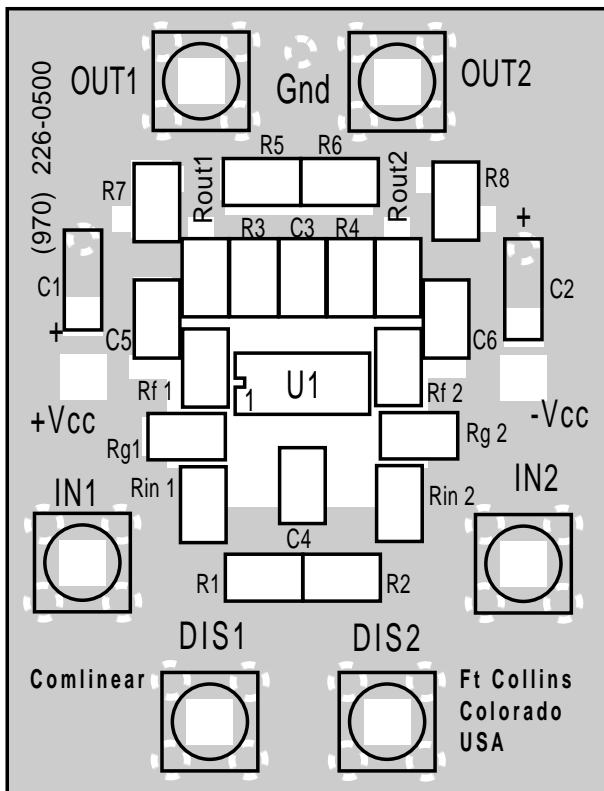
730043 – DIP – Top Side



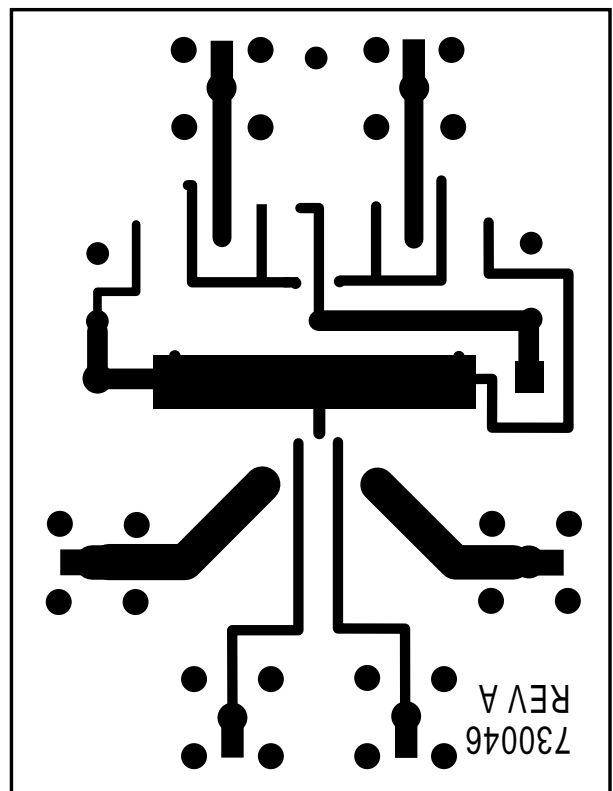
730043 – DIP – Bottom Side



730046 – SOIC – Top Side



730046 – SOIC – Bottom Side



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