National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM194-X REV 0A0

Original Creation Date: 09/13/95
Last Update Date: 03/08/01
Last Major Revision Date: 01/30/01

SUPERMATCH PAIR

General Description

The LM194 is a junction isolated ultra well-matched monolithic NPN transistor pair with an order of magnitude improvement in matching over conventional transistor pair. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1uA to 1mA and 0V up to 35V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current-the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 is available in an isolated header 6-lead T0-5 metal can package.

Industry Part Number

LM194

NS Part Numbers

LM194H/883

Prime Die

LM194

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5004

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Emitter-base voltage matched to 100uV
- Offset voltage drift less than 0.1uV/ C
- Current gain (hFE) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1uA to 1mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

CONTROLLING DOCUMENT:

LM194H/883	5962-8777701XA

(Absolute Maximum Ratings)
(Note 1)

Collector Current	20mA
Collector-Emitter Voltage	VMAX 35V
Collector-Base Voltage	35V
Collector-Substrate Voltage	35V
Collector-Collector Voltage	35V
Base-Emitter Current	$\pm$10mA
Power Dissipation (Note 2)	500mW
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C to +150 C
Soldering Information Metal Can Package (10 sec.)	260 C
Operating Temperture Range	-55 C $\leq$ Ta $\leq$ 125 C
Thermal Resistance ThetaJA (Still Air) (500LF/Min Air Flow)	 TBD TBD
ThetaJC	TBD
Package Weight (Typical) 6 Ld Metal Can	 TBD
ESD Tolerance (Note 3)	3000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5K ohms in series with 100pF

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
hFE	Current Gain	VCB = 0V, IC = 1mA			0.35		K	1
		VCB = 35V, IC = 1mA			0.35		K	1
					0.25		K	2, 3
		VCB = 0V, IC = 100uA			0.35		K	1
		VCB = 35V, IC = 100uA			0.35		K	1
		VCB = 0V, IC = 10uA			0.30		K	1
		VCB = 35V, IC = 10uA			0.30		K	1
		VCB = 0V, IC = 1uA			0.20		K	1
		VCB = 35V, IC = 1uA			0.20		K	1
hFE MATCH	Gain Match	VCB = 0V, IC = 1mA			-2	2	%	1
		VCB = 35V, IC = 1mA			-2	2	%	1
					-6	6	%	2, 3
		VCB = 0V, IC = 100uA			-2	2	%	1
		VCB = 35V, IC = 100uA			-2	2	%	1
		VCB = 0V, IC = 10uA			-2	2	%	1
		VCB = 35V, IC = 10uA			-2	2	%	1
VBEO	Emitter - Base Offset Voltage	VCB = 0V, IC = 1mA			-100	100	uV	1
		VCB = 35V, IC = 1mA			-100	100	uV	1
					-230	230	uV	2, 3
		VCB = 0V, IC = 0.3mA			-100	100	uV	1
		VCB = 0V, IC = 100uA			-100	100	uV	1
		VCB = 35V, IC = 100uA			-100	100	uV	1
					-350	350	uV	2, 3
		VCB = 0V, IC = 10uA			-100	100	uV	1
		VCB = 35V, IC = 10uA			-100	100	uV	1
		VCB = 0V, IC = 1uA			-100	100	uV	1
		VCB = 35V, IC = 1uA			-100	100	uV	1

Electrical Characteristics

DC PARAMETERS(Continued)

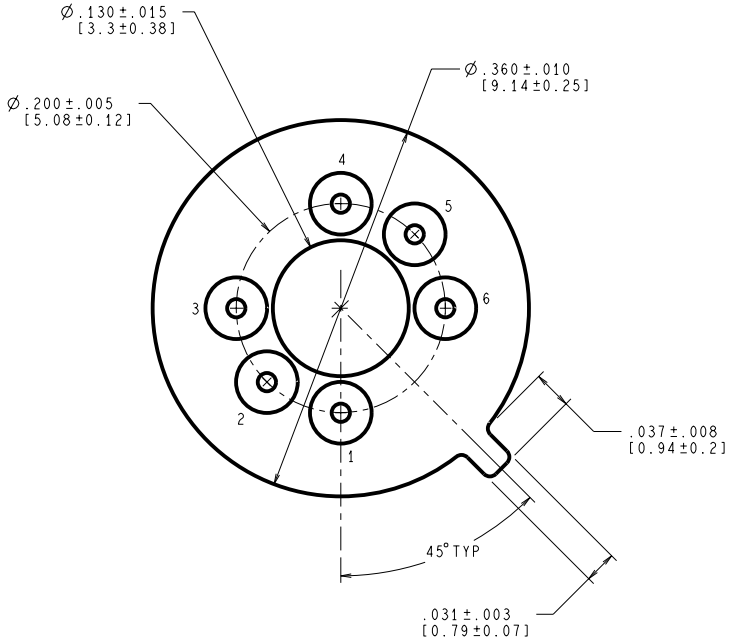
SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Delta VBEO	Change in Emitter - Base Offset	VCB = 0V to 35V, IC = 1mA			-25	25	uV	1
		VCB = 0V to 35V, IC = 100uA			-25	25	uV	1
		VCB = 0V to 35V, IC = 10uA			-25	25	uV	1
		VCB = 0V to 35V, IC = 1uA			-25	25	uV	1
		VCB = 0V, IC= 1uA to 300uA			-25	25	uV	1
ICCX	Collector-Collector Leakage	VCB = 35V, COLL1 to COLL2			-2	2	nA	1
		VCB = 35V, COLL2 to COLL1			-2	2	nA	1
ICBX	Collector- Base Leakage	VCB = 35V, COLL1 to Base1			-0.25	0.25	nA	1
		VCB = 35V, COLL2 to Base2			-0.25	0.25	nA	1

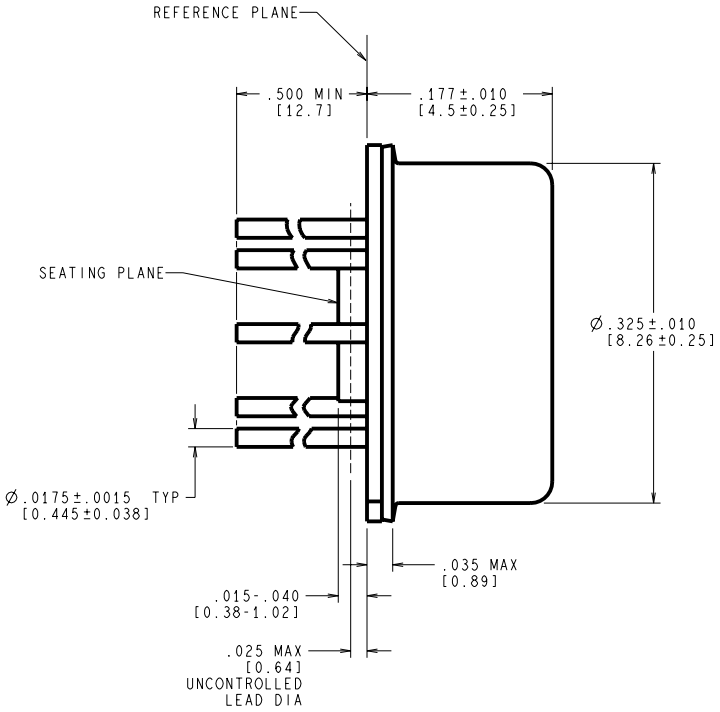
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
09724HRD3	METAL CAN (H), TO-99, 8LD, .200 DIA P.C.(B/I CKT)
H06CRE	METAL CAN (H), TO-99, 6LD, .200DIA P.C. (P/P DWG)
P000477A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PIN OUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11001	06/19/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/19/95
DFTG. CHK.	
ENGR. CHK.	

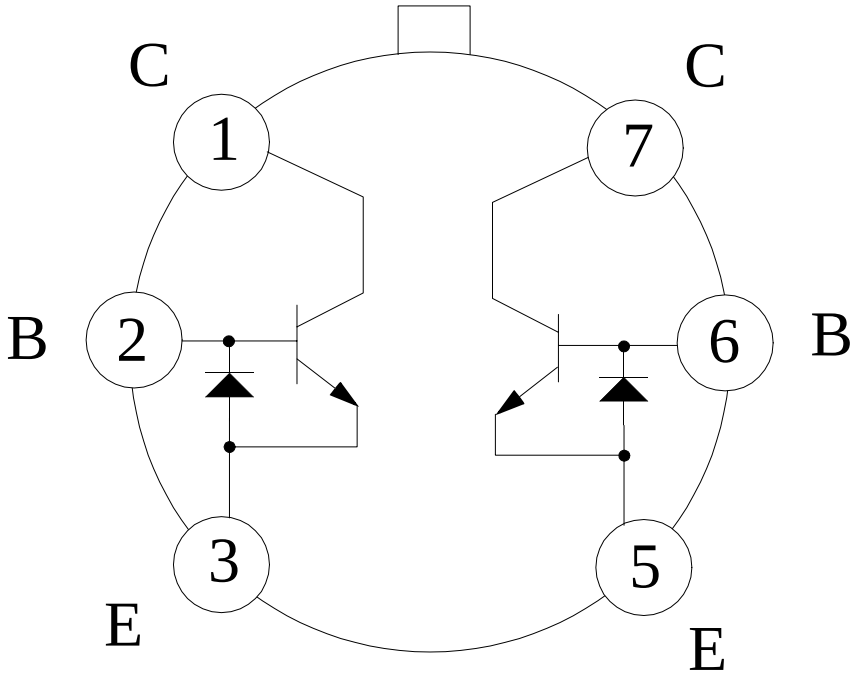
PROJECTION — INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 6 LEAD, .200 DIA P.C.

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H06C	E

DO NOT SCALE DRAWING — SHEET 1 of 1



LM194H
6 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000477A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0BL	M0001690	03/08/01	Barbara Lopez	Changed: MNLM194-X Rev. 0AL to MNLM194-X Rev. 0BL.
0A0	M0003781	03/08/01	Rose Malone	Update MDS: MNLM194-X, Rev. 0BL to Fully Released MDS MNLM194-X, Rev. 0A0.