

**MNLM1575-ADJ-X REV 2C1**

 Original Creation Date: 09/08/95  
 Last Update Date: 05/22/00  
 Last Major Revision Date: 09/08/95

**SIMPLE SWITCHER(TM) 1A STEP-DOWN VOLTAGE REGULATOR**
**General Description**

The LM1575 regulator is a monolithic integrated circuit that provides all the active functions for a step-down (buck) switching regulator, capable of driving 1A load with excellent line and load regulation.

Requiring a minimum number of external components, this regulator is simple to use and includes internal frequency compensation and a fixed-frequency oscillator.

The LM1575 offers a high-efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors optimized for use with the LM1575 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed  $\pm 4\%$  tolerance on output voltage within specified input voltages and output load conditions, and  $\pm 10\%$  on the oscillator frequency. External shutdown is included, featuring 50uA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

**Industry Part Number**

LM1575-ADJ

**NS Part Numbers**

 LM1575J-ADJ-QML  
 LM1575K-ADJ-QML  
 LM1575WGADJ-QML

**Prime Die**

LM1575-ADJ

**Controlling Document**

SEE FEATURES SECTION

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

**Subgrp Description Temp ( °C)**

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- Adjustable version output voltage range, 1.23V to 37V  $\pm 4\%$  max over line and load conditions
- Guaranteed 1A output current
- Requires only 4 external components
- 52KHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

CONTROLLING DOCUMENTS:

LM1575J-ADJ-QML	5962-9167101MEA
LM1575K-ADJ-QML	5962-9167101MXA
LM1575WGADJ-QML	5962-9167101QZA

**Applications**

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converted (Buck-Boost)

**(Absolute Maximum Ratings)**

(Note 1)

Maximum Supply Voltage	45V
$\overline{\text{ON}}$ /OFF Pin Input Voltage	$-0.3\text{V} \leq V \leq +V_{\text{in}}$
Output Voltage to Ground (Steady State)	-1V
Power Dissipation (Note 2, 3)	Internally Limited
Storage Temperature Range	$-65\text{ C} \leq T_a \leq +150\text{ C}$
Lead Temperature (Soldering, 10 seconds)	
METAL CAN	300 C
CERDIP	260 C
CERAMIC SOIC	260 C
Maximum Junction Temperature	150 C
Thermal Resistance	
ThetaJA	
METAL CAN (Still Air)	45 C/W
(500LF/Min Air Flow)	10 C/W
CERDIP (Still Air)	70 C/W
(500LF/Min Air Flow)	33 C/W
CERAMIC SOIC (Still Air)	121 C/W
(500LF/Min Air Flow)	73 C/W
ThetaJC (Note 3)	
METAL CAN	3.3 C/W
CERDIP (Note 3 applicable to this Pkg only)	2.0 C/W
CERAMIC SOIC	3.0 C/W
Package Weight (Typical)	
METAL CAN	TBD
CERDIP	TBD
CERAMIC SOIC	TBD
ESD Tolerance (Note 4)	2000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{j\text{max}}$  (maximum junction temperature),  $\Theta_{\text{JA}}$  (package junction to ambient thermal resistance), and  $T_A$  (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{\text{dmax}} = (T_{j\text{max}} - T_A)/\Theta_{\text{JA}}$  or the number given in the Absolute Maximum Ratings, whichever is lower.

**(Continued)**

- Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
- Note 4: Human body model, 1.5k Ohms in series with 100pF.

**Recommended Operating Conditions**

Temperature Range	-55 C ≤ Ta ≤ +125 C
Supply Voltage	40V

## Electrical Characteristics

### ELECTRICAL CHARACTERISTICS: SYSTEM PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$  and  $I_{load} = 200mA$ .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vfb	Feedback Voltage	$V_{out} = V_{fb}$	1		1.217	1.243	V	1
Vfbt	Feedback Voltage	$0.2A \leq I_{load} \leq 1A$ , $8V \leq V_{in} \leq 40V$ , $V_{out} = V_{fb}$	1		1.205	1.255	V	1
			1		1.193	1.267	V	2, 3

### ELECTRICAL CHARACTERISTICS: DEVICE PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$  and  $I_{load} = 200mA$ .

Ib	Feedback Bias Current	$V_{out} = V_{fb}$				100	nA	1
						500	nA	2, 3
Vsat	Saturation Voltage	$I_{out} = 1A$	2			1.2	V	1
			2			1.4	V	2, 3
Icl	Current Limit	Peak Current, $t_{ON} \leq 3\mu S$	2		1.7	3.0	A	1
			2		1.3	3.2	A	2, 3
Il	Output Leakage Current	$V_{in} = 35V$ , Output = 0V	4			2	mA	1
		$V_{in} = 35V$ , Output = -1V	4			30	mA	1
Iq	Quiescent Current		4			10	mA	1
			4			12	mA	2, 3
Istby	Standby Quiescent Current	$\overline{ON}/OFF$ Pin = 5V (OFF)				200	uA	1
						500	uA	2, 3

### AC ELECTRICAL CHARACTERISTICS: DEVICE PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$  and  $I_{load} = 200mA$ .

fo	Oscillator Frequency				47	58	KHz	4
					43	62	KHz	5, 6
Dc	Max Duty Cycle (ON)		3		93		%	9

## Electrical Characteristics

### ELECTRICAL CHARACTERISTICS: ON/OFF CONTROL

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$  and  $I_{load} = 200mA$ .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 0V$			2.2		V	1
Vih	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 0V$			2.4		V	2, 3
Vil	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 5V$				1.0	V	1
Vil	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 5V$				.8	V	2, 3
Iih	$\overline{ON}/OFF$ Pin Input Current	$\overline{ON}/OFF$ Pin = 5V (OFF)				30	uA	1
Iil	$\overline{ON}/OFF$ Pin Input Current	$\overline{ON}/OFF$ Pin = 0V (ON)				10	uA	1

Note 1: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance.

Note 2: Output pin sourcing current. No diode, inductor or capacitor connected to output.

Note 3: Feedback removed from output and connected to 0V.

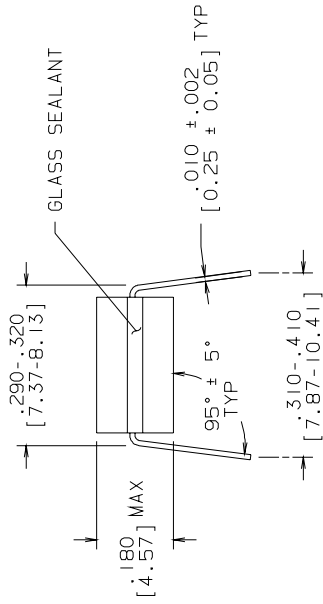
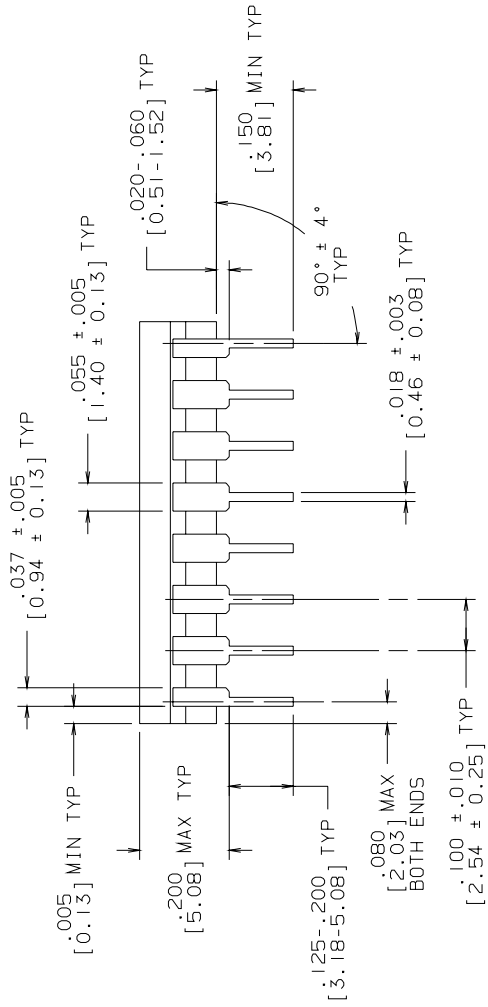
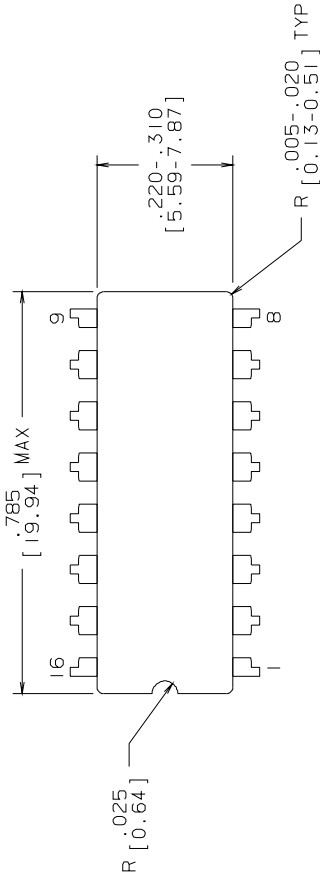
Note 4: Feedback removed from output and connected to 12V to force the output transistor OFF.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06153HRA2	METAL CAN (KA), TO-3, 4LD, LOW PROFILE (B/I CKT)
06265HRB2	CERDIP (J), 16 LEAD (B/I CKT)
06379HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
KA04BRA	METAL CAN (KA), TO-3, 4 LEAD, LOW PROFILE (P/P DWG)
P000232A	METAL CAN (KA), TO-3, 4LD, LOW PROFILE (PINOUT)
P000371A	CERDIP (J), 16 LEAD (PINOUT)
P000464A	CERAMIC SOIC (WG), 16 LEAD (PIN OUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MIL/AERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH			
APPROVALS	DATE		
DRAWN <b>T. LEQUANG</b>	09/15/93		
DFTG. CHK.			
ENGR. CHK.			
APPROVAL			
PROJECTION 			
	INCH [MM]		
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L
DO NOT SCALE DRAWING		SHEET	OF
		1	1

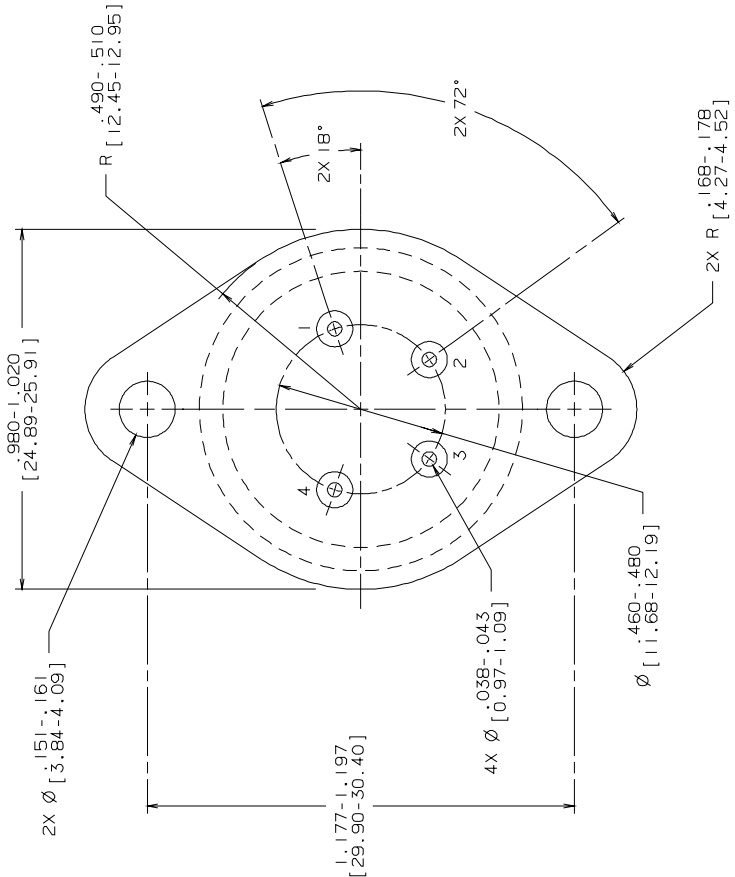
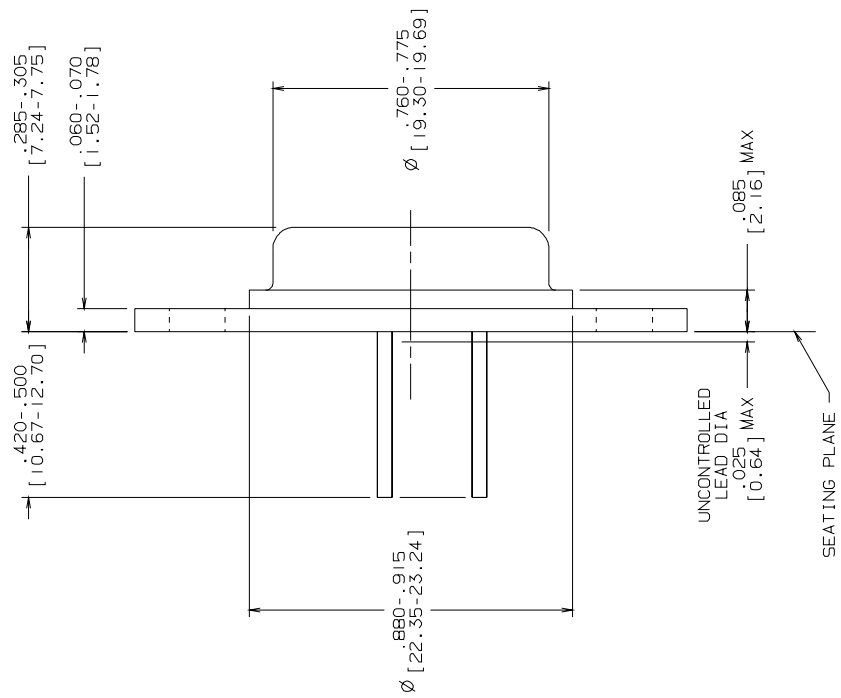
NATIONAL SEMICONDUCTOR CORPORATION  
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),  
16 LEAD

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	09260	08/14/92 DEG/

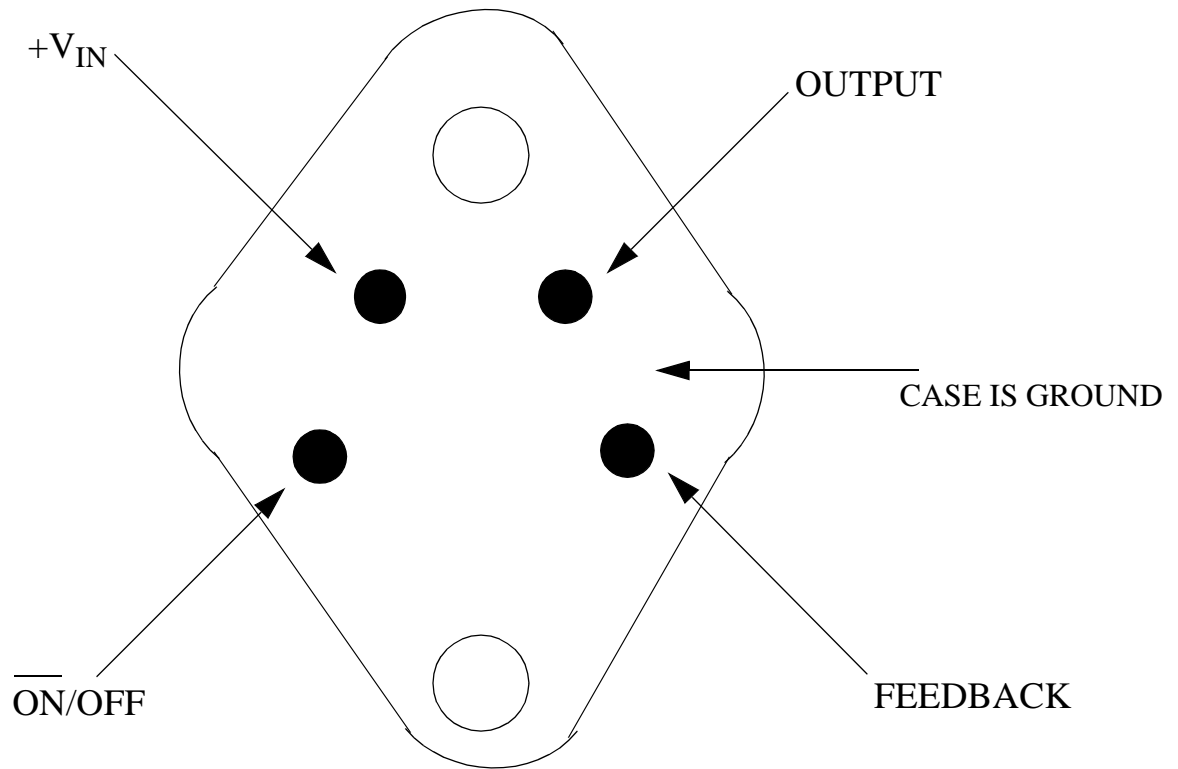


NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD HEADER TYPE SOLID BASE.
2. STANDARD LEAD FINISH:  
Sn/Pb SOLDER OVER 100 MICRONS/  
2.54 MICROMETERS MINIMUM NICKEL PLATED  
ON ALLOY 52.
3. LEAD TIPS LOCATED WITHIN ±.080 [2.03]  
OF LEAD POSITION AT BASE.
4. REFERENCE ON JEDEC REGISTRATION TO-3,  
PUBLICATION 95, PAGE 98.

MIL/AERO  
CONFIGURATION CONTROL

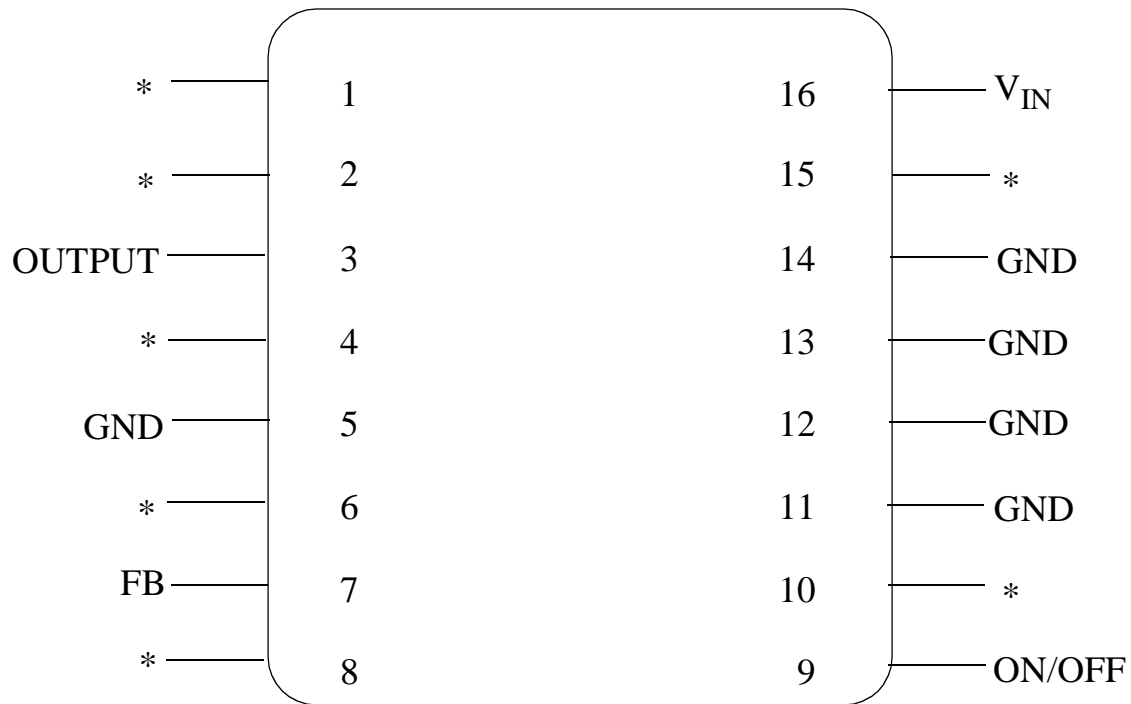
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APPROVALS	DATE
DRAWN: D.E. GRADY	10/28/91
DFG: CHK.	
ENGR. CHK.	
APPROVAL	
NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
METAL CAN, TO-3	
4 LEAD, LOW PROFILE	
SCALE	DRAWING NUMBER
N/A	C MKT-KA04B
REV	A
DO NOT SCALE DRAWING	
SHEET 1 OF 1	



LM1575K, LM1575HVK  
4 - LEAD TO-3  
CONNECTION DIAGRAM  
BOTTOM VIEW  
P000232A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050



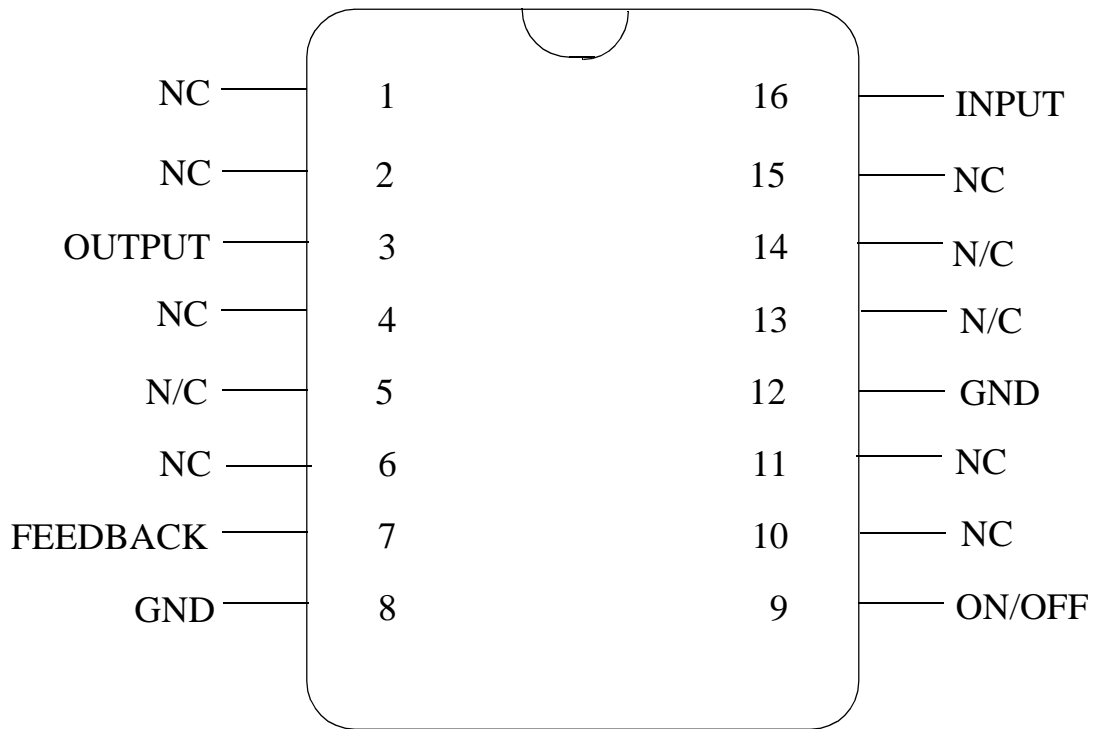
\*No Internal Connection

**LM1575J**  
**16 - LEAD DIP**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000371A**



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MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050



**LM1575WG**  
**16 - LEAD CERAMIC SOIC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000464A**

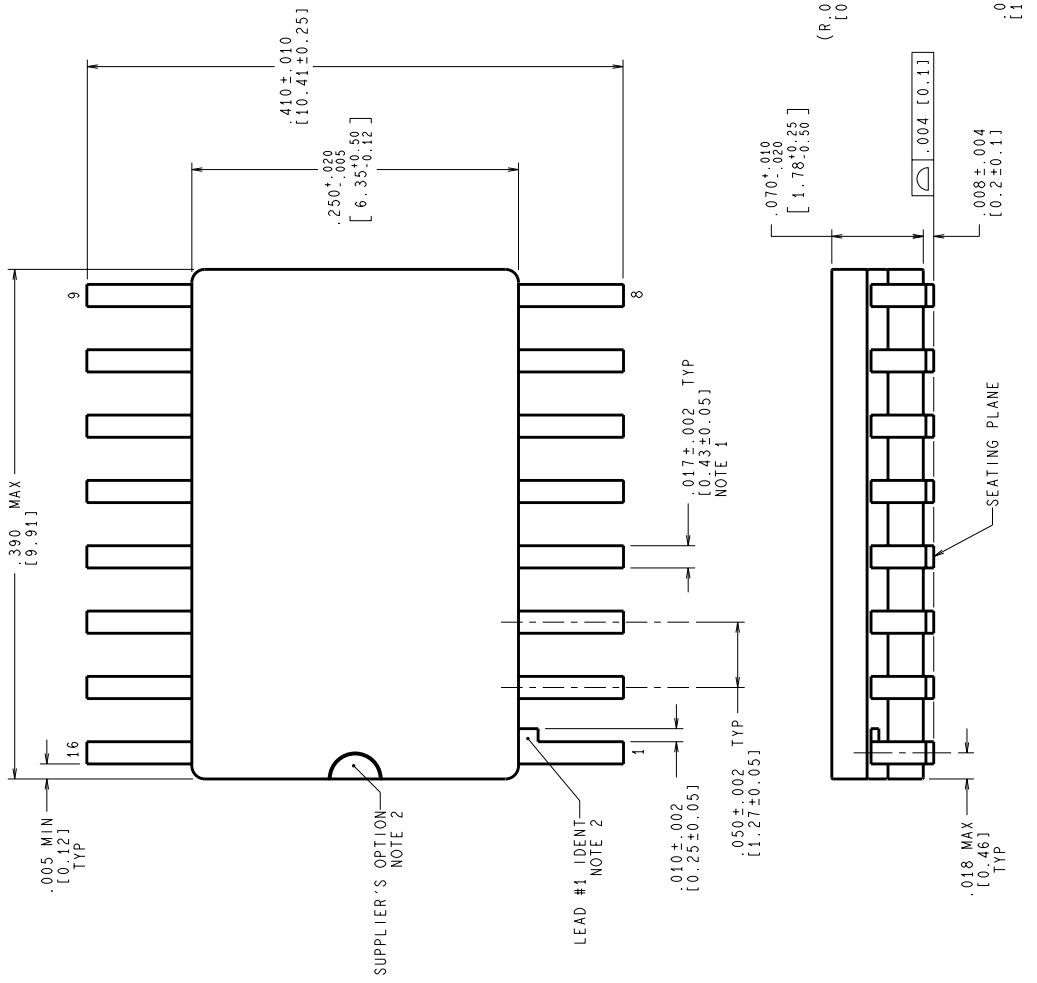


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 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM. .040±.003 WAS .037±.003	11443	04/19/1996
C	R.015(0.38) WAS R.006(0.15)	11840	10/08/1997

APPROVALS	DATE	BY/APP'D
DRN: <i>MARYA SUCHY</i>	02/29/96	MS/KH
ENGR. CHK:		MS/KH
PROJECTION		TL/



**MIL-PRF-38535  
CONFIGURATION CONTROL**

CONTROLLING DIMENSION IS INCH  
VALUES IN | ARE MILLIMETERS

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS / 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN / 0.08mm AFTER LEAD FINISH APPLIED.
  - LEAD IDENTIFICATION SHALL BE:
    - A NOTCH OR OTHER MARK WITHIN THIS AREA
    - A TAB ON LEAD 1, EITHER SIDE
  - NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

 National Semiconductor 2800 Semiconductor Dr., Santa Clara, CA 95052-8000	
DATE	02/29/96
SCALE	N/A
SIZE	C
DRAWING NUMBER	(SC)MKT-W016A
REV	C
DO NOT SCALE DRAWING	
SHEET 1 of 1	

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
2B0	M0001489	05/22/00	Barbara Lopez	Changed: MNL1575-X-ADJ Rev. 2A0 to MNL1575-ADJ-X Rev. 2B0. Added note for power dissipation for Aluminum Nitride package. Changed NSID to reflect -QML device. Changed nomenclature.
2C1	M0003690	05/22/00	Rose Malone	Update MDS: MNL1575-ADJ-X, Rev. 2B0 to MNL1575-ADJ-X, Rev. 2C1. Added reference to WG package to Main Table, Market Dwg., B/I Ckt., Pin Out to Graphics Section and to Absolute Maximum Ratings Section. Moved Controlling Documents (SMD numbers) to Features Section. Corrected typo in Recommended Operating Conditions Section.