

**MNLM1575-5.0-X REV 1B2**

 Original Creation Date: 09/08/95  
 Last Update Date: 05/22/00  
 Last Major Revision Date: 11/16/99

**SIMPLE SWITCHER(TM) 1A STEP-DOWN VOLTAGE REGULATOR**
**General Description**

The LM1575 regulator is a monolithic integrated circuit that provides all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation.

Requiring a minimum number of external components, this regulator is simple to use and includes internal frequency compensation and a fixed-frequency oscillator.

The LM1575 offers a high-efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors optimized for use with the LM1575 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed  $\pm 4\%$  tolerance on output voltage within specified input voltage and output load conditions, and  $\pm 10\%$  on the oscillator frequency. External shutdown is included, featuring 50uA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

**Industry Part Number**

LM1575-5

**NS Part Numbers**

 LM1575J-5.0-QML  
 LM1575K-5.0-QML  
 LM1575WG5.0-QML

**Prime Die**

LM1575-5

**Controlling Document**

SEE FEATURES SECTION

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

**Subgrp Description**
**Temp ( °C)**

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- Adjustable version output voltage range, 1.23V to 37V  $\pm 4\%$  max over line and load conditions
- Guaranteed 1A output current
- Requires only 4 external components
- 52KHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

CONTROLLING DOCUMENTS:

LM1575J-5.0-QML	5962-9167201QEA
LM1575K-5.0-QML	5962-9167201MXA
LM1575WG5.0-QML	5962-9167201QZA

**Applications**

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converted (Buck-Boost)

**(Absolute Maximum Ratings)**

(Note 1)

Maximum Supply Voltage	45V
$\overline{\text{ON}}$ /OFF Pin Input Voltage	$-0.3\text{V} \leq V \leq +V_{\text{in}}$
Output Voltage to Ground (Steady State)	-1V
Power Dissipation (Note 2, 3)	
METAL CAN	2.7mW
CERDIP	1.8mW
CERAMIC SOIC	1.0mW
Storage Temperature Range	$-65\text{ C} \leq T_a \leq +150\text{ C}$
Lead Temperature (Soldering, 10 seconds)	
METAL CAN	300 C
CERDIP	260 C
CERAMIC SOIC	260 C
Maximum Junction Temperature	150 C
Thermal Resistance	
ThetaJA	
METAL CAN (Still Air)	45 C/W
(500LF/Min Air flow)	10 C/W
CERDIP (Still Air)	70 C/W
(500LF/Min Air flow)	33 C/W
CERAMIC SOIC (Still Air)	121 C/W
(500LF/Min Air flow)	73 C/W
ThetaJC	
METAL CAN	3.3 C/W
CERDIP	2.0 C/W
(Note 3)	
CERAMIC SOIC	3.0 C/W
(Note 3)	
Package Weight (Typical)	
METAL CAN	TBD
CERDIP	TBD
CERAMIC SOIC	TBD
ESD Tolerance (Note 4)	3000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{j\text{max}}$  (maximum junction temperature),  $\Theta_{\text{JA}}$  (package junction to ambient thermal resistance), and  $T_A$  (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{\text{dmax}} = (T_{j\text{max}} - T_A)/\Theta_{\text{JA}}$  or the number given in the Absolute Maximum Ratings, whichever is lower.

**(Continued)**

- Note 3: The package material for these device allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
- Note 4: Human body model, 1.5k Ohms in Series with 100pF.

**Recommended Operating Conditions**

Temperature Range	-55 C ≤ Ta ≤ +125 C
Supply Voltage	40V

## Electrical Characteristics

### ELECTRICAL CHARACTERISTICS: SYSTEM PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$ , and  $I_{load} = 200mA$ .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage		1		4.950	5.050	V	1
		$0.2A \leq I_{load} \leq 1A$ , $8V \leq V_{in} \leq 40V$	1		4.850	5.150	V	1
			1		4.800	5.200	V	2, 3

### ELECTRICAL CHARACTERISTICS: DEVICE PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$ , and  $I_{load} = 200mA$ .

Vsat	Saturation Voltage	$I_{out} = 1A$	2			1.2	V	1
			2			1.4	V	2, 3
Icl	Current Limit	Peak Current, $t_{ON} \leq 3\mu S$	2		1.7	3.0	A	1
			2		1.3	3.2	A	2, 3
Il	Output Leakage Current	$V_{in} = 35V$ , Output = 0V	4			2	mA	1
		$V_{in} = 35V$ , Output = -1V	4			30	mA	1
Iq	Quiescent Current		4			10	mA	1
			4			12	mA	2, 3
Istby	Standby Quiescent Current	$\overline{ON}/OFF$ Pin = 5V (OFF)				200	uA	1
						500	uA	2, 3

### AC ELECTRICAL CHARACTERISTICS: DEVICE PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC:  $V_{in} = 12V$ , and  $I_{load} = 200mA$ .

fo	Oscillator Frequency				47	58	KHz	4
					43	62	KHz	5, 6
Dc	Max Duty Cycle (ON)		3		93		%	9

## Electrical Characteristics

### ELECTRICAL CHARACTERISTICS: ON/OFF CONTROL

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{in} = 12V$ , and  $I_{load} = 200mA$ .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 0V$			2.2		V	1
Vih	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 0V$			2.4		V	2, 3
Vil	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 5V$				1.0	V	1
Vil	$\overline{ON}/OFF$ Pin Logic Input Level	$V_{out} = 5V$				0.8	V	2, 3
Iih	$\overline{ON}/OFF$ Pin Input Current	$\overline{ON}/OFF$ Pin = 5V (OFF)				30	$\mu A$	1
Iil	$\overline{ON}/OFF$ Pin Input Current	$\overline{ON}/OFF$ Pin = 0V (ON)				10	$\mu A$	1

Note 1: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance.

Note 2: Output sourcing current. No diode, inductor or capacitor connected to output.

Note 3: Feedback removed from output and connected to 0V.

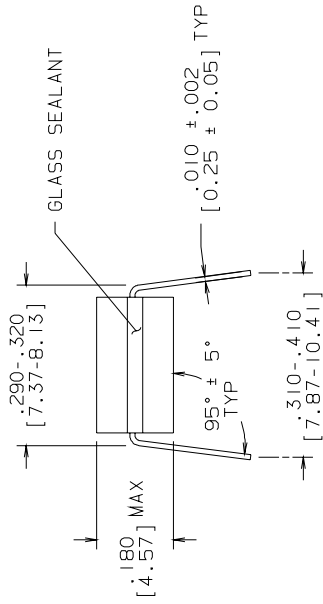
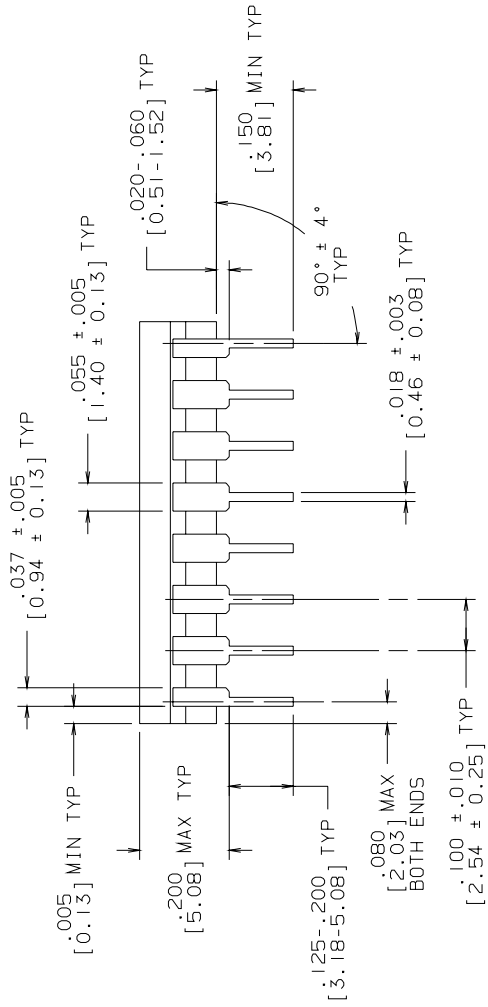
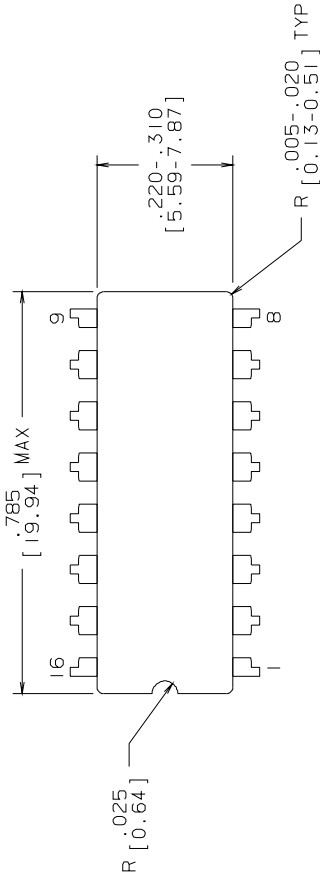
Note 4: Feedback removed from output and connected to 12V to force the output transistor OFF.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06153HRA2	METAL CAN (KA), TO-3, 4LD, LOW PROFILE (B/I CKT)
06265HRB2	CERDIP (J), 16 LEAD (B/I CKT)
06379HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
KA04BRB	METAL CAN (KA), TO-3, 4LD, LOW PROFILE (P/P DWG)
P000232A	METAL CAN (KA), TO-3, 4LD, LOW PROFILE (PINOUT)
P000371A	CERDIP (J), 16 LEAD (PINOUT)
P000464A	CERAMIC SOIC (WG), 16 LEAD (PIN OUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MIL/AERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN <b>T. LEQUANG</b>	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	
PROJECTION 	
SCALE N/A	SIZE B
DRAWING NUMBER MKT-J16A	REV L
DO NOT SCALE DRAWING	SHEET 1 OF 1

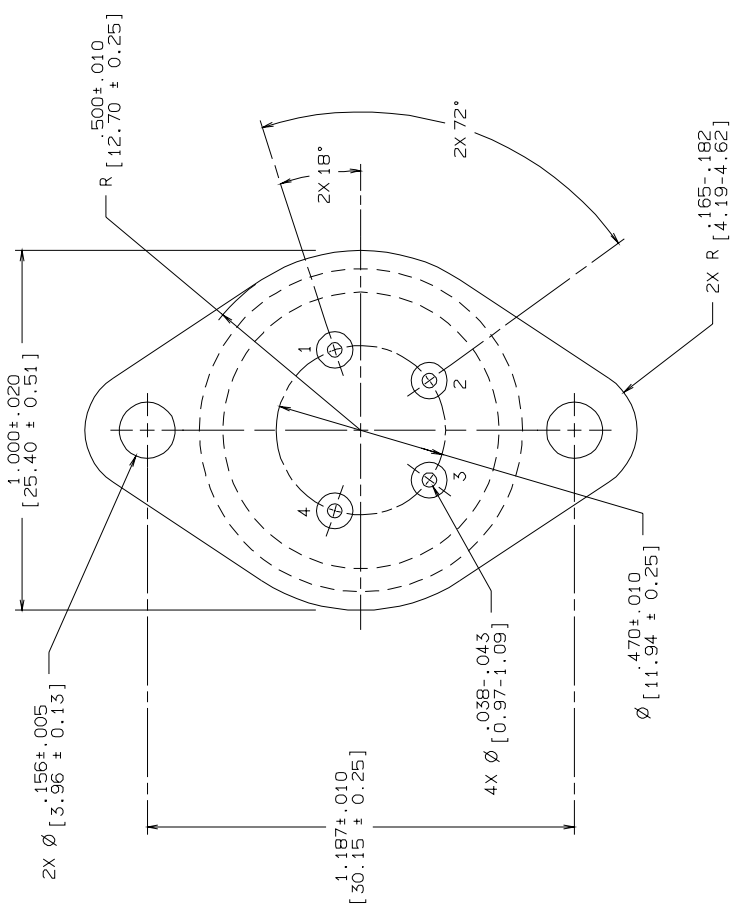
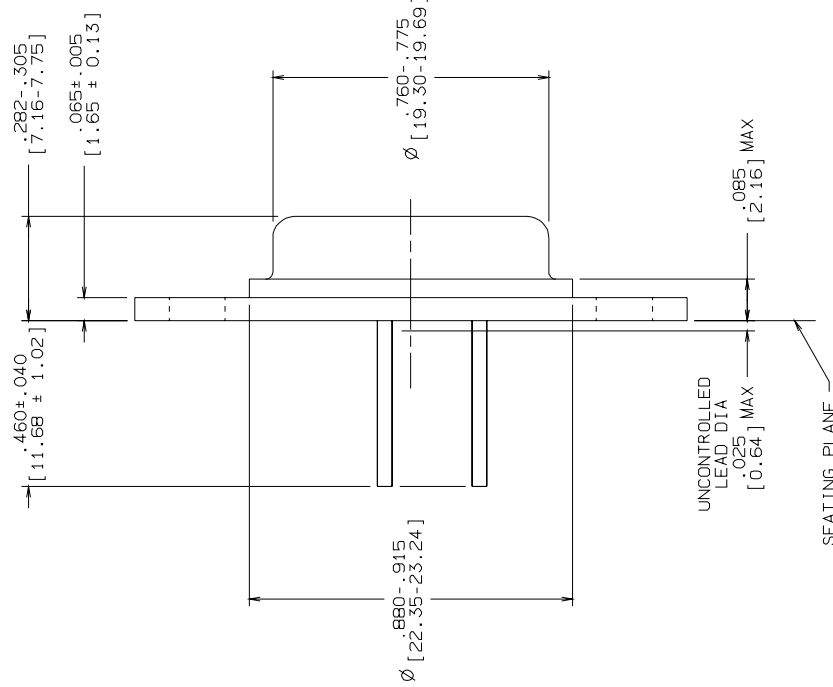
NATIONAL SEMICONDUCTOR CORPORATION  
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),  
16 LEAD

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL [.282-.305] WAS [.285-.305] [.16-.175] WAS [.16-.175] [.165-.175] WAS [.165-.175] NOTE 4: UPDATE MIL/AERO STAMP; NOMINAL DIM'S WERE LIMIT DIM'S.	09260	08/14/92 DEG/FL
B	WAS [.165-.175] CORRECT NOTE 4: UPDATE MIL/AERO STAMP; NOMINAL DIM'S WERE LIMIT DIM'S.	10916	04/10/95 MS/



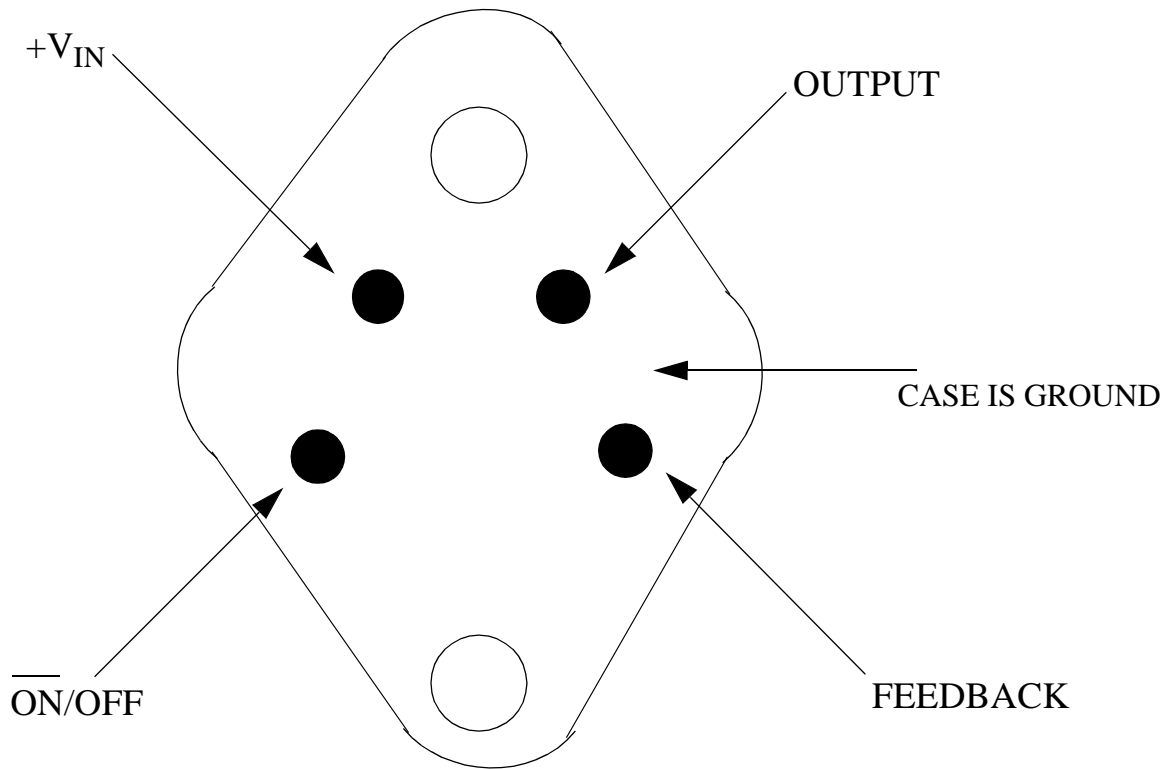
NOTES: UNLESS OTHERWISE SPECIFIED

- STANDARD HEADER TYPE SOLID BASE.
- STANDARD LEAD FINISH:  
Sn/Pb SOLDER OVER 100 MICRONS/  
2.54 MICROMETERS MINIMUM NICKEL PLATED  
ON ALLOY 52.
- LEAD TIPS LOCATED WITHIN .080 [2.03]  
OF LEAD POSITION AT BASE.
- REFERENCE JEDEC REGISTRATION TO-3,  
PUBLICATION 95, PAGE 98.

CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535  
CONFIGURATION CONTROL

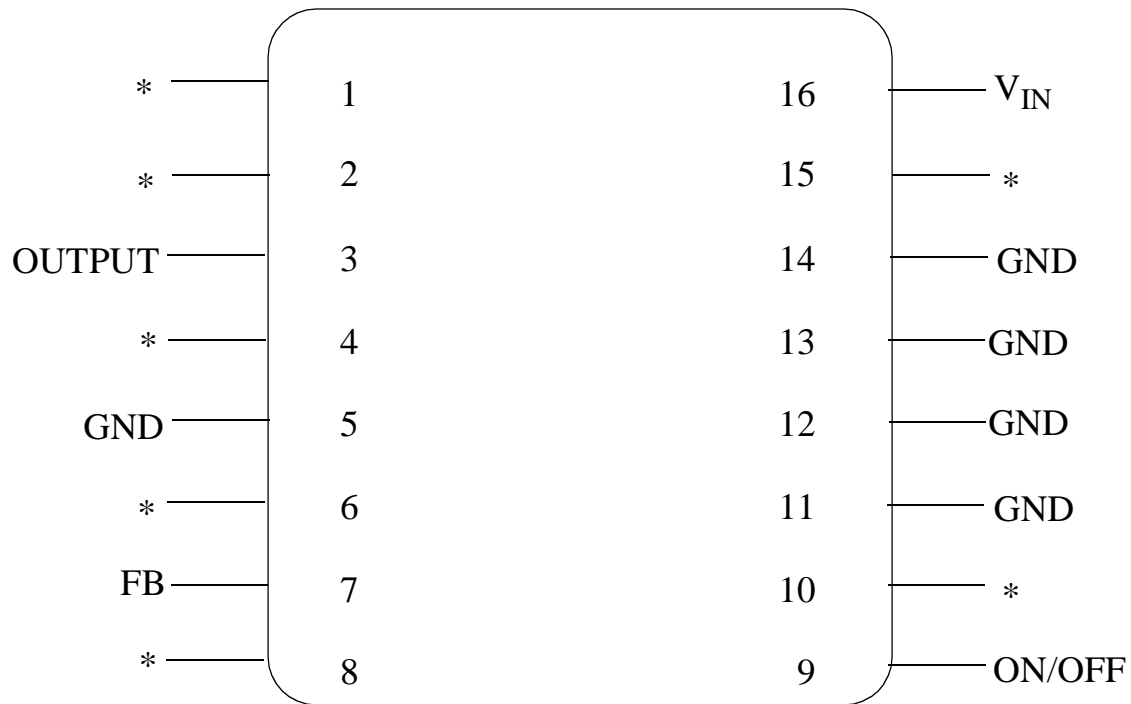
APPROVALS	DATE	National Semiconductor
DRAWN D.E. GRADY	10/28/91	2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DTG: CHK.		
ENGR: CHK.		
METAL CAN, TO-3, 4 LEAD, LOW PROFILE		
PROJECTION	SCALE	DRAWING NUMBER
	N/A	C MKT-KA04B
	DO NOT SCALE DRAWING	SHEET 1 OF 1



LM1575K, LM1575HVK  
4 - LEAD TO-3  
CONNECTION DIAGRAM  
BOTTOM VIEW  
P000232A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050



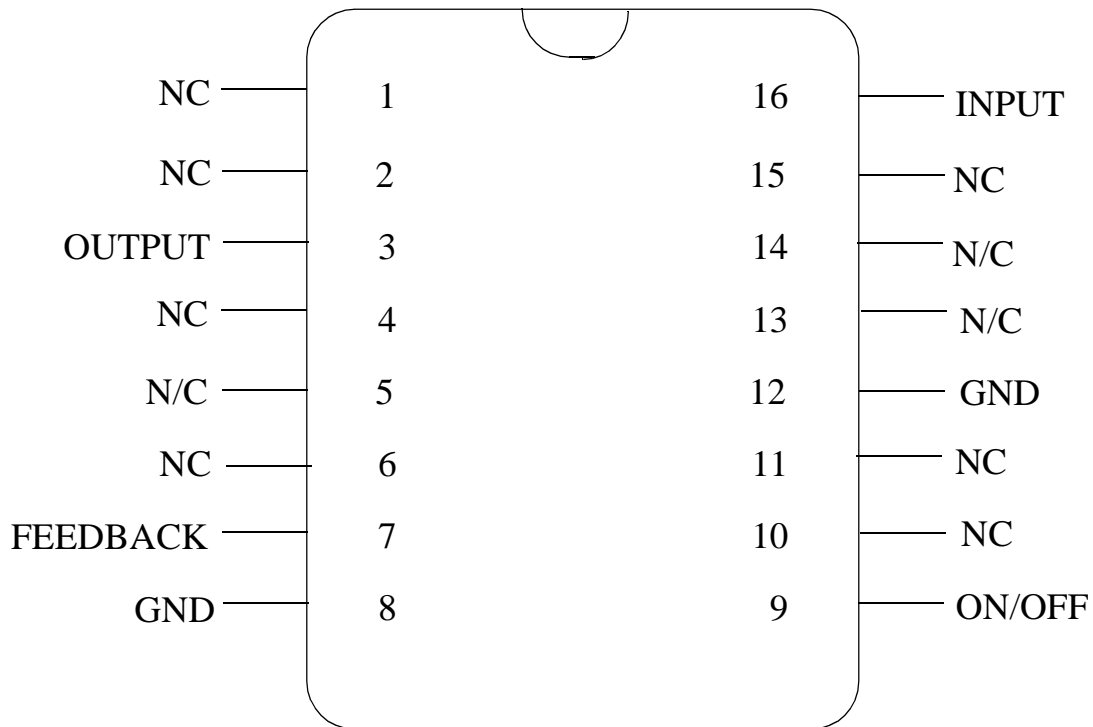
\*No Internal Connection

**LM1575J**  
**16 - LEAD DIP**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000371A**



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 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050



**LM1575WG**  
**16 - LEAD CERAMIC SOIC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000464A**

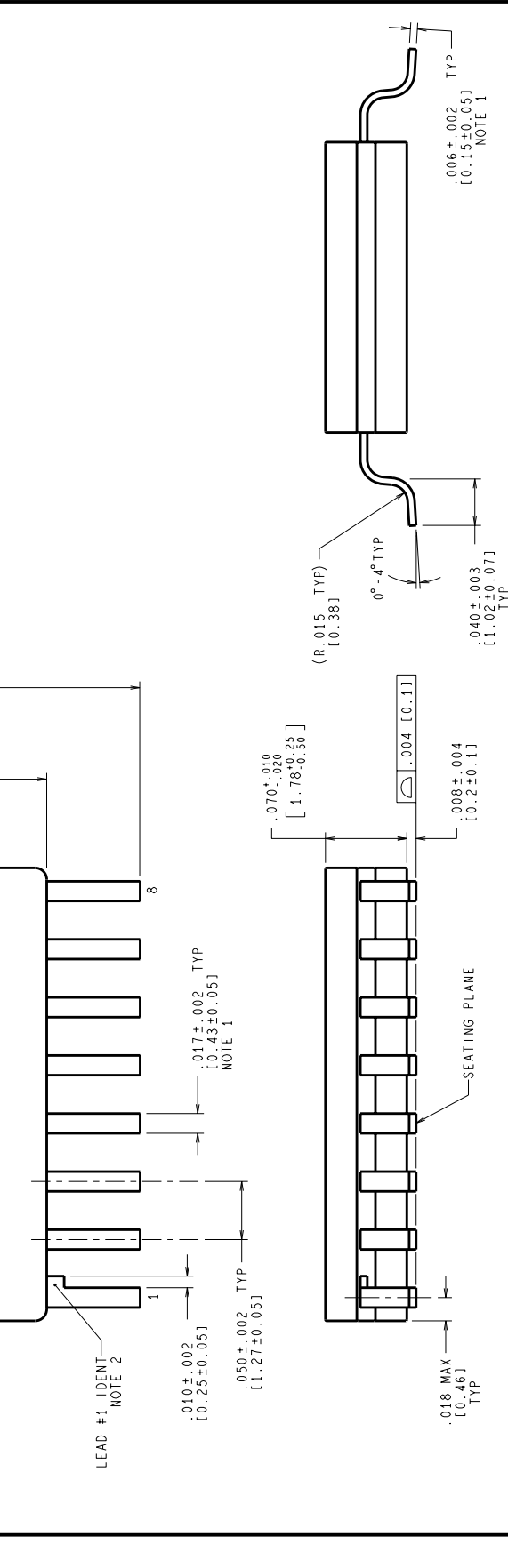
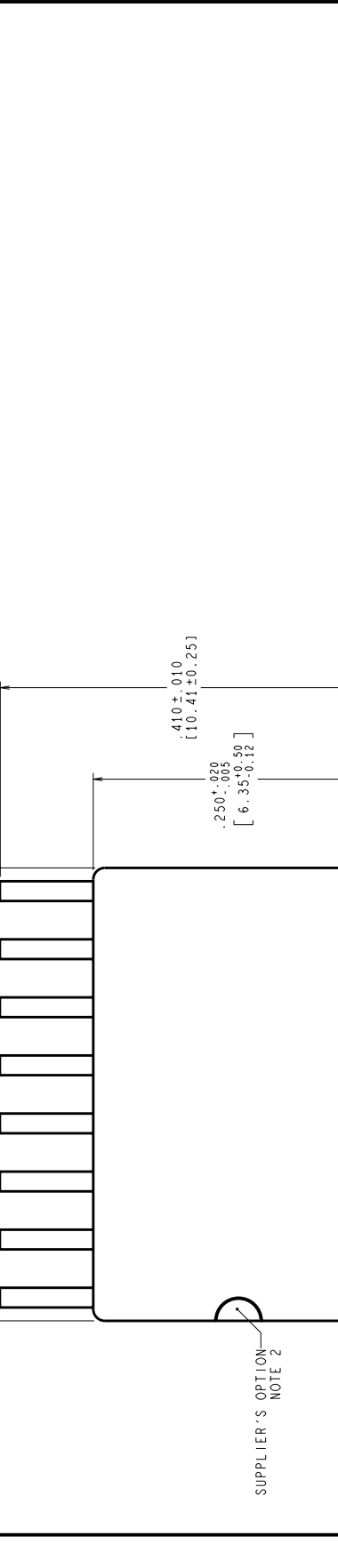


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MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM. .040±.003 WAS .037±.003	11443	04/19/1996
C	R.015(0.38) WAS R.006(0.15)	11840	10/08/1997


APPROVALS	DATE	BY/APP'D
DRN: <i>MARYA SUCHY</i>	02/29/96	MS/KH
ENGR. CHK.		MS/KH
PROJECTION		
		
SCALE	SIZE	REV
N/A	C	C
DO NOT SCALE DRAWING		



MIL-PRF-38535  
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH  
VALUES IN | ARE MILLIMETERS

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS / 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN / 0.08mm AFTER LEAD FINISH APPLIED.
  - LEAD 1 IDENTIFICATION SHALL BE:
    - A NOTCH OR OTHER MARK WITHIN THIS AREA
    - A TAB ON LEAD 1, EITHER SIDE
  - NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

 National Semiconductor 2800 Semiconductor Dr., Santa Clara, CA 95052-8000	
<b>CERPACK, 16 LEAD, GULL WING</b>	DRAWING NUMBER <b>(SC)MKT-WG16A</b>
SCALE <b>N/A</b>	SIZE <b>C</b>
REV <b>C</b>	
DO NOT SCALE DRAWING SHEET 1 of 1	

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
0C0	M0001548	12/06/99	Barbara Lopez	Changed: MNL1575-X-5 Rev. 0B0 to MNL1575-5.0-X Rev. 0C0. Added power dissipation note for Aluminum Nitride package. Changed nomenclature.
1A1	M0003599	05/22/00	Rose Malone	Update MDS: MNL1575-5.0-X, Rev. 0C0 to MNL1575-5.0-X, Rev. 1A1. Added information for WG pkg.
1B2	M0003691	05/22/00	Rose Malone	Update MDS: MNL1575-5.0-X, Rev. 1A1 to MNL1575-5.0-X, Rev. 1B2. Corrected typo's in Features Section, Absolute Maximum Ratings Section. Added ESD - Note 4 to the Note Section, WG package B/I Ckt. to Graphics Section