

**MJLF412-X REV 0C1**

Original Creation Date: 05/02/95  
Last Update Date: 04/14/98  
Last Major Revision Date: 05/02/95

**LOW OFFSET, LOW DRIFT DUAL JFET INPUT OPERATIONAL  
AMPLIFIER**

**General Description**

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

**Industry Part Number**

LF412

**NS Part Numbers**

JL412BGA  
JL412BPA

**Prime Die**

LF412

**Controlling Document**

38510/11905

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

Subgrp	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25

**Features**

- Internally trimmed offset voltage 1mV (max)
- Input offset voltage drift 10uV/ C (max)
- Low input bias current 50pA
- Low input noise Current 0.01pA/Root Hz
- Wide gain bandwidth 3MHz (min)
- High slew rate 10V/uS (min)
- Low supply current 1.8mA/Amplifier
- High input impedance 10E12 Ohms
- Low total harmonic distortion AV=10, RL=10K,  $\pm 0.02\%$   
Vo=20 Vp-p, BW=20 Hz - 20KHz
- Low 1/f noise corner 50Hz
- Fast settling time to 0.01% 2uS

**(Absolute Maximum Ratings)**

(Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration (Note 4)	Continuous
Power Dissipation (Note 2)	
H Package	800mW
J Package	TBD
Tjmax	175 C
ThetaJA (Typical)	
METAL CAN	
(Still Air)	160 C/W
(500 LF/Min Air Flow)	83 C/W
CERDIP	
(Still Air)	122 C/W
(500 LF/Min Air Flow)	66 C/W
ThetaJC	
METAL CAN	38 C/W
CERDIP	15 C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{dmax} = (T_{jmax} - T_A) / \Theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

## Recommended Operating Conditions

Operating Temperature Range	-55 C ≤ TA ≤ 125 C
Supply Voltage Range	±5V to ±15V
Storage Temperature Range	-65 C ≤ TA ≤ 150 C
Lead Temperature (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 1)	1700V

Note 1: Human body model, 1.5K Ohms in series with 100pF

## Electrical Characteristics

### DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $\pm V_{cc} = \pm 15V$ ,  $V_{cm} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-5	5	mV	1
					-7	7	mV	2, 3
					-5	5	mV	1
					-7	7	mV	2, 3
		$\pm V_{cc} = \pm 5V$			-5	5	mV	1
		$\pm V_{cc} = \pm 5V$			-7	7	mV	2, 3
+Iib	Input Bias Current	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-0.4	0.2	nA	1
					-10	50	nA	2
					-0.2	0.2	nA	1
					-10	50	nA	2
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-0.2	1.2	nA	1
					-10	70	nA	2
-Iib	Input Bias Current	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-0.4	0.2	nA	1
					-10	50	nA	2
					-0.2	0.2	nA	1
					-10	50	nA	2
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-0.2	1.2	nA	1
					-10	70	nA	2
Iio	Input Offset Current				-0.1	0.1	nA	1
					-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	+Vcc = 20V to 10V, -Vcc = -15V			80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+Vcc = 15V, -Vcc = -20V to -10V			80		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	Vcm = -11V to +11V			80		dB	1, 2, 3
Ios(+)	Output Short Circuit Current	$t \leq 25mS$			-80		mA	1, 2, 3
Ios(-)	Output Short Circuit Current	$t \leq 25mS$				80	mA	1, 2, 3

## Electrical Characteristics

### DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $\pm V_{cc} = \pm 15V$ ,  $V_{cm} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I <sub>cc</sub>	Supply Current					7	mA	1, 2
						8	mA	3
DELTA V <sub>io</sub> / DELTA T	Input Offset Voltage	25 C ≤ TA ≤ +125 C	1		-30	30	uV/C	2
		-55 C ≤ TA ≤ 25 C	1		-30	30	uV/C	3
+V <sub>op</sub>	Output Voltage Swing	RL = 10K Ohms			12		V	4, 5, 6
		RL = 2K Ohms			10		V	4, 5, 6
-V <sub>op</sub>	Output Voltage Swing	RL = 10K Ohms				-12	V	4, 5, 6
		RL = 2K Ohms				-10	V	4, 5, 6
AVS-	Open Loop Voltage Gain	RL = 2K Ohms, V <sub>out</sub> = -10V	2		50		V/mV	4
			2		25		V/mV	5, 6
AVS+	Open Loop Voltage Gain	RL = 2K Ohms, V <sub>out</sub> = 10V	2		50		V/mV	4
			2		25		V/mV	5, 6
AVS	Open Loop Voltage Gain	RL = 10K Ohms, V <sub>out</sub> = ±2V, ±V <sub>cc</sub> = ±5V	2		20		V/mV	4, 5, 6

## Electrical Characteristics

### AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC:  $\pm V_{cc} = \pm 15V$ ,  $V_{cm} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TR(tr)	Transient Response Rise Time	AV = 1, Vin = 50mV, CL = 100pF, RL = 2K Ohms	3			200	nS	7, 8A, 8B
TR(os)	Transient Response Rise Time	AV = 1, Vin = 50mV, CL = 100pF, RL = 2K Ohms	3			40	%	7, 8A, 8B
SR+	Slew Rate	Vin = -5V to +5V			7		V/uS	7
					5		V/uS	8A, 8B
SR-	Slew Rate	Vin = +5V to -5V			7		V/uS	7
					5		V/uS	8A, 8B
NI(BB)	Noise Broadband	BW = 10Hz to 15KHz, RS = 0 Ohms	4			15	uVrms	7
NI(PC)	Noise Popcorn	BW = 10Hz to 15KHz, RS = 100K Ohms	4			80	uVpk	7
CS	Channel Separation	RL = 2K Ohms, Vin = $\pm 10V$	4		80		dB	7
tS(+)	Settling Time	AV = 1	3			1500	nS	12
tS(-)	Settling Time	AV = 1	3			1500	nS	12

### DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $\pm V_{cc} = \pm 15V$ ,  $V_{cm} = 0V$ . "Delta calculations performed at group B-5".

Vio	Input Offset Voltage				-1	1	mV	1
+Iib	Input Bias Current				-0.1	0.1	nA	1
-Iib	Input Bias Current				-0.1	0.1	nA	1

- Note 1: Calculated parameter  
 Note 2: Datalog reading in K = V/mV.  
 Note 3: Bench test  
 Note 4: Test on either A360, J273 AC or bench test.

## Graphics and Diagrams

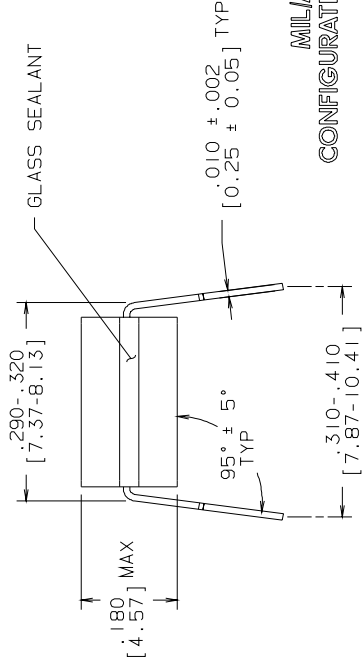
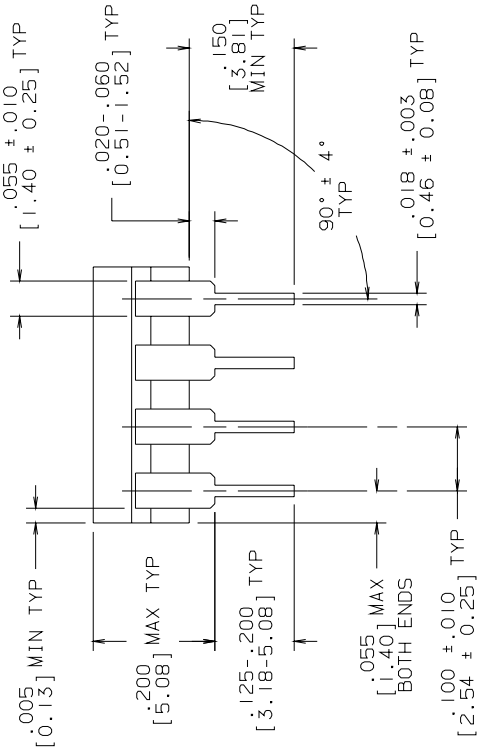
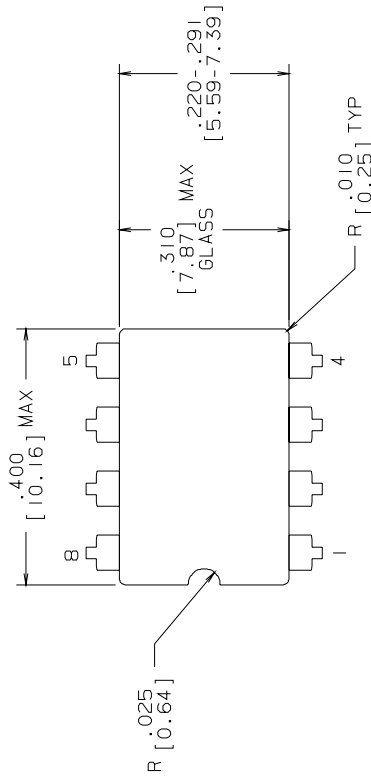
GRAPHICS#	DESCRIPTION
05487HRA3	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
05974HRA2	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000176A	METAL CAN (H), 8 LEAD (PINOUT)
P000177A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.



REV I S I O N S

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/



MILAERO  
CONFIGURATION CONTROL  
MIL-M-38510  
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

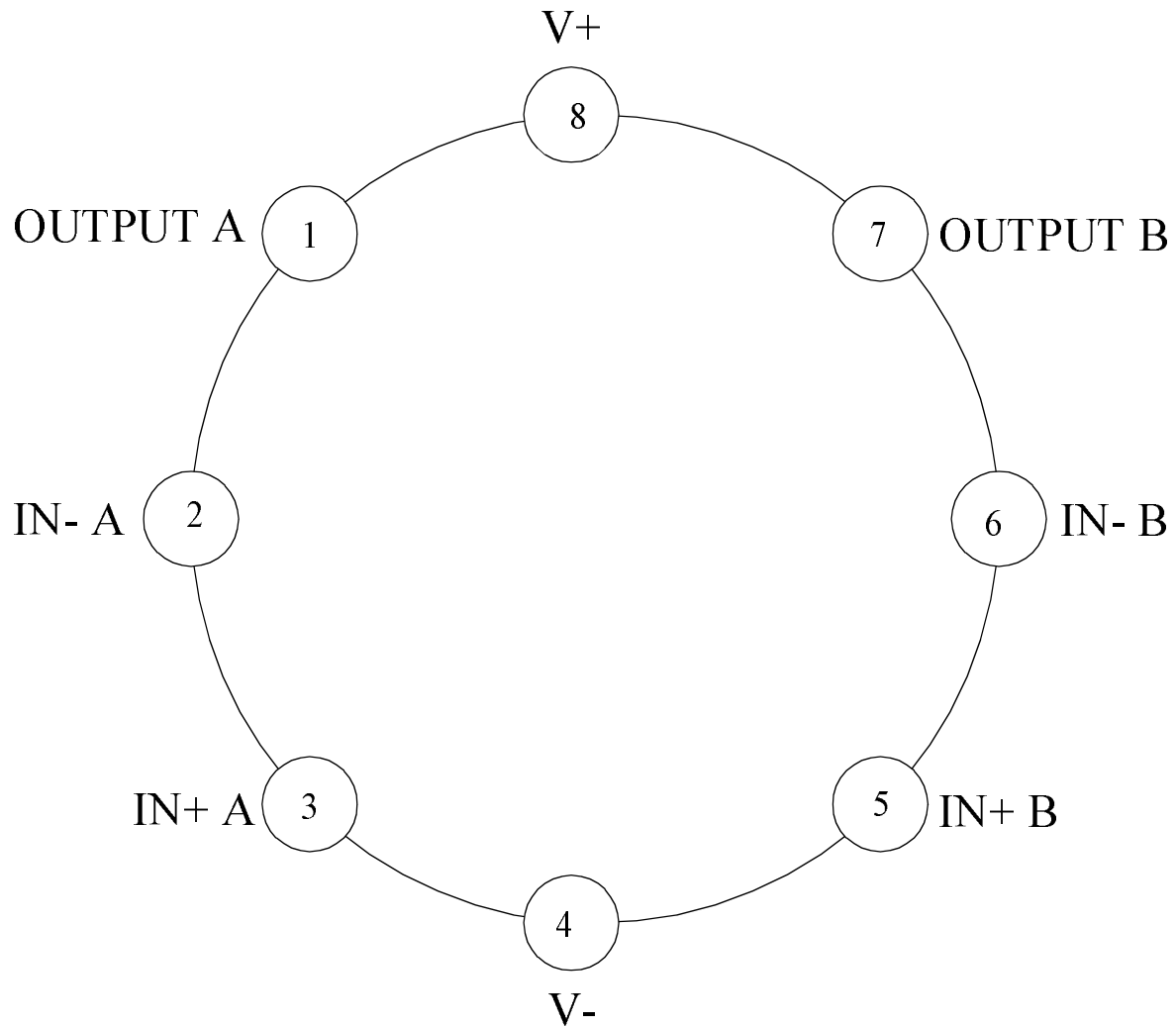
APPROVALS	DATE	APPROVALS	DATE
DRAWN <i>T. LEQUANG</i>	09/21/93	NATIONAL SEMICONDUCTOR CORPORATION	
DFTG. CHK.		2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
ENGR. CHK.			
APPROVAL			

CERDIP (J),  
8 LEAD

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J08A	L
	DO NOT SCALE DRAWING	SHEET	OF	

NOTES: UNLESS OTHERWISE SPECIFIED

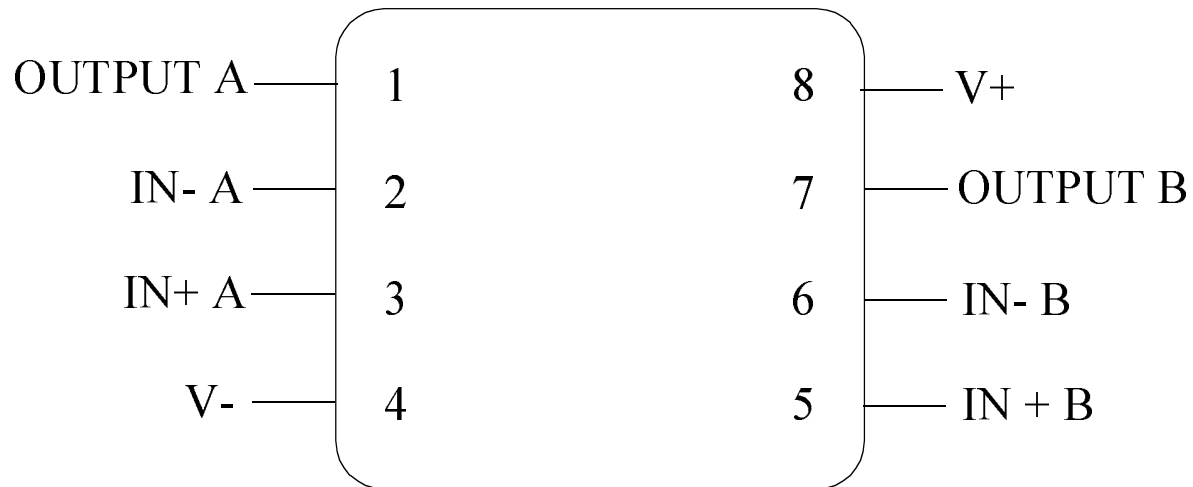
- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.



LF412H  
8 - PIN METAL CAN  
CONNECTION DIAGRAM  
TOP VIEW  
P000176A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050



LF412J  
8 - LEAD DIP  
CONNECTION DIAGRAM  
TOP VIEW  
P000177A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
0C1	M0002838	04/14/98	Barbara Lopez	Update MDS: MJLF412-X Rev. 0B0 to MJLF412-X Rev. 0C1. Updated graphics. Added thermal data. Added power dissipation and Absolute note. Deleted Rev. A for drawing number per Spec Control.