



MICROCIRCUIT DATA SHEET

MNCOP8SAC728-X REV 0B0

Original Creation Date: 09/02/99
Last Update Date: 05/15/00
Last Major Revision Date: 12/15/99

8 Bit One-Time Programmable (OTP) Microcontroller

General Description

The COPSAC7 OTP microcontroller is a member of the COP8 feature family using an 8-bit single chip core architecture. These devices are fabricated in National Semiconductor's high density EPROM process and are offered in a variety of packages, temperature ranges and voltage ranges to satisfy a wide variety of applications.

Industry Part Number

COP8SAC7

NS Part Numbers

COP8SAC728J-MIL

Prime Die

TSL8SAC7A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 8-bit OTP microcontroller
- OTP program space with read/write protection(fully secured)
- Quiet Design (low radiated emissions)
- 4K OTP EPROM
- User selectable clock options
 - > Crystal/Resonator options
 - > Crystal/Resonator option with on-chip bias resistor
 - > External Oscillator
 - > Internal R/C Oscillator
- Internal Power-on Reset -- user selectable
- WATCHDOG and Clock Monitor Logic - user selectable

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	7V
Voltage at Any Pin	-0.6V to Vcc +0.6V
Total Current to Vcc (Source)	80mA
Total Current from GND (Sink)	100mA
Storage Temperature Range	-65 C to +140 C

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

Recommended Operating Conditions

Operating Voltage	4.5V (minimum) 5.5V (maximum)
Power Supply Rise Time from 0.0V (on Chip Power-on Reset Selected)	10ns (minimum) 50ms (maximum)
VCC Start Voltage to Guarantee POR	0.25V (maximum)
Power Supply Ripple (Peak-to-Peak) (maximum rate of voltage change must be <0.5 V/ms)	0.1Vcc (maximum)

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{cc} = 5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IDD Dynamic	Supply Current	CKI = 10MHz, $V_{cc} = 5.5V$	1, 6, 9			6	mA	4, 5, 6
		CKI = 64kHz, $V_{cc} = 4.0V$	12			155	uA	4, 5, 6
IDD Halt	HALT Current	$V_{cc} = 5.5V$, CKI = 0MHz Watchdog Disabled	2, 5, 8			30	uA	1, 2, 3
IDD Idle	IDLE Current	$V_{cc} = 5.5V$, CKI = 10MHz	1, 6, 9			1.5	mA	4, 5, 6
Leakage	Hi-Z Input Leakage	$V_{cc} = 5.5V$	5, 8		-5	5	uA	1, 2, 3
In_Pup	Input Pullup Current	$V_{cc} = 5.5V$, $V_{in} = 0.0V$	5, 8		-35	-400	uA	1, 2, 3
PP_D	Output Current Source	D Ports $V_{cc} = 4.5V$, $V_{oh} = 3.3V$	5, 8		-0.4		mA	1, 2, 3
PP_OTH	Output Current Source	Fx, Gx, Lx Ports $V_{cc} = 4.5V$, $V_{oh} = 3.3V$	5, 8		-0.4		mA	1, 2, 3
PS_D	Output Current Sink	D Ports $V_{cc} = 4.5V$, $V_{ol} = 1.0V$	5, 8		9		mA	1, 2, 3
PS_L1	Output Current Sink	L0-L3 Ports $V_{cc} = 4.5V$, $V_{ol} = 1.0V$	5, 8		9		mA	1, 2, 3
PS_L2	Output Current Sink	L4-L7 Ports $V_{cc} = 4.5V$, $V_{ol} = 0.4V$	5, 8		1.4		mA	1, 2, 3
PS_6	Output Current Sink	Fx, Gx Ports $V_{cc} = 4.5V$, $V_{ol} = 0.4V$	5, 8		1.4		mA	1, 2, 3
Vr	RAM Retention Voltage		12		2.0		V	1, 2, 3
	V_{cc} Rise Time from a $V_{cc} \geq 2.0V$		3, 12		12		us	1, 2, 3
CI	Input Capacitance		12			7	pF	4
CIO	Input/Output Capacitance		12			1000	pF	4
	Input Levels (V_{ih} , V_{il})	Logic High	5, 8, 11		0.8 V_{cc}		V	1, 2, 3
		Logic Low	5, 8, 11			0.2 V_{cc}	V	1, 2, 3
	Value of the Internal Bias Resistor for the Crystal/Resonator Oscillator		12		0.5	2.0	Mohm	1, 2, 3

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{cc} = 5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	CKI Resistance to VCC or GND when R/C Oscillator is selected	$V_{cc} = 5.5V$	12		5	11	Kohm	1, 2, 3
	G & L Port Input Hysteresis		12		0.25 V_{cc}		V	1, 2, 3
	Allowable Sink Current per pin D Outputs and L0-L3		12			15	mA	1, 2, 3
	Allowable Sink Current per Pin All others		12			3	mA	1, 2, 3
	Max Input Current without Latchup	Room Temp	4, 12			± 200	mA	1

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $V_{cc} = 5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	Instruction Cycle Time (tC)	Crystal/Resonator, External $4.5V \leq V_{cc} \leq 5.5V$	12		1.0	DC	us	9, 10, 11
		Internal R/C Oscillator $4.5V \leq V_{cc} \leq 5.5V$	12			DC	us	9, 10, 11
		R/C Oscillator Frequency Variation $4.5V \leq V_{cc} \leq 5.5V$	12			40	%	9, 10, 11
	External CKI	Clock Duty Cycle, $f_r = \text{Max}$	12		45	55	%	9, 10, 11
		Rise Time, $f_r = 10 \text{ MHz Ext Clock}$	12			12	ns	9, 10, 11
		Fall Time, $f_r = 10 \text{ MHz Ext Clock}$	12			8	ns	9, 10, 11
	MICROWIRE Set-Up Time (Tuws)	(see Figure A)	12, 13		20		ns	9, 10, 11
	MICROWIRE Hold Time (Tuwh)	(see Figure A)	12, 13		56		ns	9, 10, 11
	MICROWIRE Output Propagation Delay (Tupd)	(see Figure A)	12, 13			220	ns	9, 10, 11
	MICROWIRE Maximum Shift Clock Master Mode		12			500	kHz	9, 10, 11
	MICROWIRE Maximum Shift Clock Slave Mode		12			1	mHz	9, 10, 11
	Input Pulse Width	Interrupt Input High Time	12		1		tC	9, 10, 11
		Interrupt Input Low Time	12		1		tC	9, 10, 11
		Timer 1, 2, 3 Input High Time	12		1		tC	9, 10, 11
		Timer 1, 2, 3 Input Low Time	12		1		tC	9, 10, 11
	Reset Pulse Width		12		1		us	9, 10, 11

Note 1: Supply and IDLE currents are measured with CKI driven with a square wave oscillator, CKO driven 180 degrees out of phase with CKI, inputs connected to VCC and outputs driven low but not connected to a load.

Note 2: The HALT mode will stop CKI from oscillating in the R/C and the Crystal configurations. In the R/C configuration, CKI is forced high internally. In the crystal or external configuration, CKI is TRI-STATE. Measurement of IDD HALT is done with device neither sourcing nor sinking current; with L, F, G0 and G2-G5 programmed as low outputs and not driving a load; all outputs programmed low and not driving a load; all inputs tied to Vcc; WATCHDOG and clock monitor disabled. Parameter refers to HALT mode entered via setting bit 7 of the G port data register.

(Continued)

- Note 3: Rise times faster than this specification may reset the device if POR is enabled and may affect the value of Idle Timer if POR is not enabled.
- Note 4: Pins G6 and RESET are designed with a high voltage input network. These pins allow input voltages > Vcc and the pins will have sink current to Vcc when biased at voltages > Vcc (the pins do not have source current when biased at a voltage below Vcc). The effective resistance to Vcc is 750 ohms (typical). These two pins will not latch up. The voltage at the pins must be limited to < 14V. WARNING: Voltages in excess of 14V will cause damage to the pins. This warning excludes ESD transients.
- Note 5: Screen tested 100% on each device at -55C, +25C and +125C temperature, subgroups 1, 2, 3, 7 and 8.
- Note 6: Screen tested 100% on each device at -55C, +25C and +125C temperature, subgroups 4, 5, 6, 7 and 8.
- Note 7: Screen tested 100% on each device at -55C, +125C and +25C temperature, subgroups A9, A10 and A11.
- Note 8: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A1, 2, 3, 7 and 8.
- Note 9: Sample tested (Method 5005, Table 1) on each MFG. lot at -55C, +25C and +125C temperature, subgroups 4, 5, 6, 7 and 8.
- Note 10: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A9, A10 and A11.
- Note 11: Guaranteed by applying specified input condition during Function testing.
- Note 12: Parameter characterized but not tested.
- Note 13: The output propagation delay is referenced to the end of the instruction cycle where the output change occurs.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
AN00037A	TIMING DIAGRAM

See attached graphics following this page.

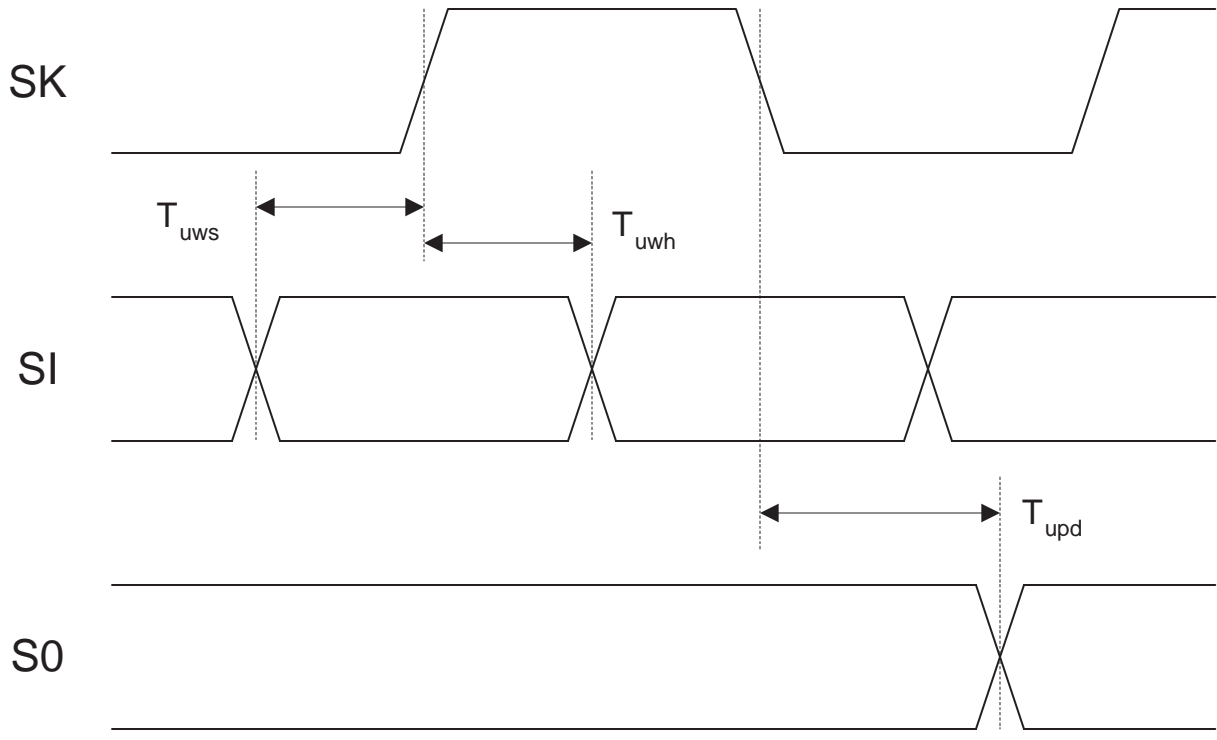


Figure A
MICROWIRE Timing Diagram

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003558	05/15/00	Bill Petcher	Initial MDS Release
0B0	M0003666	05/15/00	Linda Collins	New Update: MDS MNCOP8SAC728-X Rev. 0B0 Made corrections in the features section of the MDS by adding OTP to the first paragraph. Rewrote the 4th paragraph to read '4K OTP EPROM' instead of '8 bytes of user storage space in EPROM'.