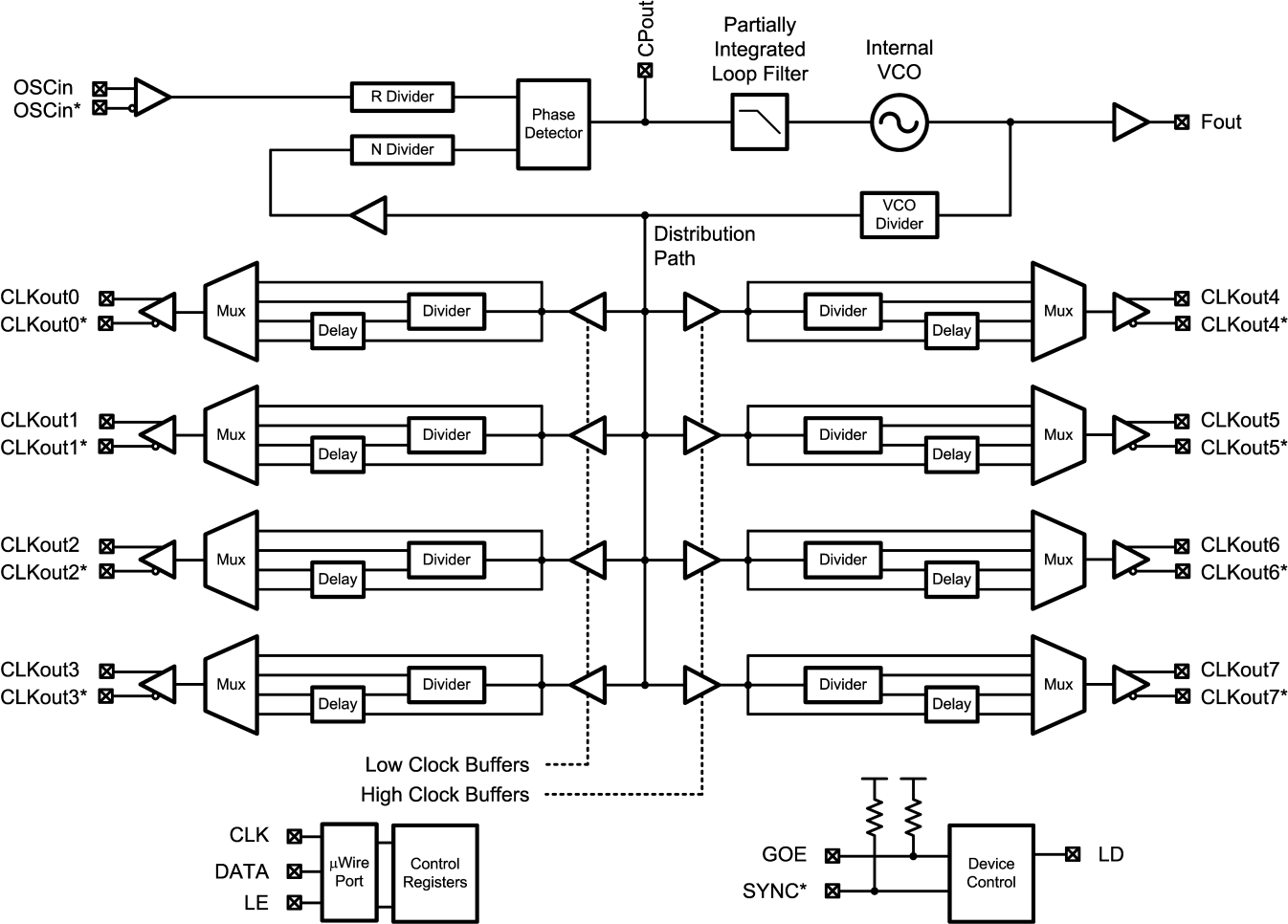
OSCin
OSCin*
R Divider
N Divider
Phase Detector
CPout
Partially Integrated Loop Filter
Internal VCO
Fout
VCO Divider
Distribution Path
CLKout0
CLKout0*
Mux
Delay
Divider
CLKout4
CLKout4*
CLKout1
CLKout1*
CLKout5
CLKout5*
CLKout2
CLKout2*
CLKout6
CLKout6*
CLKout3
CLKout3*
CLKout7
CLKout7*
Low Clock Buffers
High Clock Buffers
CLK
DATA
LE
µWire Port
Control Registers
GOE
SYNC*
Device Control
LD