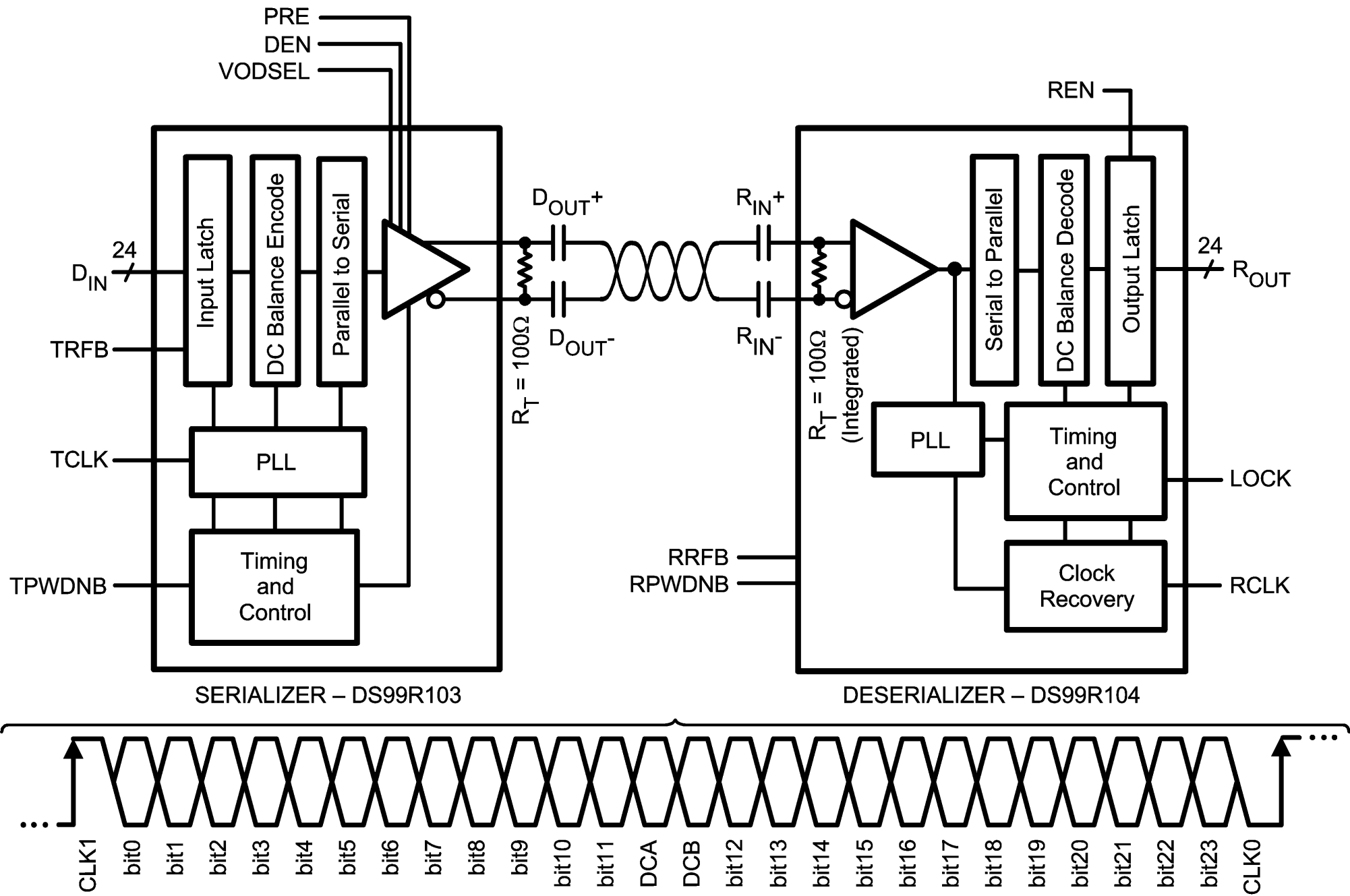
PRE
DEN
VODSEL
REN
24
D_{IN}
TRFB
TCLK
TPWDNB
Input Latch
DC Balance Encode
Parallel to Serial
PLL
Timing and Control
D_{OUT}+
D_{OUT}-
R_T = 100Ω
R_{IN}+
R_{IN}-
R_T = 100Ω (Integrated)
RRFB
RPWDNB
Serial to Parallel
DC Balance Decode
Output Latch
PLL
Timing and Control
Clock Recovery
24
R_{OUT}
LOCK
RCLK
SERIALIZER – DS99R103
DESERIALIZER – DS99R104
CLK1
bit0
bit1
bit2
bit3
bit4
bit5
bit6
bit7
bit8
bit9
bit10
bit11
DCA
DCB
bit12
bit13
bit14
bit15
bit16
bit17
bit18
bit19
bit20
bit21
bit22
bit23
CLK0