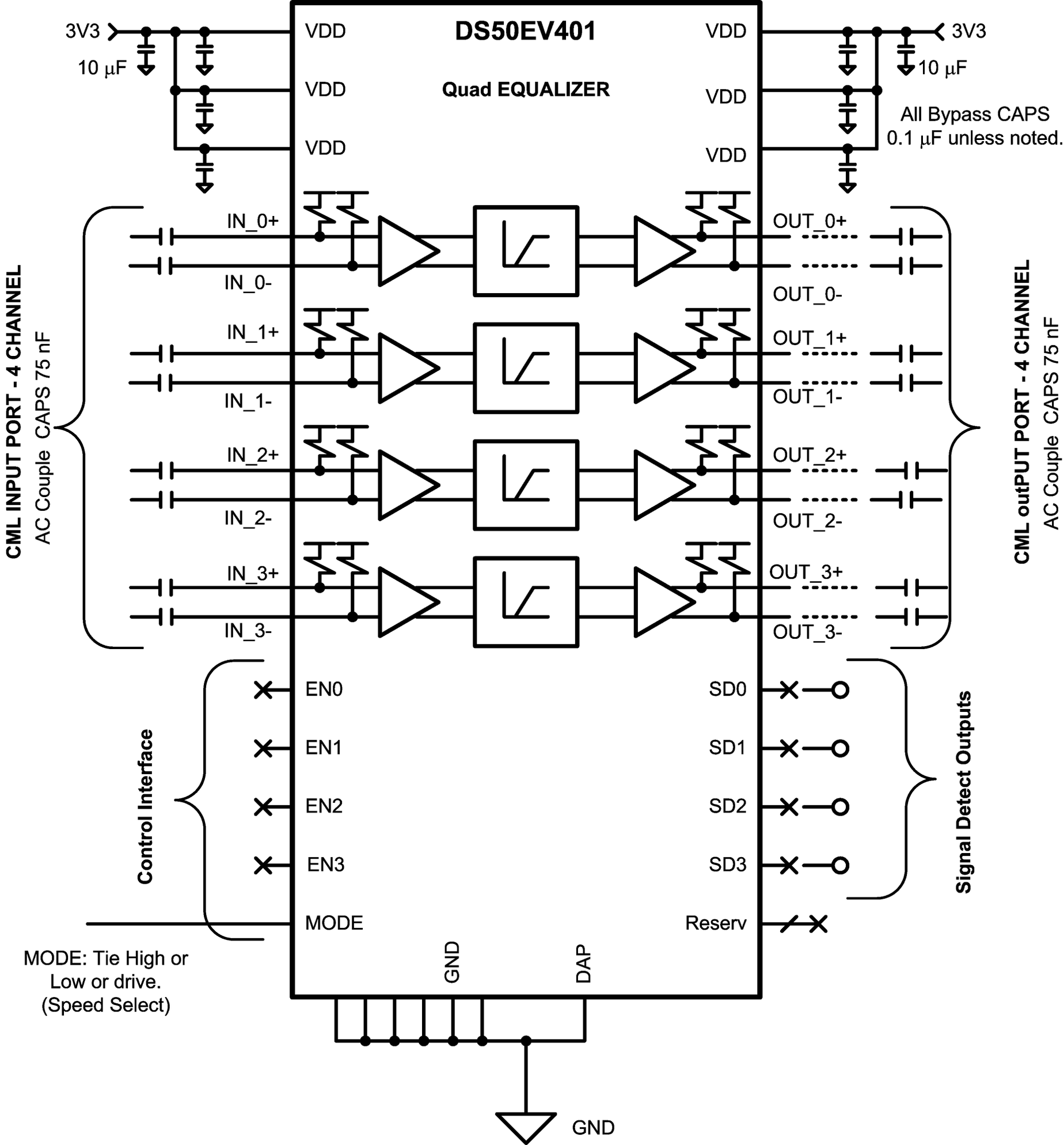
DS50EV401
Quad EQUALIZER
3V3
10 µF
VDD
VDD
VDD
VDD
VDD
VDD
3V3
10 µF
All Bypass CAPS
0.1 µF unless noted.
CML INPUT PORT - 4 CHANNEL
AC Couple CAPS 75 nF
IN_0+
IN_0-
IN_1+
IN_1-
IN_2+
IN_2-
IN_3+
IN_3-
OUT_0+
OUT_0-
OUT_1+
OUT_1-
OUT_2+
OUT_2-
OUT_3+
OUT_3-
CML outPUT PORT - 4 CHANNEL
AC Couple CAPS 75 nF
Control Interface
EN0
EN1
EN2
EN3
MODE
SD0
SD1
SD2
SD3
Reserv
Signal Detect Outputs
MODE: Tie High or
Low or drive.
(Speed Select)
GND
DAP
GND