

LM98519

10-bit 65 MSPS 6 Channel Imaging Signal Processor

General Description

The LM98519 is a fully integrated, high performance 10-Bit, 65 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative six channel architecture utilizing Correlated Double Sampling (CDS), or Sample and Hold (SH) type sampling. 1x or 2x gain settings are available in the CDS/SH input stage. Each channel has a dedicated 1x to 10x (8 bit) PGA that allows accurate gain adjustment of each channel. The Digital White Level auto calibration loop can automatically set the PGA value to achieve a selected white target level. Each channel also has a ± 4 bit coarse and ± 10 -bit fine analog offset correction DAC that allows offset correction before the sample-and-hold amplifier. These correction values can be controlled by an automated Digital Black Level correction loop. The PGA and offset DACs for each channel are programmed independently allowing unique values of gain and offset for each of the six channels. A 2-to-1 multiplexing scheme routes the signals to three 65MHz high performance ADCs. The fully differential processing channels achieve exceptional noise immunity, having a very low noise floor of -68dB. The 10-bit analog-to-digital converters have excellent dynamic performance making the LM98519 transparent in the image reproduction chain.

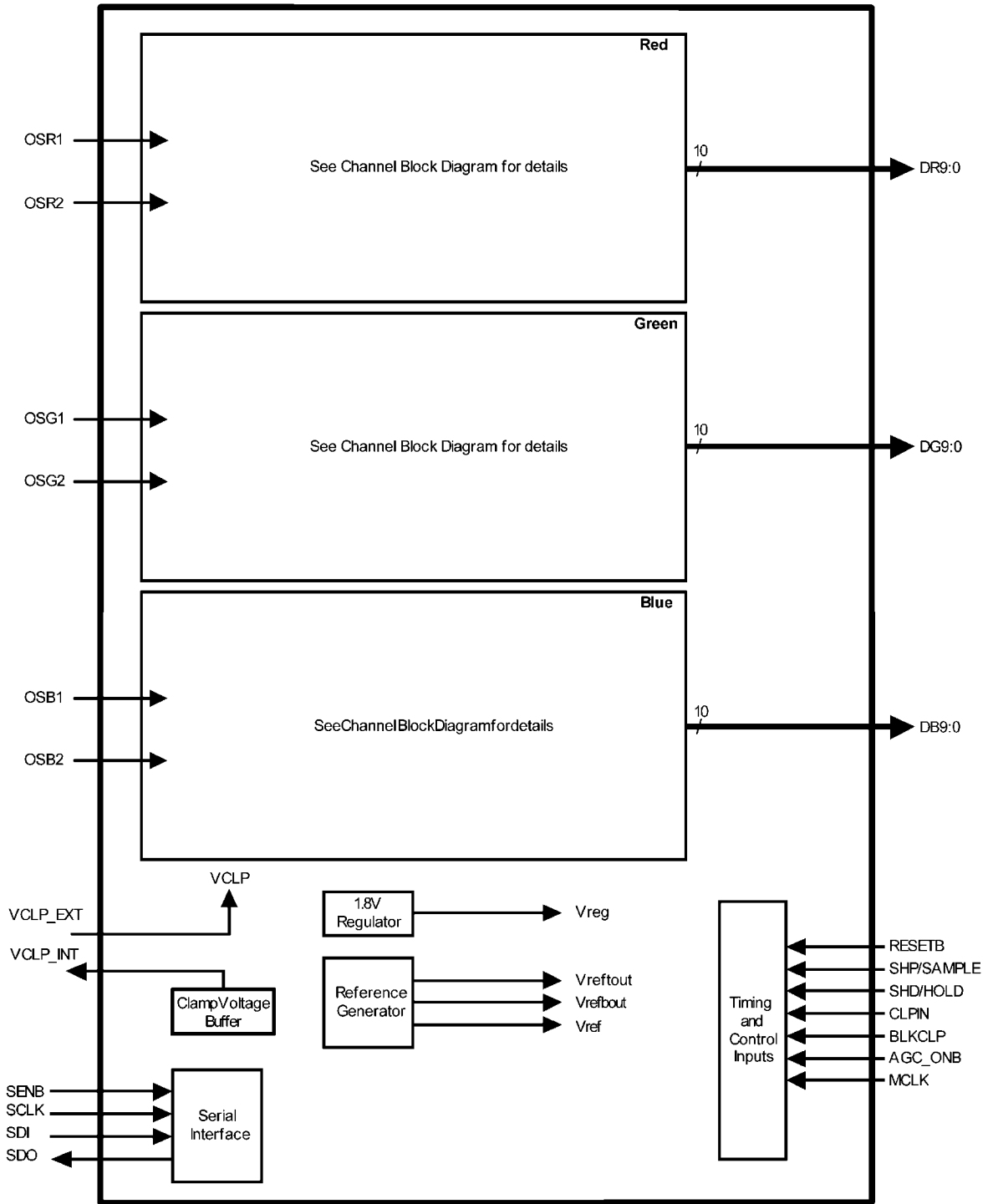
Features

- 3.3V Single Supply Operation
- CDS or S/H Processing with Negative Input Signal Polarity
- 32.5 MHz Channel Rate
- Enhanced ESD Protection on Timing and Control Pins
- Low Power CMOS Design
- 4-Wire Serial interface
- 2 Channel Symmetrical Architecture
- Independent Gain & Offset Correction for each Channel
- Digital Black Level Calibration for each Channel
- Digital White Level Calibration for each Channel
- Programmable Input Clamp

Key Specifications

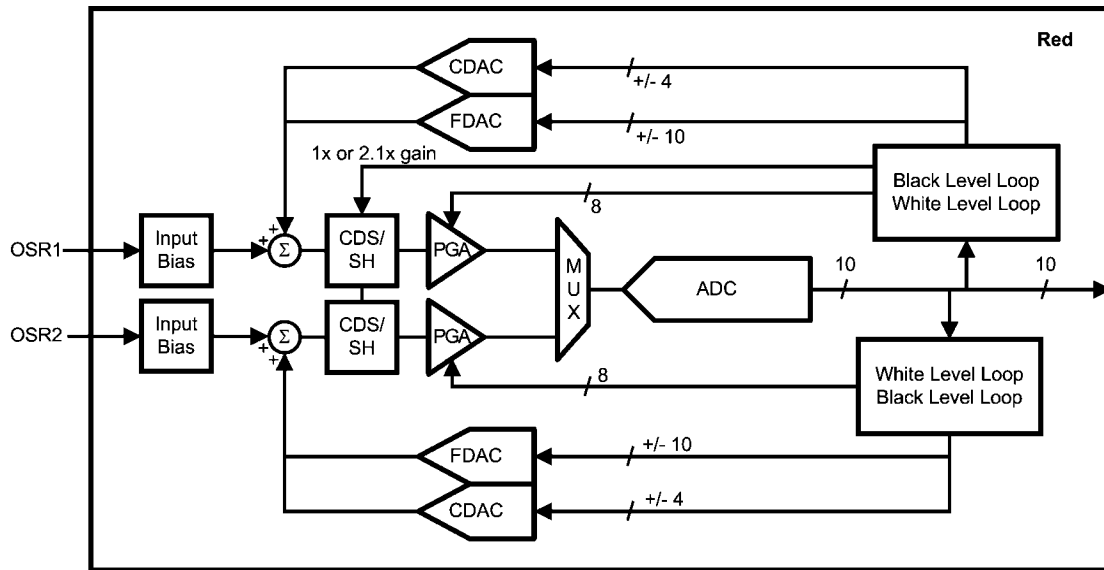
- Maximum Input Level 1.19 Vp-p (CDS gain = 1.0)
0.58 Vp-p (CDS gain = 2.1)
- Input Sample Rate 5 to 32.5 MSPS - 6ch mode
10 to 32.5 MSPS - 3ch mode
- PGA Gain Range 1x to 10x (0 to 20 dB)
- CDS/SH Gain Settings 1x or 2.1x
- Total Channel Gain 1x to 20x (0 to 26 dB)
- PGA Gain Resolution 8 bits - Analog
- ADC Resolution 10 bits
- ADC Sampling Rate 10 to 65 MSPS
- SNR 68 dB (Gain = 1x)
- Offset DAC Range ± 111 mV or ± 60 mV - FDAC
 ± 277 mV - CDAC
- Offset DAC Resolution ± 10 bits - FDAC
 ± 4 bits - CDAC
- Supply voltage 3.0V to 3.6V
- Power Dissipation 1.04 W (typical)

Chip Block Diagram



30032201

Channel Block Diagram



30032202

Ordering Information

Commercial Temperature Range	NS Package
LM98519VHB	80-Pin TQFP

Notes

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Notes

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