

Interfacing National's FPGA-Link Ser/Des with Altera Cyclone III FPGAs

National Semiconductor
Lab Report
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Introduction

The highly integrated FPGA-Link SerDes chipset (DS32ELX0421 and DS32ELX0124) enable low-cost FPGAs in a variety of high performance, high speed applications. They feature advanced on-chip signal and clock conditioning circuitry that extends data transmission reach of CAT-6 (shielded 23 AWG) cable beyond 20 meters without additional external components.

The SerDes' unique architecture is designed specifically to address the interface requirements of low cost FPGA devices like Altera's Cyclone family. The 5-bit LVDS parallel data interface simplifies board layout by reducing the number of input/output (I/O) pins and traces between the serializer, deserializer and the FPGA.

This lab report gives an overview to the LVDS interface timing using Altera Cyclone III devices and shows how to setup the ALT_LVDS megafunction for the DS32ELX0421 and DS32ELX0124 serializer and deserializer.

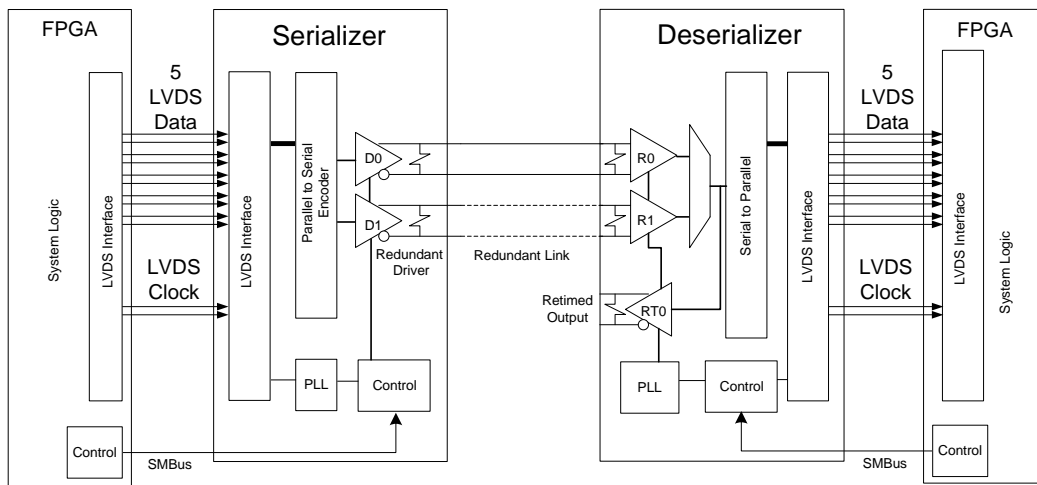


Figure 1: FPGA-Link Block Diagram

Part 1: Device Timing Requirements

Please see National Semiconductor Application Note AN-1979 and the DS32ELX0124 and DS32ELX0421 datasheets for a detailed explanation of the device timing requirements.

Part 2: FPGA Link Using ALT_LVDS Megafunction:

1. FPGA-Link compatible ALT_LVDS 20-to-5 Serializer

a. Configuration

- i. 5 channels (number of output channels)
- ii. (De)serialization factor of 4 (20/5)
- iii. Select output data rate *per channel* in Mbps (e.g. 625 Mbps for 3125 Mbps line rate)
- iv. Select input clock rate for the 20-bit data in MHz (e.g. 156.25 MHz for 3125 Mbps line rate)
- v. (Optional) Enable asynchronous reset "pll_areset" input port
- vi. (Optional) Enable registering of 20-bit input data
- vii. Enable tx_outclock with divide-by-2 option (which will give 312.5 MHz for 3125 Mbps line rate)
- viii. Configure phase alignment of tx_outclock relative to tx_out
- ix. (Optional) Enable "tx_locked" output port
- x. (Optional) Enable "tx_coreclock" output port

b. Notes:

- i. ALT_LVDS sends the most significant bits of the parallel data first.
- ii. Optional configuration items must be chosen to match the design requirements and architecture.

MegaWizard Plug-In Manager - ALTLVDS [page 5 of 7]

ALTLVDS

About Documentation

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General Frequency/PLL settings Transmitter settings

tx_coreclock altlvds_tx0 tx_out[4..0]

tx_in[19..0] tx_inclock pll_areset LVDS Transmitter tx_outclock tx_locked tx_coreclock

5 channels, x4
156.25 MHz
O/P data rate=625.00
Core Clk Freq=156.25
Outclk Freq = 312.50

Cyclone III

Resource Usage
1 cycloneiii_pll + 6 IO + 1 lut + 50 reg

Transmitter outclock

Use 'tx_outclock' output port

What is the outclock divide factor (B)? 2

Specify phase alignment of 'tx_outclock' with respect to 'tx_out'

What is the phase alignment of 'tx_outclock' with respect to 'tx_out' (in degrees)? 0.00

Phase shift at PLL is 0

Use 'tx_locked' output port

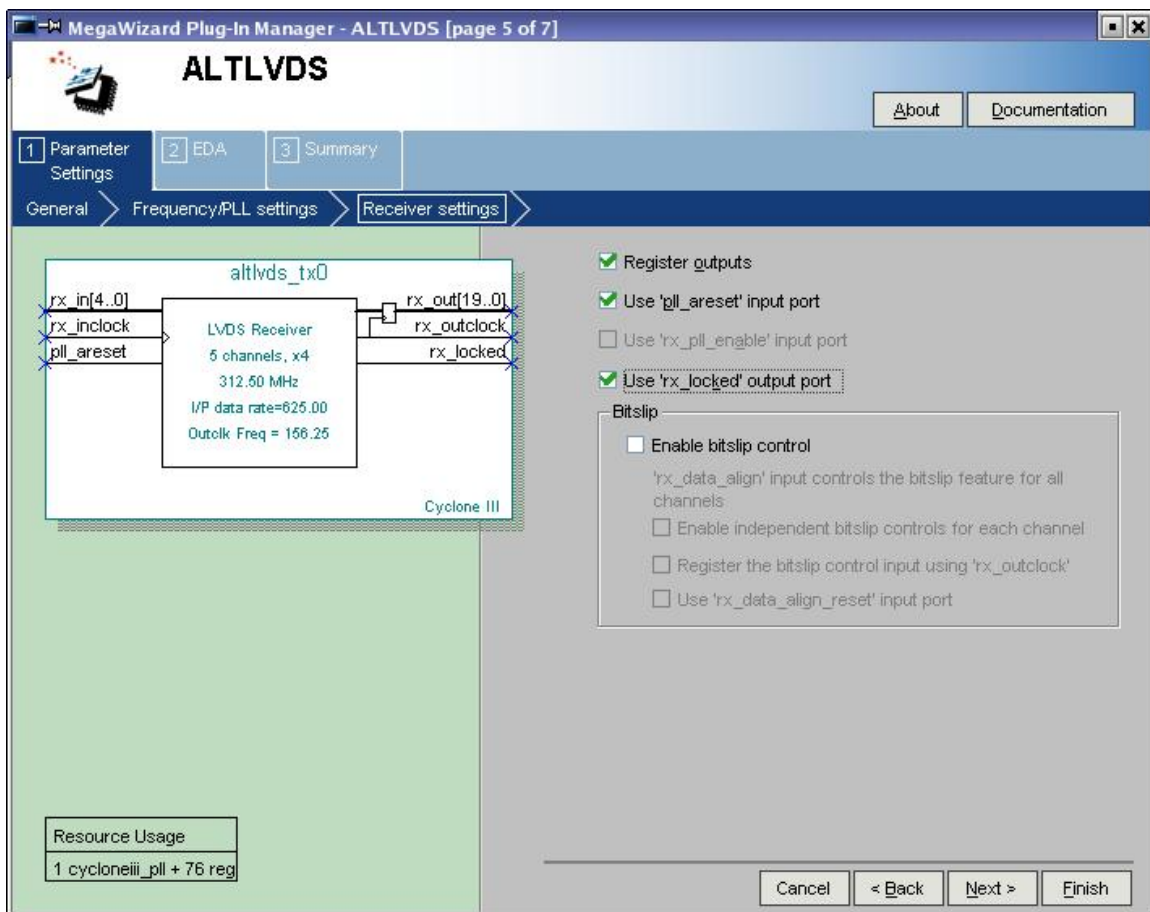
Use 'tx_coreclock' output port

What is the clock resource used for 'tx_coreclock'? Auto selection

Cancel < Back Next > Finish

2. FPGA-Link compatible ALT_LVDS 5-to-20 Deserializer

- a. Configuration
 - i. 5 channels (number of input channels)
 - ii. Deserialization factor of 4 (5×4)
 - iii. Select input data rate *per channel* in Mbps (e.g. 625 Mbps for 3125 Mbps line rate)
 - iv. Select input clock rate for the 5-bit data in MHz (e.g. 312.5 MHz for 3125 Mbps line rate since the data are clocked on both edges)
 - v. Configure phase alignment of the input data relative to the input clock.
 - vi. (Optional) Enable asynchronous reset "pll_areset" input port
 - vii. (Optional) Enable registering of 20-bit output data
 - viii. (Optional) Enable "rx_locked" output port
- b. Notes:
 - i. Need to explore deserializer parallel bit ordering, but assume it is symmetrical with the serializer parallel bit ordering.



Conclusion:

In summary this application guide give a brief overview of how to setup the DS32ELX0421 and DS32ELX0124 serializer and deserializer devices with Altera Cyclone III FPGAs.

Referenced Products:

DS32EL0421, DS32EL0124, DS32ELX0421, DS32ELX0124