

# **RSDS™ “Intra-panel” Interface Specification**

**Revision 1.0**  
**May 2003**

## **Forward**

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## 1.0 Scope

RSDS™, **R**educed **S**wing **D**ifferential **S**ignaling, is an intra-panel interface bus standard. The RSDS™ standard defines the characteristics of transmitter and receiver along with the protocol for a chip-to-chip interface. The RSDS™ interface standard is intended to cover electrical characteristics and protocol of the data only. Additional Control signals that are required by the Source (Column) Driver and/or Gate (Row) Drivers are not covered in this specification, as they are unique to the specific LCD manufacturer's design.

## 2.0 Introduction

The RSDS™ bus provides many benefits to the applications that include the following:

- Reduced bus width – enables smaller thinner column driver boards
- Lower Dynamic power dissipation – extends system run time
- Low EMI generation – eliminates EMI suppression components and shielding
- High noise rejection – maintains signal image
- High throughput – enables high resolution displays

The RSDS™ interface is intend to be used in display applications with resolutions between VGA through UXGA or higher. Higher resolution support is scaleable with RSDS™ and is only limited by the RSDS™ bus bandwidth supported by the transmitter/receiver pair.

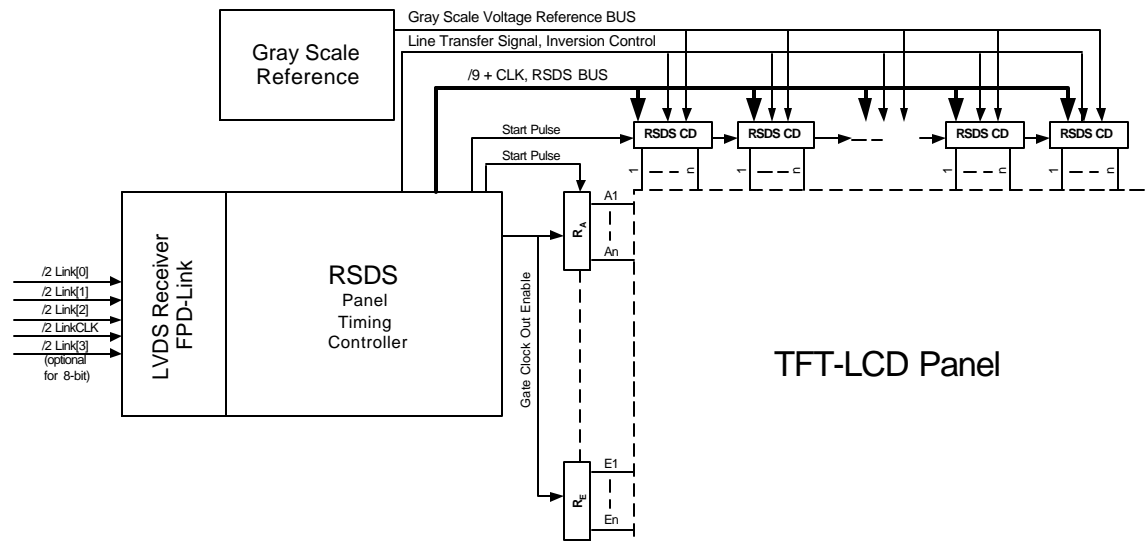
Like LVDS, RSDS™ is a differential interface with a nominal signal swing of 200mV. It retains many benefits of the industry proven LVDS interface commonly used between the host and the Flat panel display for high bandwidth and robust digital interface. Noting that the RSDS™ applications is within a sub-system, the signal swing was reduced further from LVDS to further lower power, thus the “Reduced Swing” or RS of RSDS™.

## 3.0 Definitions

FPD-Link	Flat Panel Display Link – defacto standard for embedded display digital interface
LVDS	Low Voltage Differential Signaling – see ANSI/TIA/EIA -644-A for full details
RSDS™	Reduced Swing Differential Signaling
OpenLDI	Open LVDS Display Interface
SP	Start Pulse of horizontal line of valid data to the Column or Source Driver. May also be referred to as STH (Start Horizontal), or Load.

## 4.0 System Diagram

Figure 1 depicts a typical application block diagram of the LCD Module. In this case LVDS is used as the interface between the host and the LCD Panel Module. This is either an FPD-Link or LDI Interface. The LVDS receiver function is typically integrated into the Panel Timing controller and is 3 or 4 or data pairs per color primary (Red, Green and Blue) plus clock depending upon the color depth supported(6 or 8 bits/color). The RSDS™ bus is located between the Panel Timing Controller (TCON) and the Column Drivers. There are several connection schemes allowed which are discussed in the bus configuration section (section 8). This bus is typically nine pair wide for 6 bit/color plus clock and is a multidrop bus configuration, 1 transmitter and multiple receivers.



**Figure 1: Block Diagram of the LCD Module with Discrete Timing Controller**

## 5.0 Electrical Specifications

A typical RSDS™ interface circuit is shown in figure 2. The circuit contains three parts: a transmitter (Tx), receivers (Rx) and a balanced interconnecting medium with a termination. The Tx and Rx design characteristics are defined in sections 5.1, 5.2, table 1 and 2.

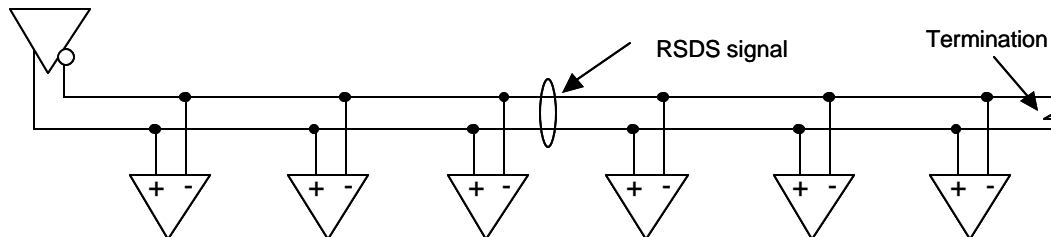


Figure 2: RSDSä Interface

### 5.1 RSDSä Transmitter Characteristics

The driver output consists of two complimentary outputs that are terminated at the end of the Data Bus (Figure 3 and 4). A differential voltage is generated from two single-ended outputs of the transmitter. As in LVDS, the single-ended outputs alternate between sourcing and sinking of a constant current. The differential voltage is the product of this constant current across the terminating resistance  $R_T$ .

Due to a wide variation in the characteristic impedance of the transmission media ( $25\Omega$  to  $100\Omega$ ), it is recommended that the transmitter be designed with the capability to drive such loads with a minimal amount of signal integrity artifacts such as reflection, ringing, overshoot, undershoot.

In another cases, the resultant  $R_T$  is approximately  $50\Omega$ . The  $50\Omega$  is a result of the double/parallel termination scheme used in one of the more popular RSDS™ bus architecture (refer to section 8). For cases such as this, some means of adjusting the output current need to be provided in the transmitter such that the output voltage swing can be increased for inter-operability with the minimum RSDS™ receiver threshold (Figure 5).

The following specifications apply to both clock and data pairs over a specified range of termination resistance values and operating voltages.

Parameter	Definition	Conditions / Note	MIN	TYP	MAX	Units
$V_{OD}$	Differential Output Voltage (Figure 4)	$R_L = 100 \text{ Ohm}$	100	200	600	mV
$V_{OS}$	Offset Voltage (Figure 3)		0.5	1.2	1.5	V
$I_{RSDS}$	RSDS Driver Current		1	2	6	mA
$T_R/T_F$	Transition Time: Rise, & Fall (Figure 6)	20% to 80%, $V_{OD} = 200 \text{ mV}$ , $CL \cong 5 \text{ pF}$		500		ps
	RSDS Clock Duty Cycle		45	50	55	%

Table 1 – Electrical Specifications of RSDSä transmitters

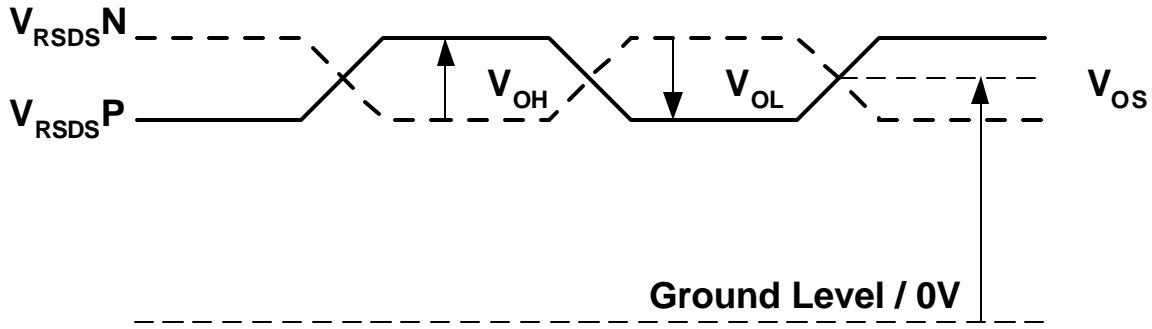


Figure 3: RSDS Transmitter Output

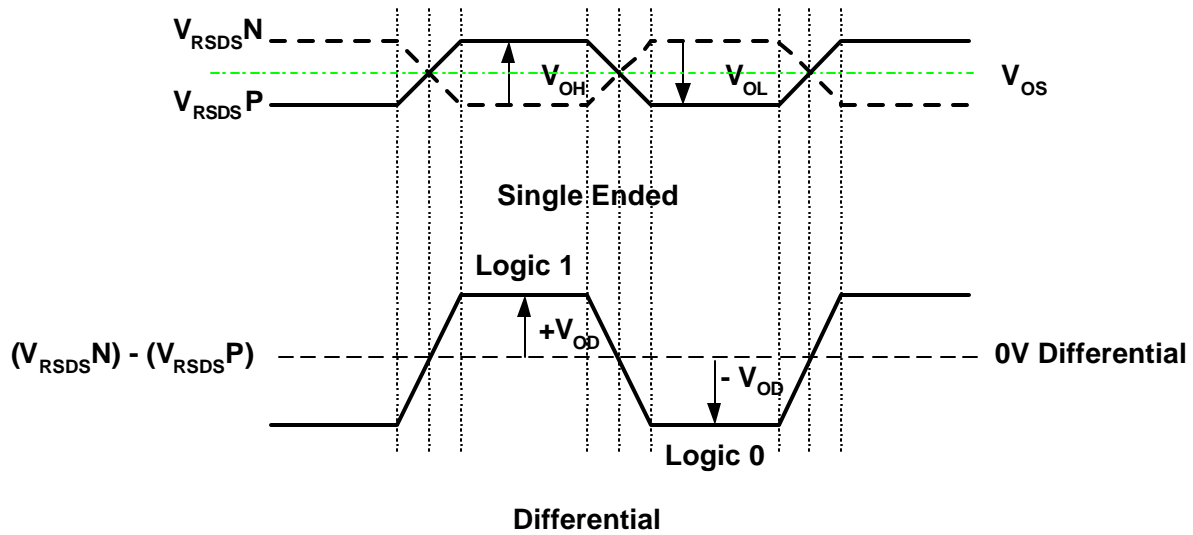


Figure 4: RSDS Transmitter Output, Single Ended Vs. Differential

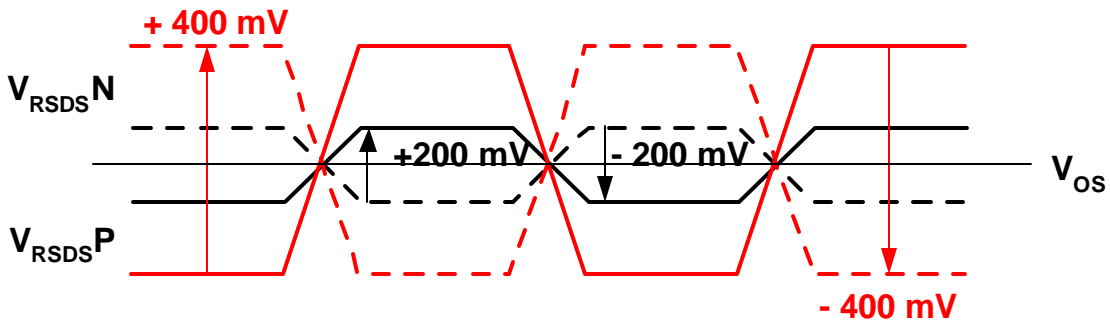


Figure 5: RSDS Transmitter Output Swing Level Control

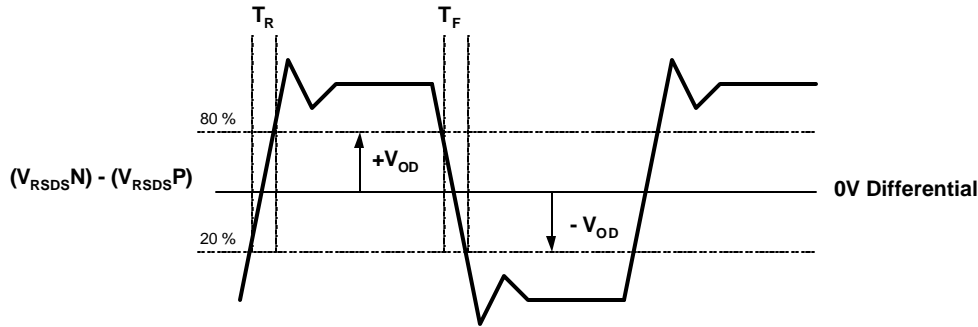


Figure 6: RSDS Transmitter Fall/Rise Time

## 5.2 RSDS Receiver Characteristics

At a minimum, the RSDS™ receiver for both the clock and data shall adhere to the following recommended requirements over specified ranges of operation.

Parameter	Definition	Conditions / Note	MIN	TYP	MAX	Units
$V_{TH}$	Differential Threshold				+/-100	mV
$V_{CM}$	Input Common Mode Voltage		0.3		1.5	V
$I_L$	RSDS Rx Input Leakage		-10		10	$\mu A$

Table 2 – Electrical Specifications of RSDS transmitters

## 6.0 Timing Characteristics: Clock/SP/Data Relationship

The relationship between clock and data is shown in figure 7. Note that RSDS™ interface uses both edges (rise and falling) of the clock to strobe data.

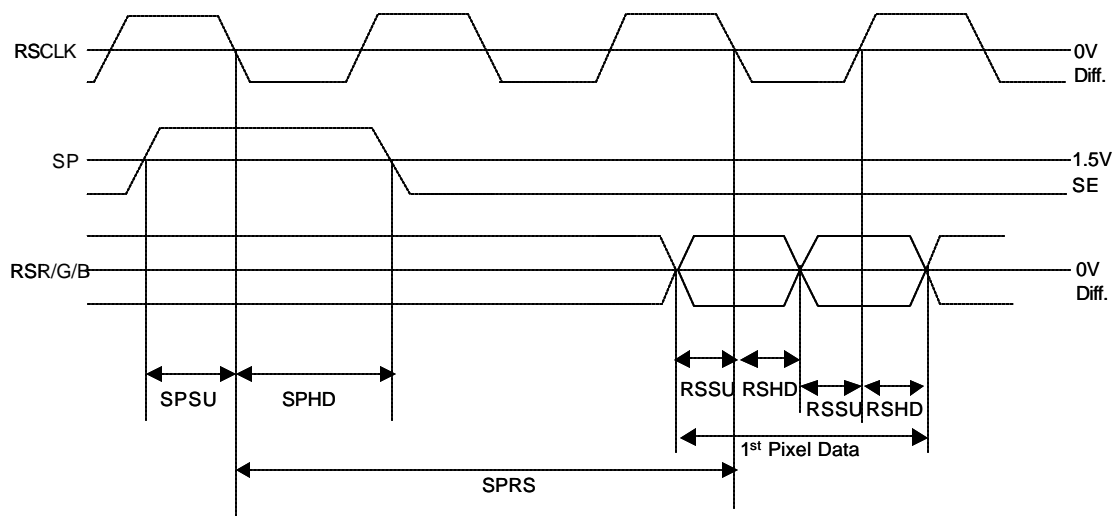


Figure 7: RSDS Clock – SP – RSDS RGB Data Relationships

## 6.1 SP/Data Relationship

The start pulse (SP) is two clock cycles (or 5 clock edges) prior to the start of valid data. The SP (Start Pulse) is a single-ended (SE) signal with a logic threshold of 1.5 V for 3.3 Volt systems. The SP signal is a latch pulse indicating the start of valid data transmission to the first Column driver (RSDS™ Receiver) within a RSDS bus.

**SPSU** Start Pulse signal set up time

**SPHD** Start Pulse signal hold time

**SPRS** Start Pulse to Data Valid Delay

**RSSU** RSDS™ Data set up time

**RSHD** RSDS™ Data hold time

Parameter	Definition	Conditions / Note	MIN	TYP	MAX	Units
<b>SPSU</b>	SP Set-up Time			0.5		CLK
<b>SPHD</b>	SP Hold Time			0.5		CLK
<b>SPRS</b>	SP to Data Valid Delay			2		CLK

Table 3 – SP and RSDSä Clock/Data Relationship

## 6.2 RSDSä Clock/Data Timing Characteristics

Due to the open nature of the RSDS™ standard, set-up and hold time requirements for RSDS™ receivers can vary from one manufacturer to another. As an example, National Semiconductor's Column Drivers typically require 2ns / 0ns at 85 MHz for set-up/hold time. However, other manufacturers require 2ns/2ns of set-up/hold time. Therefore to assure inter-operability with the various receiver AC characteristics, the RSDS™ Transmitter should be designed with the capability for set-up/hold time adjustments. An example of a possible skew control architecture is provided in Figure 8.

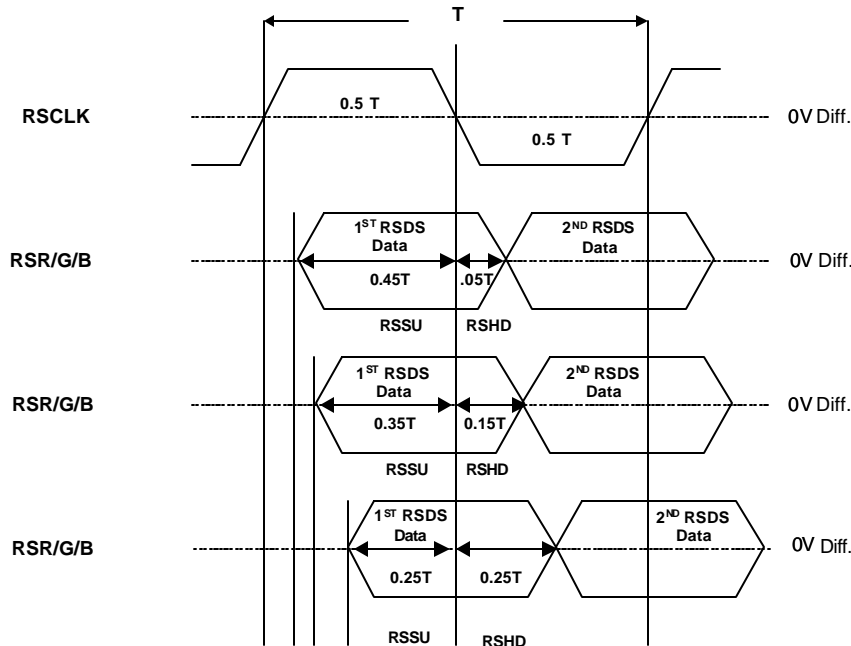


Figure 8: RSDSä Skew – Step-Up/Hold Time Control

## 7 – Bit Mapping

Due to the scaleable nature of RSDS™ system, RSDS™ can support from 6 to 10 bits per RGB color mapping. 6 bit for primarily Notebook PC and value line Monitor Applications. 8 bit for Premium line LCD Monitor Applications and 10 bit for LCD TV Applications.

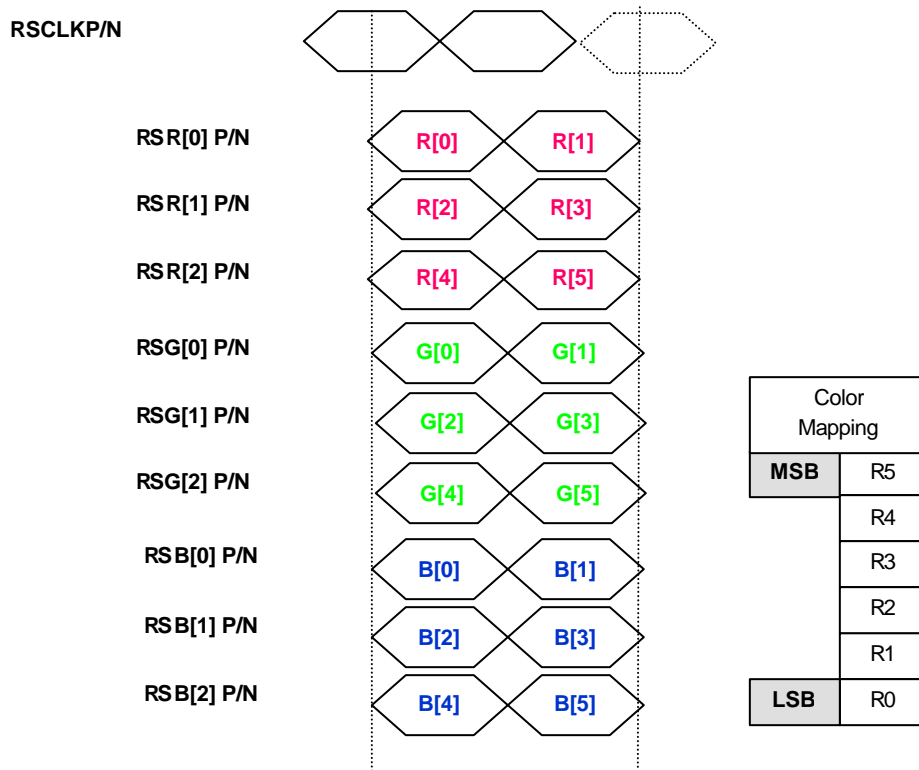
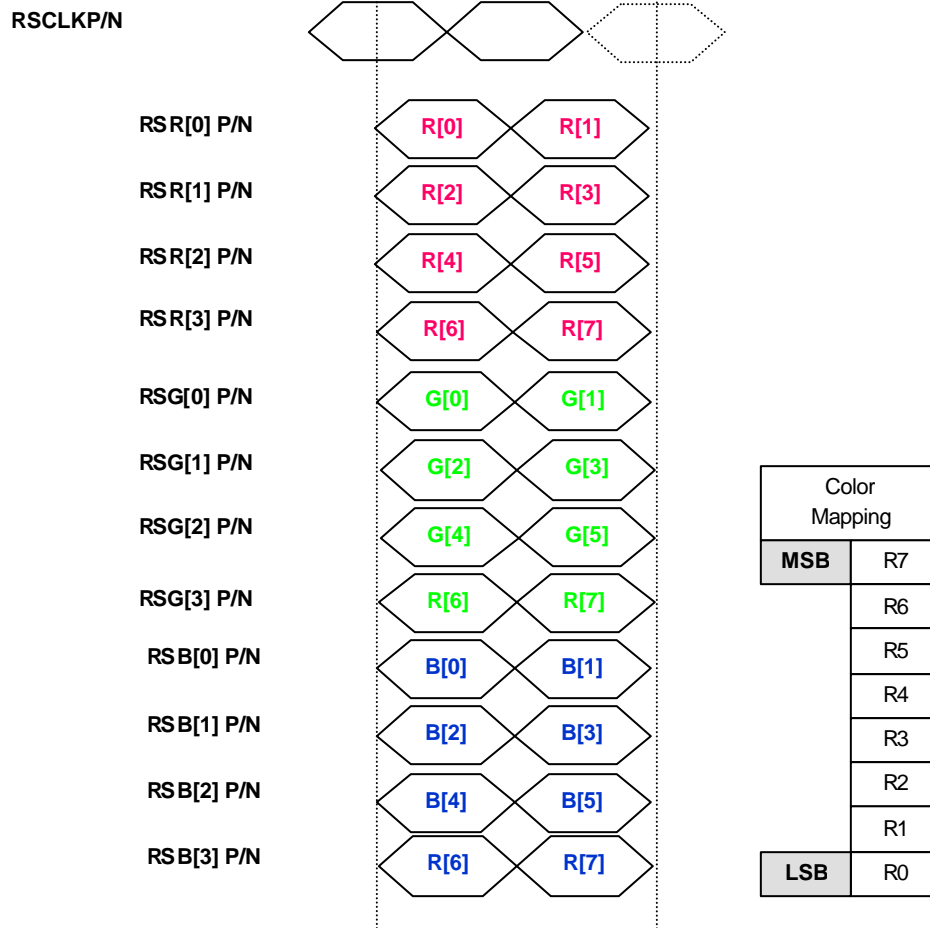


Figure 9: RSDS 6 Bit Color Mapping



**Figure 10: RSDSä 8 Bit Color Mapping**



**Figure 11: RSDS 10 Bit Color Mapping**

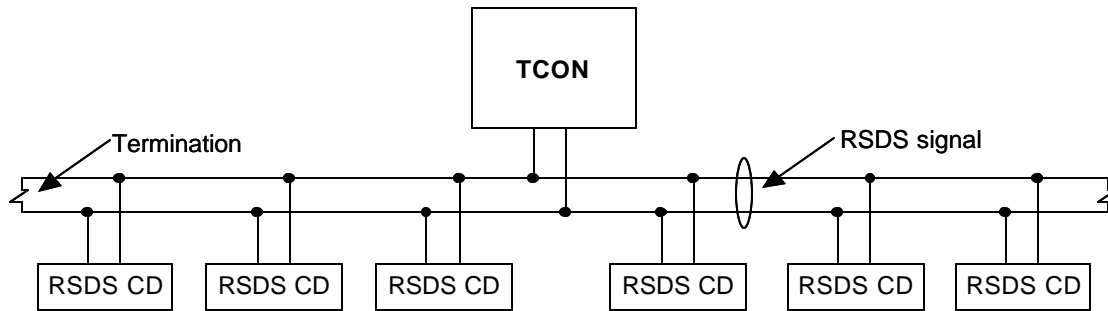
Note that the Bit Mapping shown in figures 9, 10 and 11 are recommended to allow direct inter-operation between the current generation of transmitters and receivers. Other bit mappings may exist; therefore a careful review of TCON/Transmitter and Column Driver/Receiver datasheets is recommended to ensure that they inter-operate.

## 8 – Bus Configurations

The RSDS™ is a versatile interface that may be configured differently depending upon the end application requirements. Considerations include the location of the TCON, the resolution of the panel, and the color depth for example. The common implementations include the following bus types:

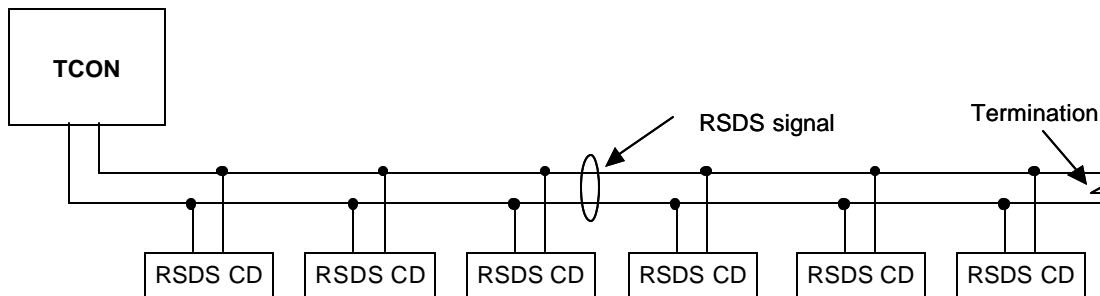
- Type 1 – Multidrop bus with double terminations
- Type 2 – Multidrop bus with single end termination
- Type 3 – Double multidrop bus with single termination

In a Type 1 configuration the source (TCON) is located in the center of the bus via a short stub. The bus is terminated at both ends with a nominal termination of 100 Ohms. The interconnecting media is a balanced coupled pair with ideal (unloaded) differential impedance of 100 Ohms. However in actual applications the bus impedance can be much lower than ideal due to the additional loading or PCB characteristics. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported. See figure 12. In this application the RSDS™ driver will see a DC load of 50 Ohms instead of 100 Ohms. For this case, output drive of the RSDS™ driver must be adjusted to comply with the VOD specification with the 50-Ohm load presented by the the Type 1 configuration.



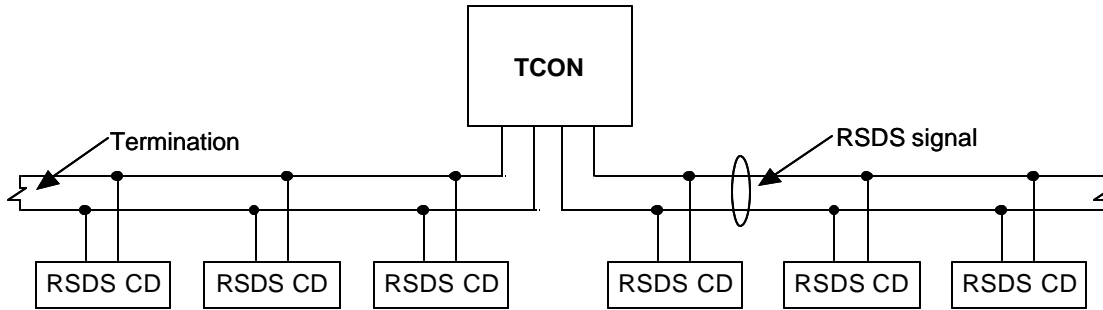
**Figure 12: Type 1 Bus Configuration**

In a Type 2 configuration the source (TCON) is located at one end of the bus. The bus is terminated at the far end with a nominal termination of 100 Ohms. The interconnecting media is a balanced coupled pair with nominal (unloaded) differential impedance of 100 Ohms. The bus may be a single or dual bus depending upon the panel's resolution. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported for a single bus. See figure 13.



**Figure 13: Type 2 Bus Configuration**

In a Type 3 configuration the source (TCON) is located in the center of the application. There are two buses out of the TCON that run to the right and left respectively. Each bus is terminated at the far end with a nominal termination of 100 Ohms. The interconnecting media is a balanced coupled pair with nominal (unloaded) differential impedance of 100 Ohms. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported for a single bus for each bus. Note that the connection of the TCON to the main line is not a stub in this configuration, but rather is part of the main line. This helps to improve signal quality. See figure 14.



**Figure 14: Type 3 Bus Configuration**

Note that in figures 12, 13 and 14, the complete bus is not illustrated; only a single RSDS™ pair is shown. The number of column drivers on the bus is also application specific and depends upon the panel resolution and also if a single or dual bus is used.

**Revision History**

Revision	Date	Update
0.95	May 25, 2001	Initial Release – J. Goldie/A. Lee
1.00	May, 2003	Extensively revised – A. Lee

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