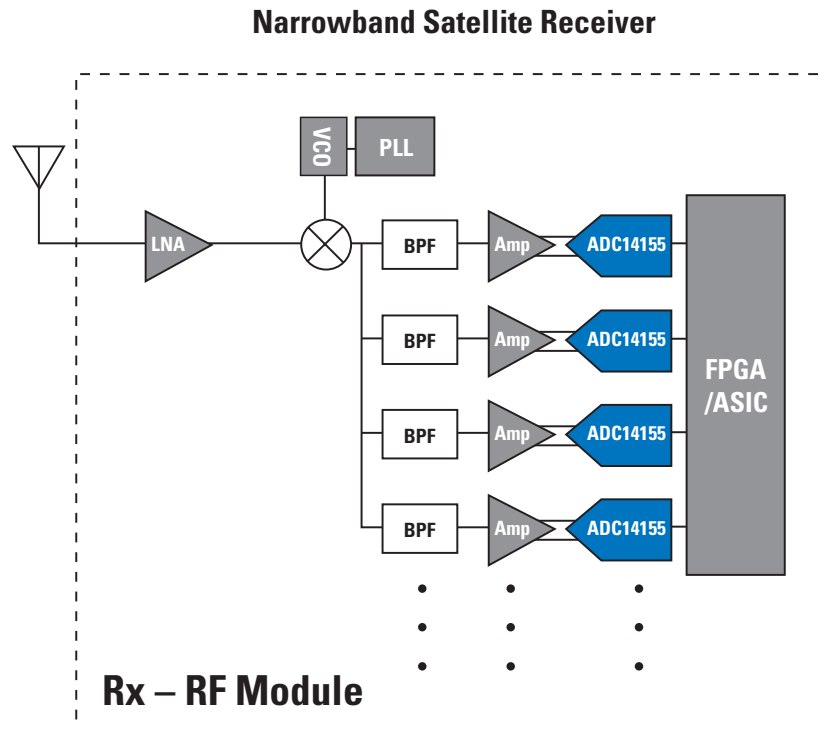


1.1 GHz Bandwidth ADC Enables High IF-Sampling for Space-Based Narrowband Communications Applications



Introduction

The ADC14155 is a high-performance CMOS Analog-to-Digital Converter (ADC) capable of converting analog input signals into 14-bit digital words at rates up to 155 Mega Samples per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.1 GHz. The ADC14155 operates from 3.3V analog supply and +1.8V for the digital output interface and consumes 967 mW of power at 155 MSPS. A power-down feature reduces the power consumption to 5 mW with the clock input disabled, while still allowing fast wake-up time to full operation.

The differential inputs provide a full scale differential input swing equal to 2 times the reference voltage. A stable 1.0V internal voltage reference is provided, or the ADC14155 can be operated with an external reference. The ADC14155 can be configured for operation with either single-ended or differential clock input.

Clock mode (differential versus single ended) and output data format (offset binary versus 2's complement) are pin-selectable. A duty cycle stabilizer maintains performance over a wide range of clock duty cycles. The ADC14155 is available in a 48-lead thermally enhanced multi-layer ceramic quad package and operates over the military temperature range of -55°C to +125°C.

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Benefits

The high-bandwidth design of the ADC14155 provides excellent SNR and SFDR performance at very high input frequencies. For instance, at 300 MHz, the SNR is 67 dB and SFDR is 80 dB. This performance allows the system designer to adopt a high IF sampling design where digitization is done at first IF. This eliminates an IF stage thereby lowering component count and power consumption while allowing flexibility in frequency planning. The dynamic performance makes this product desirable in multi-carrier architectures where several signals are digitized by a single ADC which translates to consolidation of signal paths while reducing board size, power consumption, and improving system reliability.

Features

- 1.1 GHz full power bandwidth
- Internal sample-and-hold circuit
- Low-power consumption
- Power-down mode
- Internal precision 1.0V reference
- Single-ended or differential clock modes
- Data ready output clock
- Clock duty cycle stabilizer
- 48-lead ceramic quad flat package
- Dual +3.3V and +1.8V supply operation
- Radiation performance
 - TID of 100 krad(Si)
 - Single event latchup > 120 MeV

Applications

- High IF sampling receivers
- Power amplifier linearization
- Multi-carrier, multi-mode receivers
- Test and measurement equipment
- Communications instrumentation
- Radar systems

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