

# PLL Fundamentals

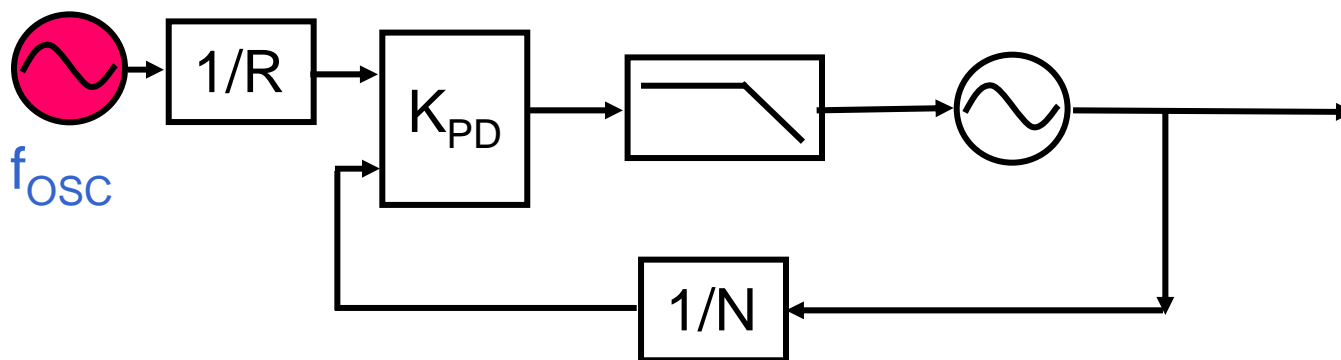
Part 1: PLL Building Blocks

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# Overview

- Oscillators
  - Crystal Oscillators
  - High Frequency Oscillators
  - Voltage Controlled Oscillators (VCO)
  - Silicon Voltage Controlled Oscillators
  - Oscillator Phase Noise
- Other PLL Building Blocks
  - Counters
  - Phase Detector/Charge Pump
  - Loop Filter

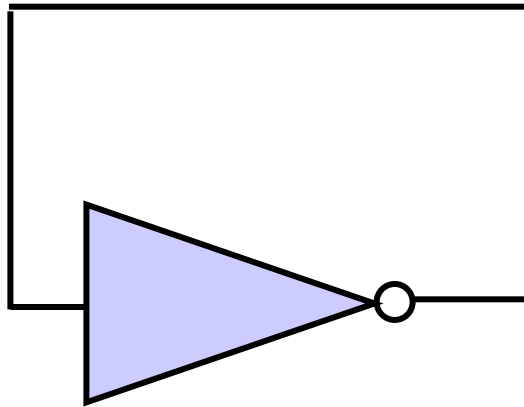
# Reference Oscillator



- Typically a fixed frequency of operation =  $f_{osc}$
- Can come in many forms
  - Crystal
  - Crystal Oscillator (XO)
  - Temperature Compensated Crystal Oscillator (TCXO)
  - Oven Controlled Crystal Oscillator (OCXO)
  - Output from another device
  - Recovered clock
  - DDS Signal



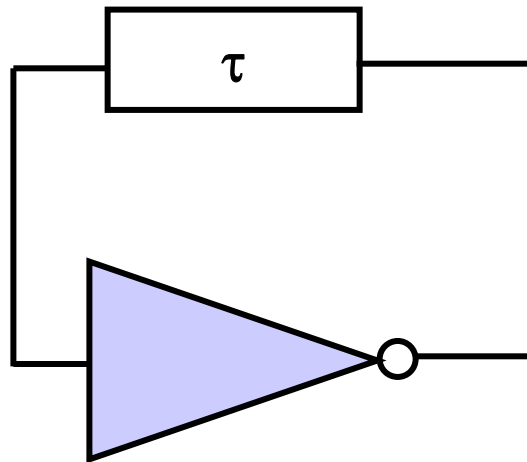
# The Traditional Oscillator



- **Output of Inverter is fed back to the input**
- **Frequency of oscillation is determined by delay of inverter**

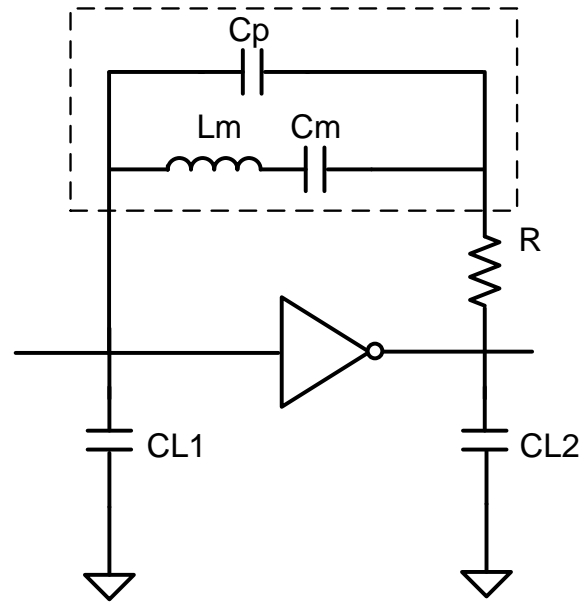


# The Traditional Oscillator



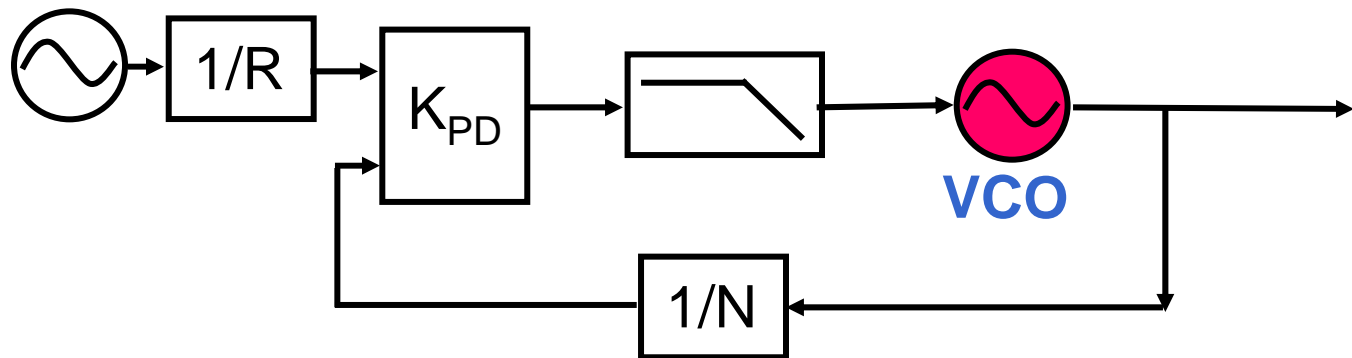
- Delay of  $\tau$  can be added in feedback path to set the frequency
  - $f = 1/\tau$
- A filter can also be added for a sine wave. Note that it is impossible to filter without delay, so a filter and a delay are related.

# Typical Crystal Oscillator



- **Crystal**
  - **$L_m$  (Motional Inductance)**
  - **$C_m$  (Motional Capacitance)**
  - **$C_p$  (Parallel Capacitance)**

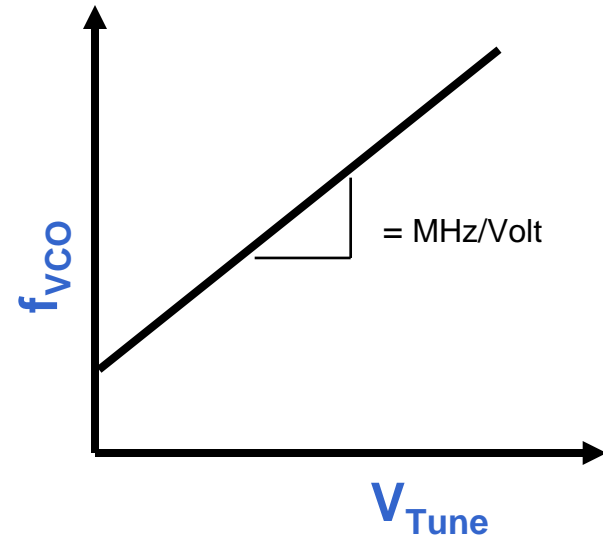
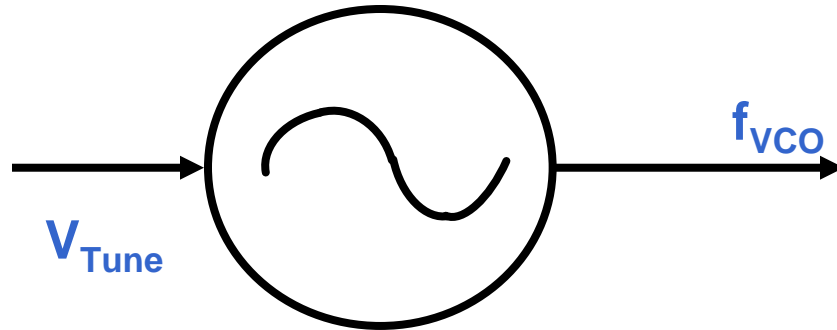
# VCO (Voltage Controlled Oscillator)



- **The VCO (Voltage Controlled Oscillator)**
  - Converts voltage to frequency
  - Generates frequencies over restricted frequency range
  - Frequency drifts considerably over temperature, voltage and process
  - Typically Much higher frequency than the reference oscillator



# VCO Frequency Tuning



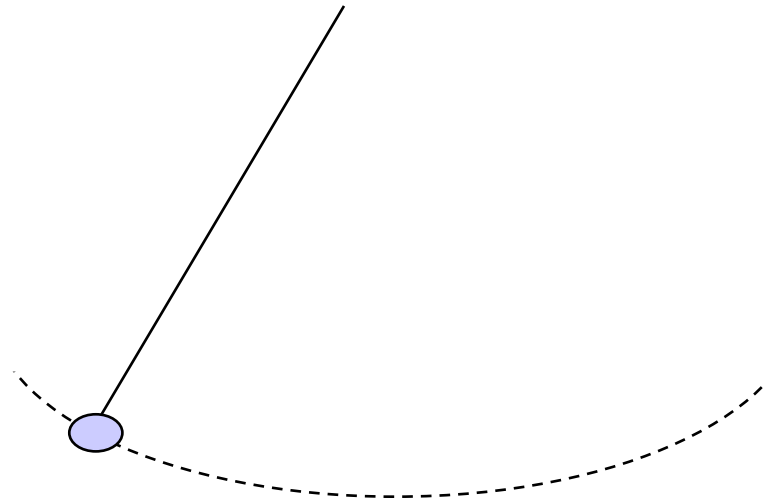
- **VCO Figures of Merit**

- Tuning Range
- Output Power
- Tuning Sensitivity ( $K_{VCO}$  in MHz/Volt)
- Tuning Linearity (Want  $K_{VCO}$  constant)
- Pushing (Frequency shift over supply voltage)
- Pulling (Frequency shift over load)
- Harmonics (Undesired Multiples of intended frequency)
- Power Consumption
- Size
- Phase Noise

# Understanding How VCOs Work

- **Crystals and VCOs are Not the Same**
  - Crystals are typically limited to lower frequencies (<100 MHz)
  - Crystals typically have a frequency range that is too narrow for most applications
- **Hard to Relate VCO Circuits to Crystal Circuits**
  - Higher frequency oscillators like VCOs often contain transistors and MOS devices that deal with currents, not voltages
  - Trying to relate a VCO schematic to this traditional oscillator model takes a lot of imagination.

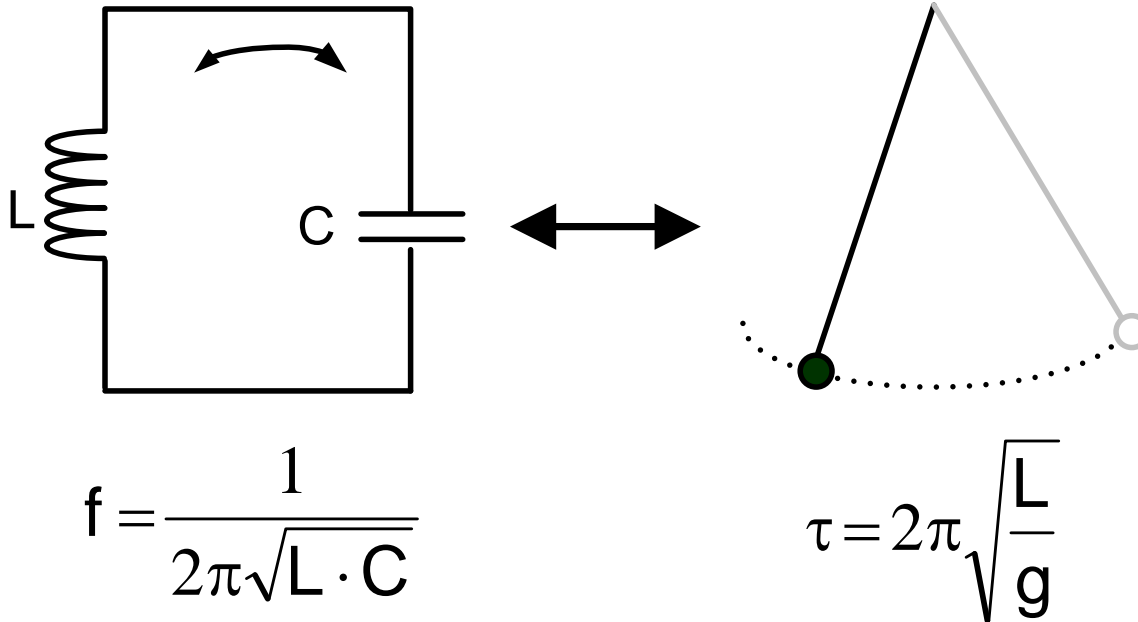
# A Better Way to Think of a VCO



- Neglecting the Impacts of Friction, the pendulum conserves energy. It just converts it between potential and kinetic energy
- In the real world, there is friction, so a small stimulus needs to be applied to keep the circuit going.

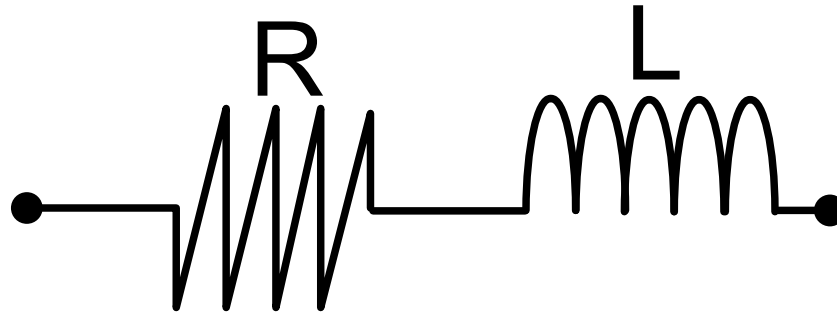


# The Tank Circuit



- Tank circuit can be viewed as an electronic spring.
  - When voltage across the capacitor is maximum, current in the inductor is minimum, and vice versa
- Assuming no parasitic resistances, circuit would go on forever, but wouldn't that be nice?

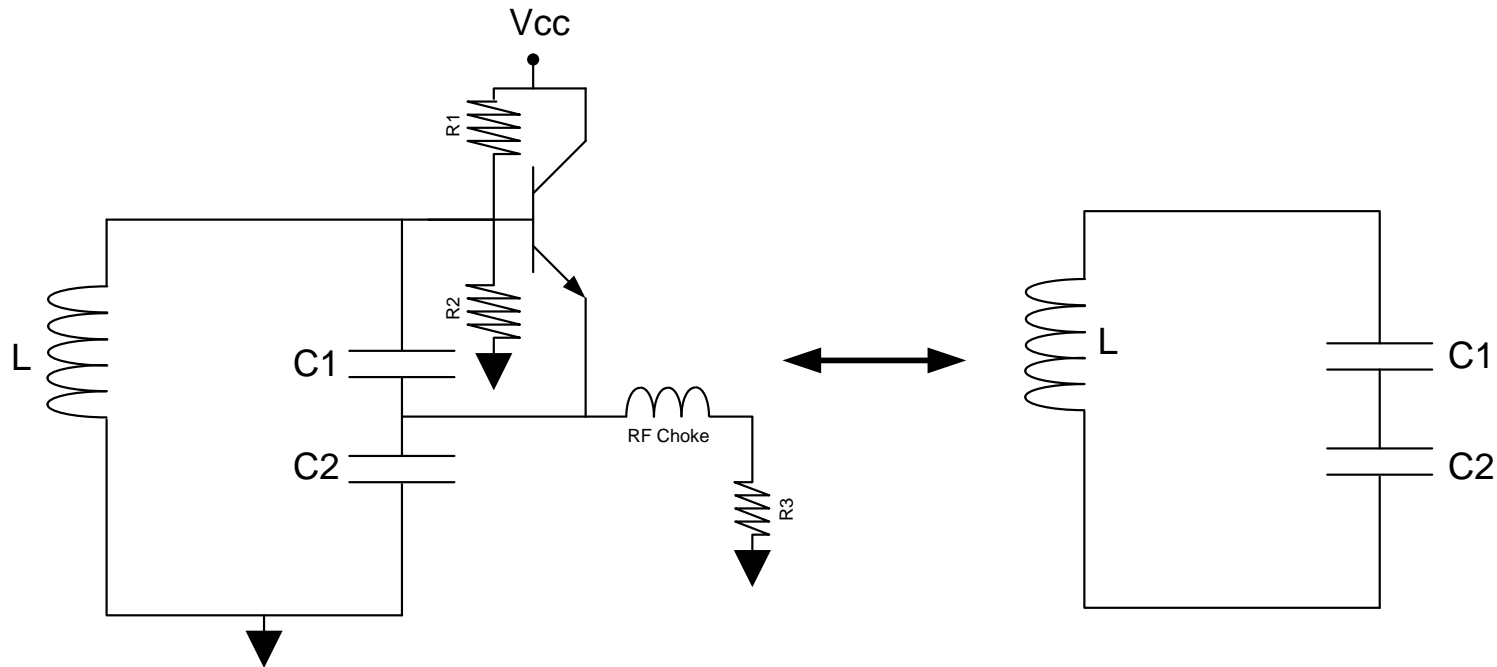
# The Real World Inductor



$$Q_L(f) = \frac{X_L}{R_L} = \frac{2\pi \cdot f \cdot L}{R}$$

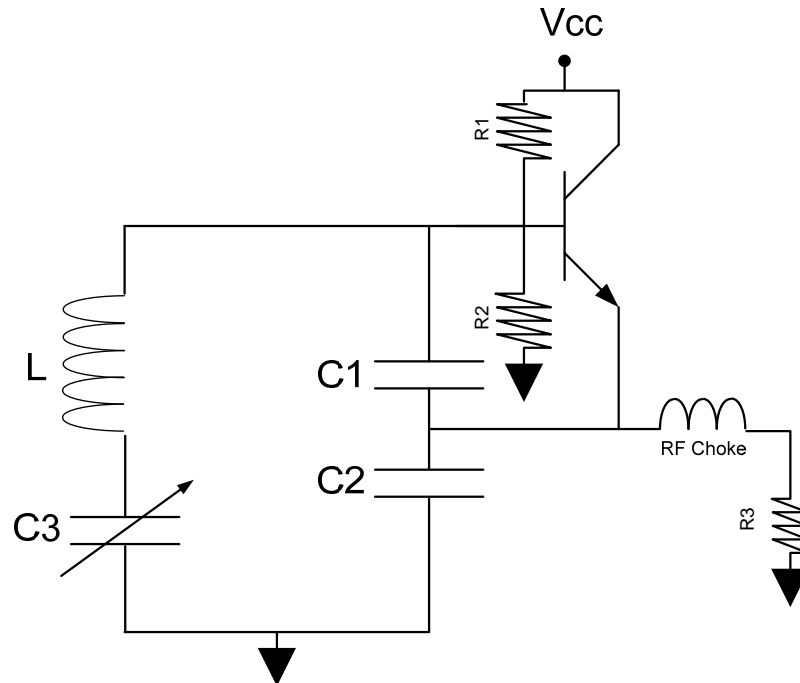
- **Q is the quality factor, measured at the frequency of interest**
- **Parasitic resistances, such as the one in the inductor cause the circuit to eventually stop oscillating.**
- **Just as with the pendulum, it is necessary to provide some stimulus to keep the circuit going.**

# Now Add the Stimulus



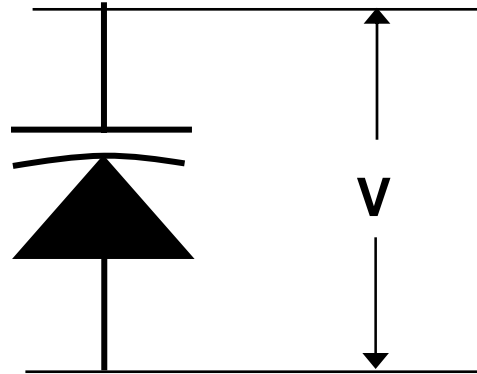
- **Amplified signal from emitter is lightly coupled into the circuit to sustain oscillation**
- **Above Circuit is Colpitts Oscillator**

# Typical Clapp (Clapp-Gouriet) Oscillator



- **Very similar to the Colpitts oscillator, except ..**
  - **Series capacitance C3 (Often adjustable), is typically added**
  - **This is better than Colpitts with a variable capacitor because changing the C3 capacitance does not change the feedback at C1 and C2.**

# The Varactor Diode

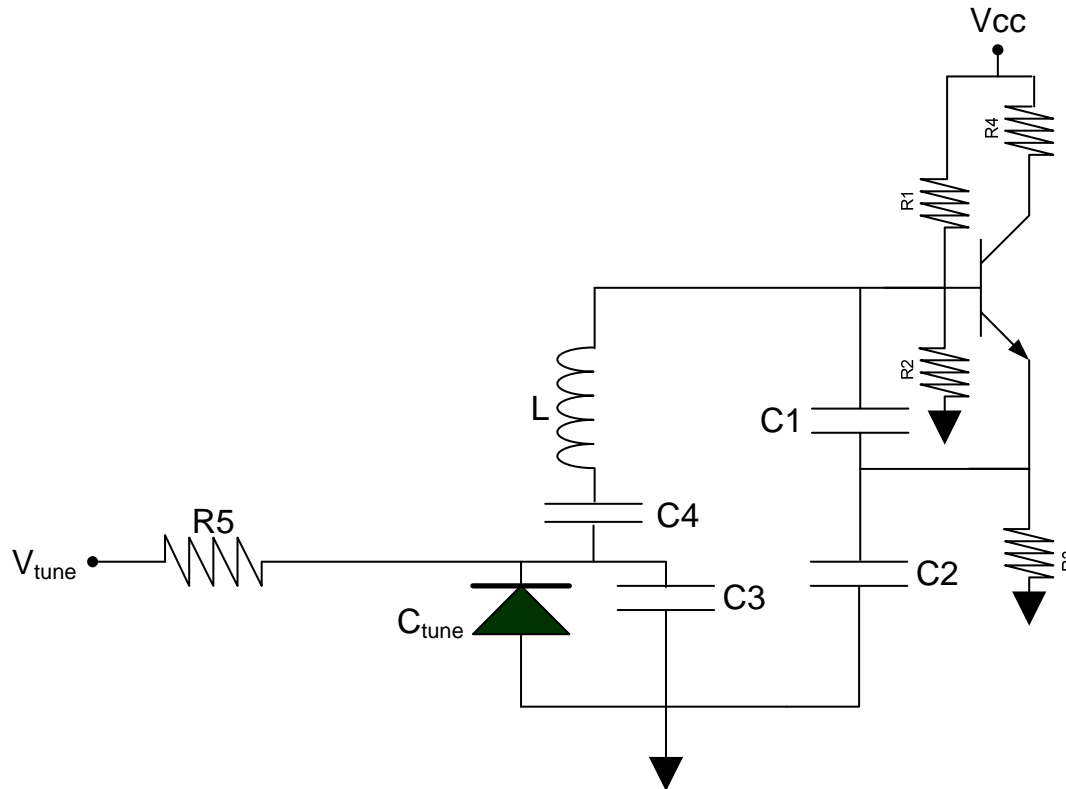


- To implement the variable capacitance for the VCO, a varactor diode is often used. As more voltage is applied to the diode, the capacitance decreases

$$C_{Varactor}(V) = \frac{C_{Varactor}(0\text{volts})}{\sqrt{\phi + V}}$$

- 15-20 pF of capacitance is typical

# Complete VCO Circuit



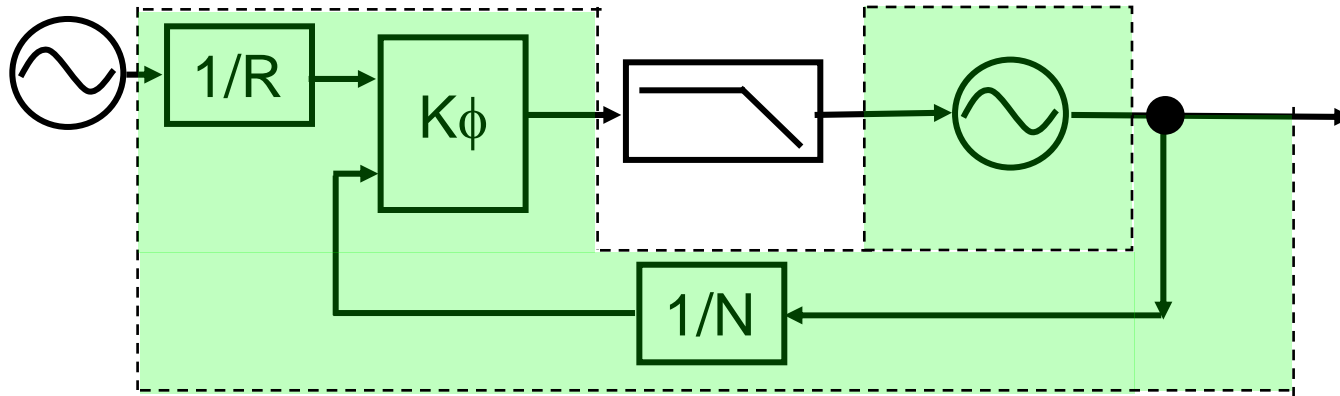
- **Varactor Diode Capacitance Adds to C3**
  - Larger C3 => better Phase Noise, but less tuning range
- **Resistor R5 isolates Tuning voltage from Loop Filter**

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- Other PLL Building Blocks
  - Counters
  - Phase Detector/Charge Pump
  - Loop Filter



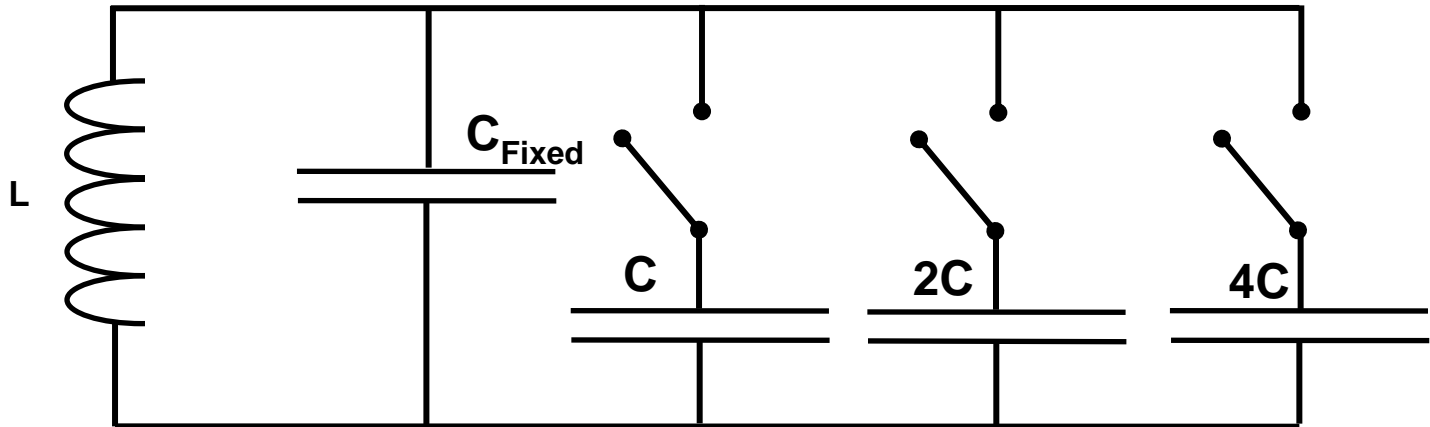
# Integrating VCOs on Silicon



- **Inductance is Typically Formed by Bond Wires**
  - VCO frequencies tend to be higher due to low inductances
  - Can also do small inductors on silicon, but they are small
  - Can allow external inductors to be added for lower frequencies
  - Often easier to generate a higher frequency and divide it down
- **Capacitance is Formed by an Internal Bank of Capacitors**
  - Frequency calibration is typically necessary



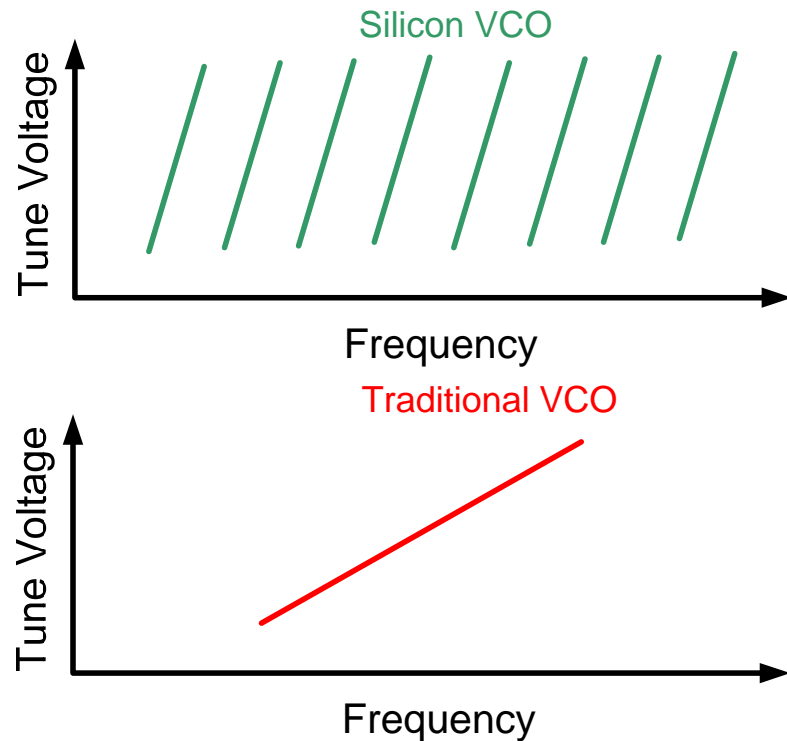
# Bank of Switched Capacitors



- Capacitors can be switched in and out to create multiple bands
  - The best phase noise and lowest tuning gain is often at the lowest frequency with all the capacitors switched in
- Logic is necessary to switch capacitors in and out to find the correct combination
  - On resistance of the switches is one source of phase noise

# Silicon VCO Tuning Range

- **VCO Range Divided into many bands**
- **These bands cover the whole frequency range and need**
- **Bands need to overlap to account for temperature drift**
- **Correct band is selected when frequency is changed**
- **This technique allows wider tuning range without sacrificing phase noise**





# Things to Watch for with Silicon VCOs

- **Temperature Drift**

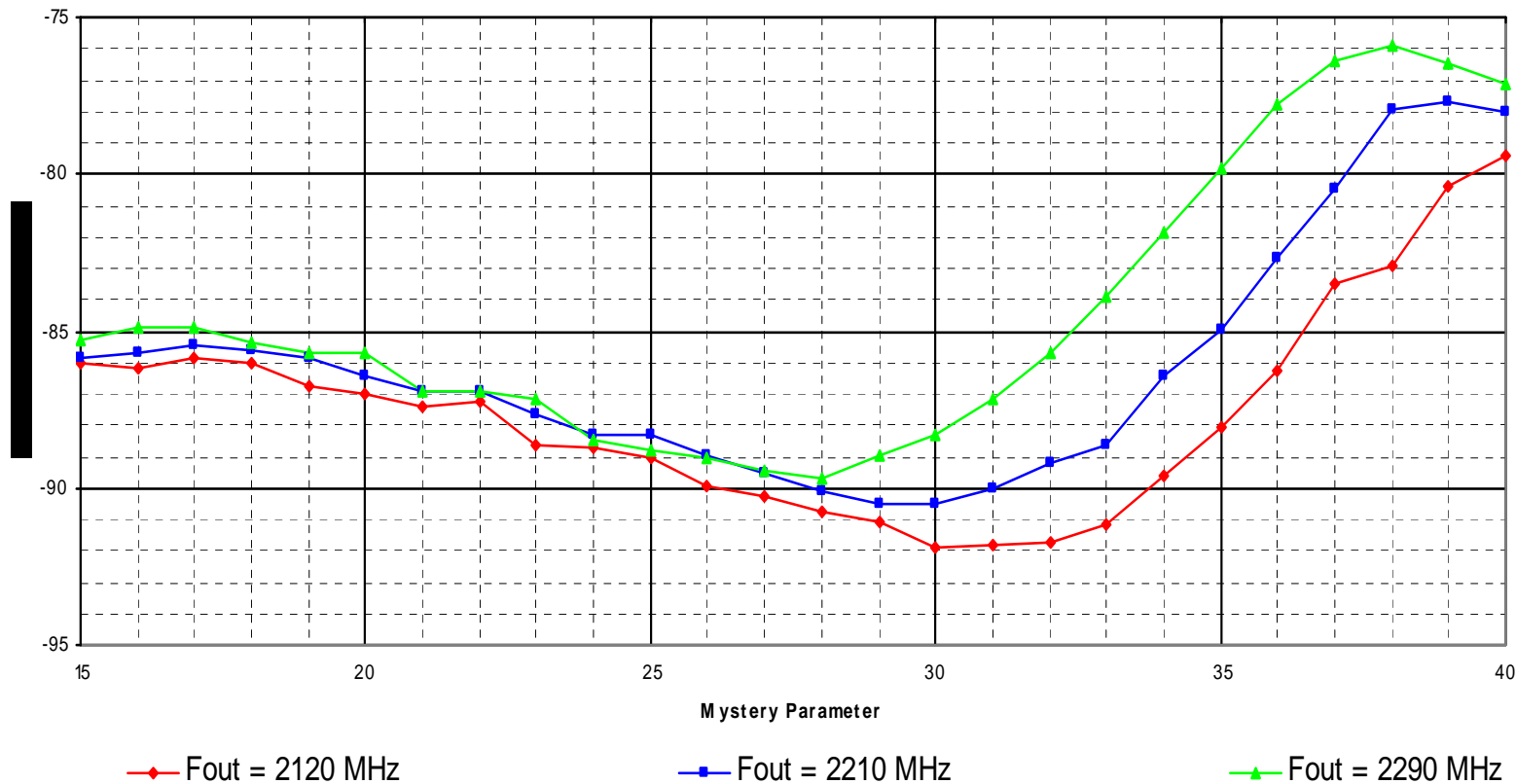
- If temperature changes without the VCO doing its frequency calibration, tuning voltage drifts towards a rail
- Typically bands overlap to accommodate for this
- National has a proprietary method to deal with this issue

- **Calibration Time**

- Faster for higher OSCin frequencies
- Improves lock time if bandwidth is narrow or if there are large cycle slipping issues
- Hurts lock time if loop filter is fast (i.e. <400 us)

# LMX2531 VCO Phase Noise Optimization

Phase Noise vs Mystery Parameter at 10 kHz Offset





# Traditional vs. Silicon VCOs

- **Traditional VCO Advantages**

- Potentially better performance (tuning range and/or phase noise) if there is a large tuning voltage supplied
- Can be customized to frequency

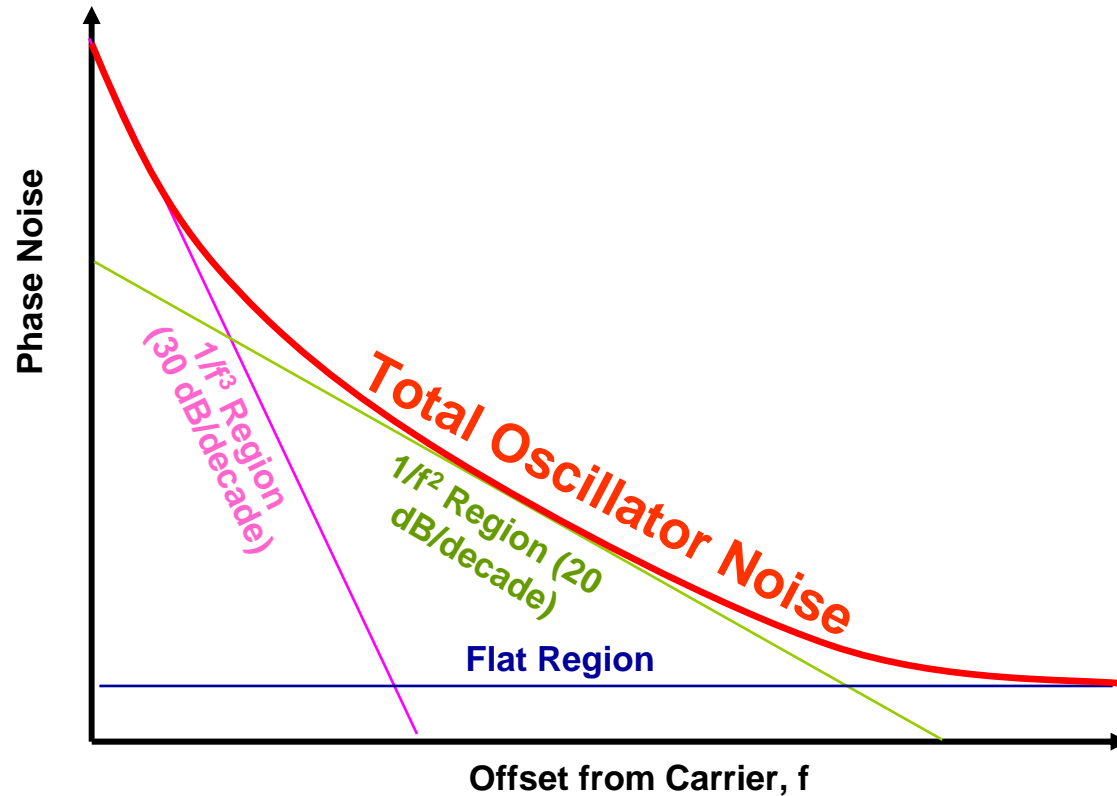
- **Silicon VCO Advantages**

- Lower Cost
- Smaller Size
- Higher Reliability
- VCO to PLL mismatch issues eliminated
- Wider tuning range for a given supply voltage
- Extra bells and whistles
  - Programmable Output Power
  - Switchable Dividers

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# Classical Oscillator Phase Noise Model





# Lesson's Equation

- Lesson's Equation

$$L(f) = 10 \cdot \log \left( N_3 \cdot \left( \frac{f_{\text{default}}}{f} \right)^3 + N_2 \cdot \left( \frac{f_{\text{default}}}{f} \right)^2 + N_0 \right)$$

Diagram illustrating the regions of the equation:

- $1/f^3$  Region points to the  $N_3 \cdot \left( \frac{f_{\text{default}}}{f} \right)^3$  term.
- $1/f^2$  Region points to the  $N_2 \cdot \left( \frac{f_{\text{default}}}{f} \right)^2$  term.
- Flat Region points to the  $N_0$  term.

- Parameters

- $N_3, N_2, N_0$  are constants to be discussed later
- $f_{\text{default}}$  is the a default frequency where these constants are defined, and is constant
- $f$  is the offset frequency



# 1/f<sup>3</sup> Region

- **Noise Coefficient**

$$N3 = \frac{1}{f^3} \text{ Noise Coefficient} = \frac{F \cdot k \cdot T}{P} \cdot \frac{f_{1/f^3} \cdot f_{vco}^2}{8 \cdot Q_L^2 \cdot f_{default}^3}$$

- **Phase noise goes down by 30 dB/decade in this region**
- **Phase Noise is caused by the flicker noise of the transistor**
- **Q<sub>L</sub> is the loaded Q of the inductor, and is the most important term and the one with the greatest influence**



# 1/f<sup>2</sup> Region

- **N2 Noise Coefficient**

$$N2 = \frac{1}{f^2} \text{ Noise Coefficient} = \frac{F \cdot k \cdot T}{P} \cdot \frac{f_{vco}^2}{8 \cdot Q_L^2 \cdot f_{default}^2} + \frac{2 \cdot k \cdot T \cdot R_{var} \cdot K_{vco}^2}{f_{default}^2}$$

- **Phase Noise goes down by 20 db/decade in this region**
- **R<sub>var</sub> is the noise resistance of the varactor diode. Note that for a larger VCO gain, K<sub>vco</sub>, this noise is multiplied.**
  - Putting multiple varactor diodes in parallel helps reduce this noise.
- **Loaded Q<sub>L</sub> is also important**



# Flat Region

- **Noise Coefficient**

$$N0 = VCO \text{ Noise Floor} = \frac{F \cdot k \cdot T}{P}$$

- **Terms here**

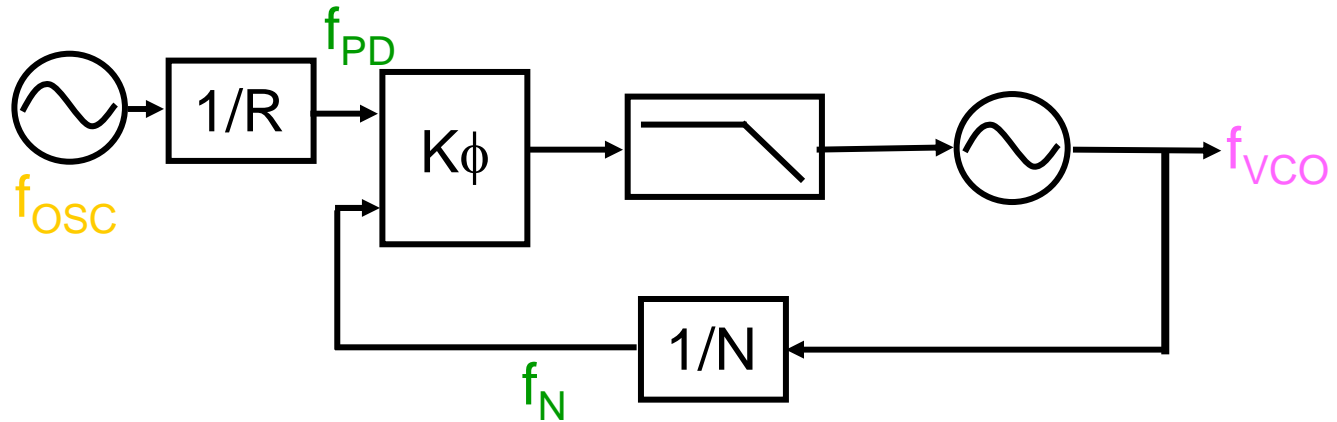
- F is the noise figure
  - T is the temperature in Kelvin
  - k is Boltzmann's constant
  - P is the output power
- **Output buffer dominates here. High output power is good for phase noise because of the thermal noise floor**
  - **Theoretically, the best VCO phase noise is at cold temperature and worse at hot temperature in all three regions**

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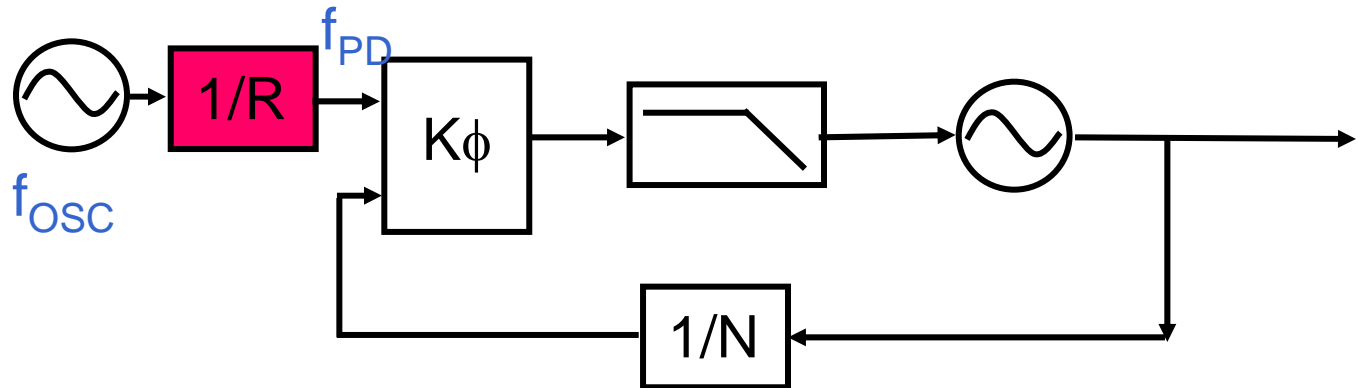
# Basic PLL Operation



$$f_{\text{osc}} / R = f_{\text{PD}} = f_{\text{N}} = f_{\text{vco}} / N$$

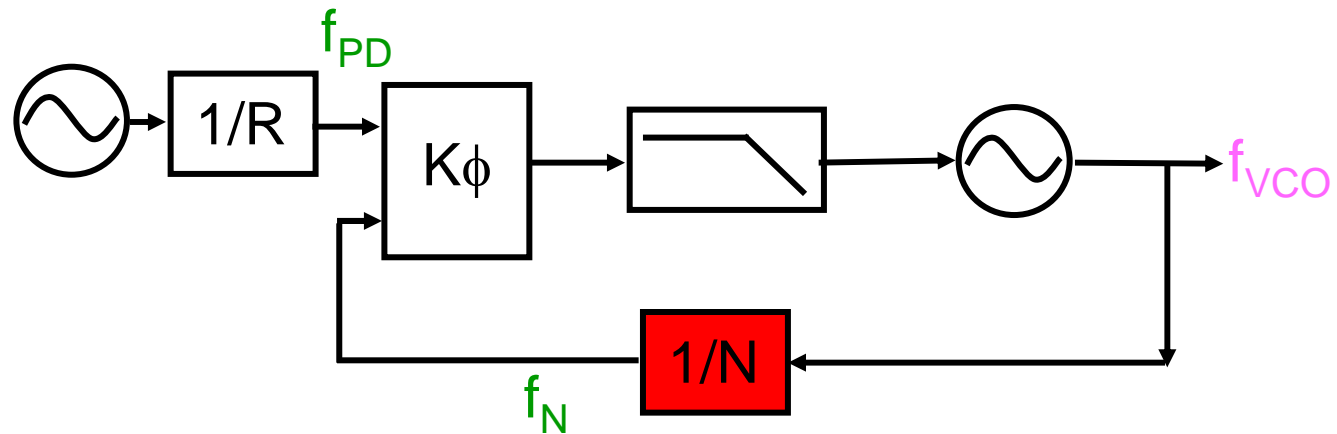
$$f_{\text{vco}} = f_{\text{osc}} \bullet (N/R)$$

# Reference Oscillator and R Counter



- **Phase Detector Frequency**
  - Fixed frequency of operation =  $f_{PD}$
  - Equal to the channel spacing for an integer PLL
- **R Counter Value**
  - $R = f_{OSC} / f_{PD}$

# N Counter

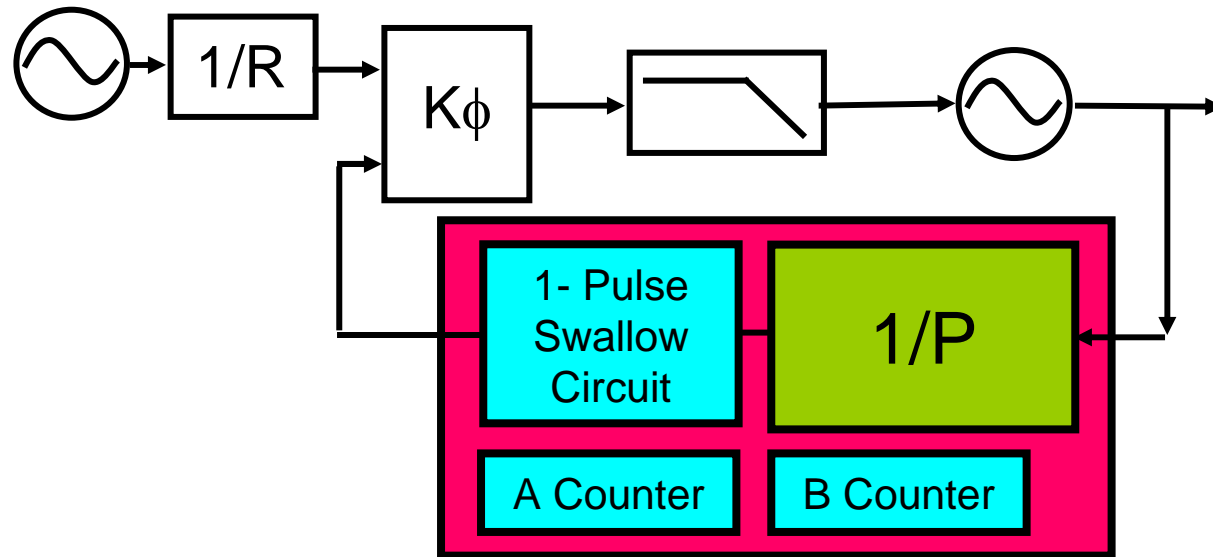


- **N Counter Value**

- $N = f_{VCO}/f_N = f_{VCO}/f_{PD}$

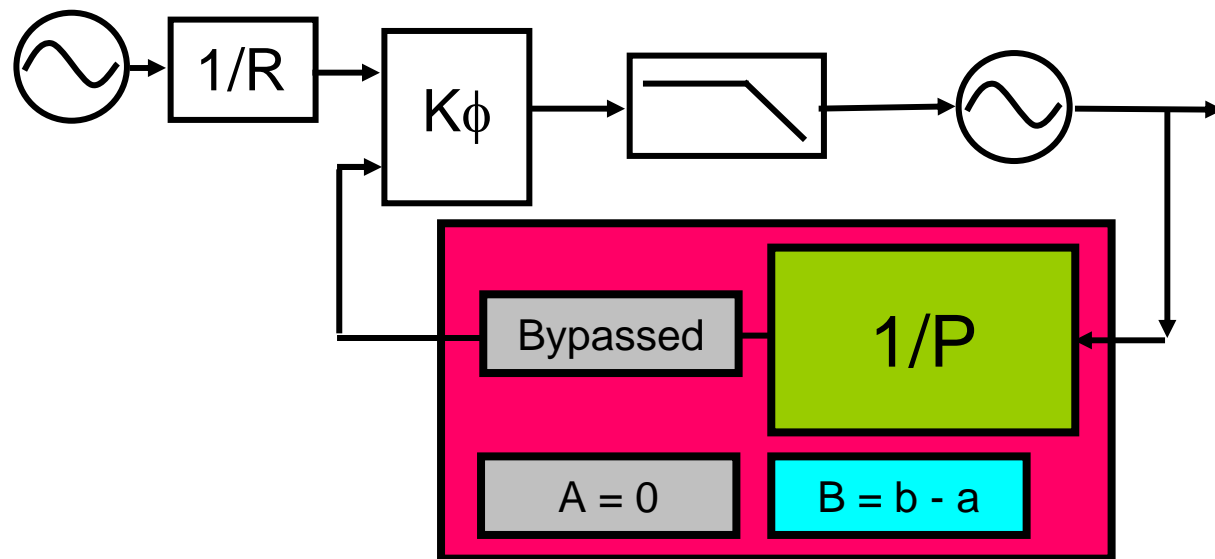
- **Because the input to this counter can be high frequency, prescalers are typically inside this counter**

# Dual Modulus Prescalers



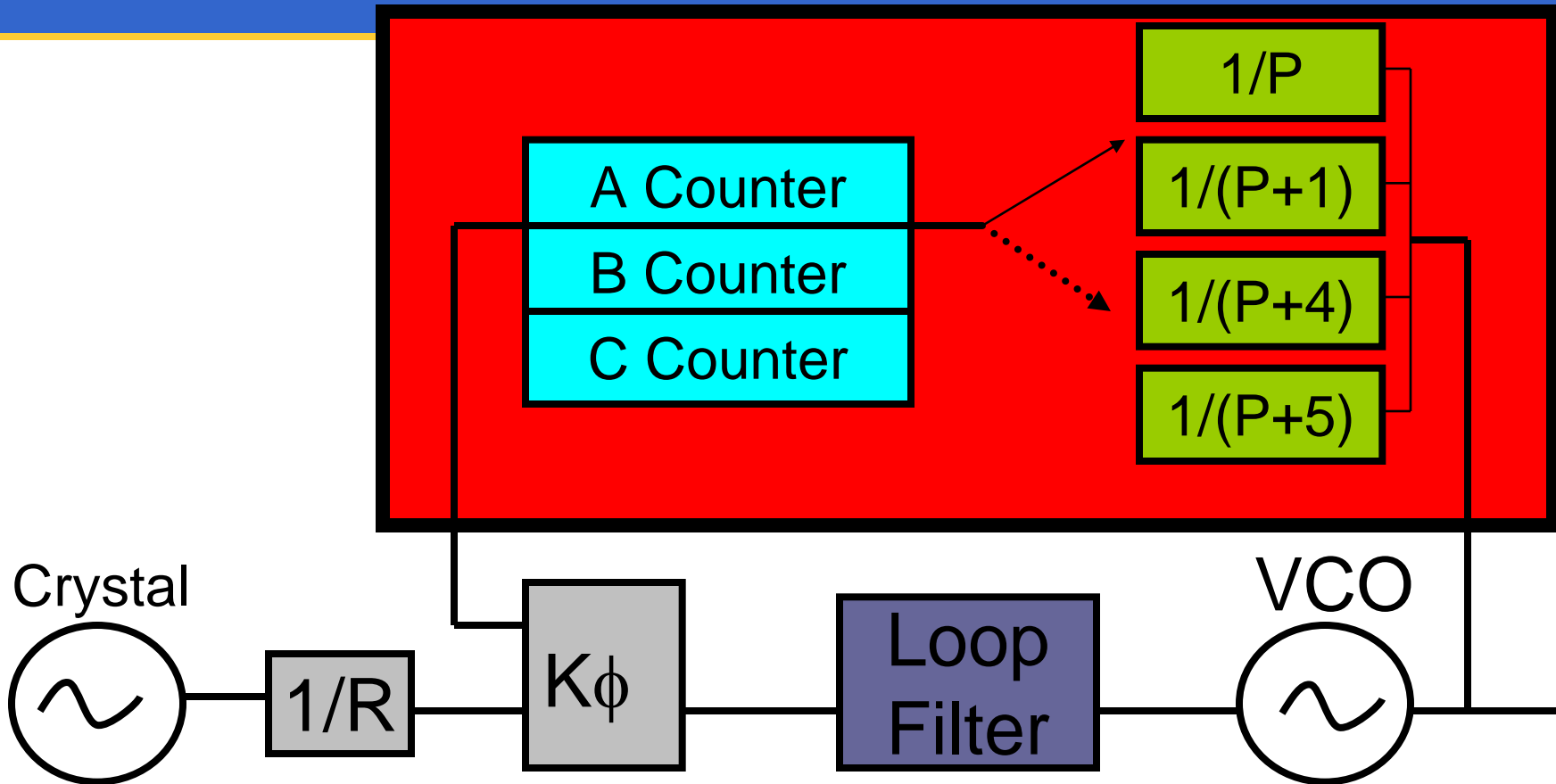
- **VCO Frequency is divided by prescaler**
  - Only the Prescaler has high frequency requirements
- **After the prescaler and the 1-pulse swallow circuit, each cycle decreases the A counter by 1 cycle**
  - This takes a•(P+1) cycles
  - B Counter is also decreased with the A counter

# Dual Modulus Prescalers



- **After the A counter reaches zero ..**
  - Pulse Swallow circuitry is disabled
  - B counter counts down to zero
  - This takes  $(b-a)IP$  cycles
- **Total N Count**
  - $N = a \cdot (P+1) + (b-a) \cdot P = P \cdot B + A$
  - $b \geq a$  is a consequence of this architecture

# Quadruple Modulus Prescaler



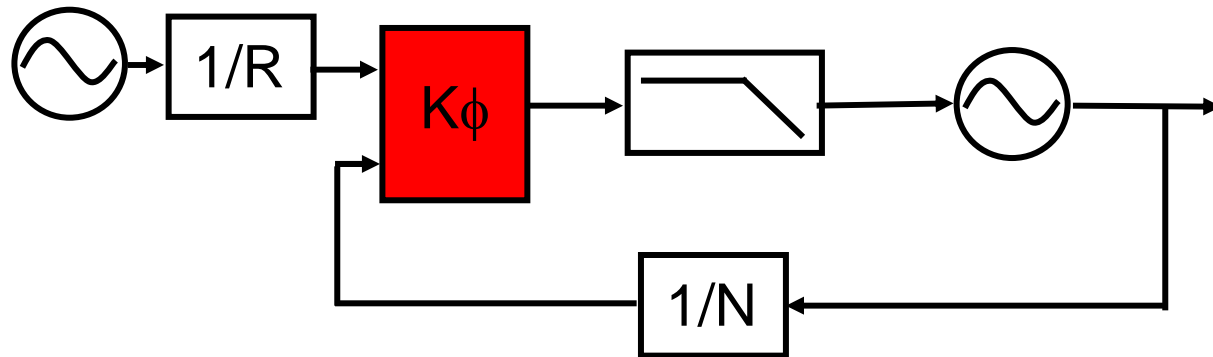
■ Advantage Allows lower divide ratios.

■  $N = P \cdot C + 4 \cdot B + A$

# Overview

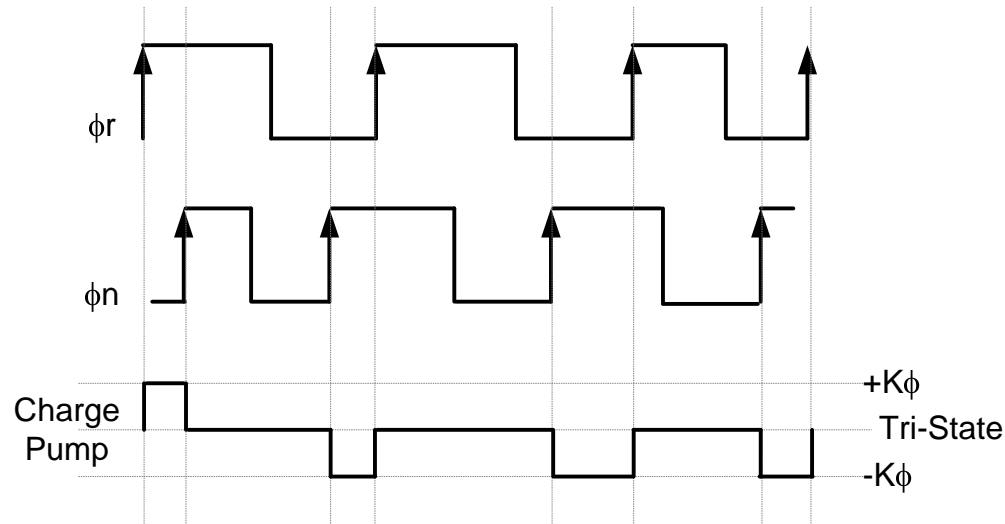
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# Phase Frequency Detector/Charge Pump



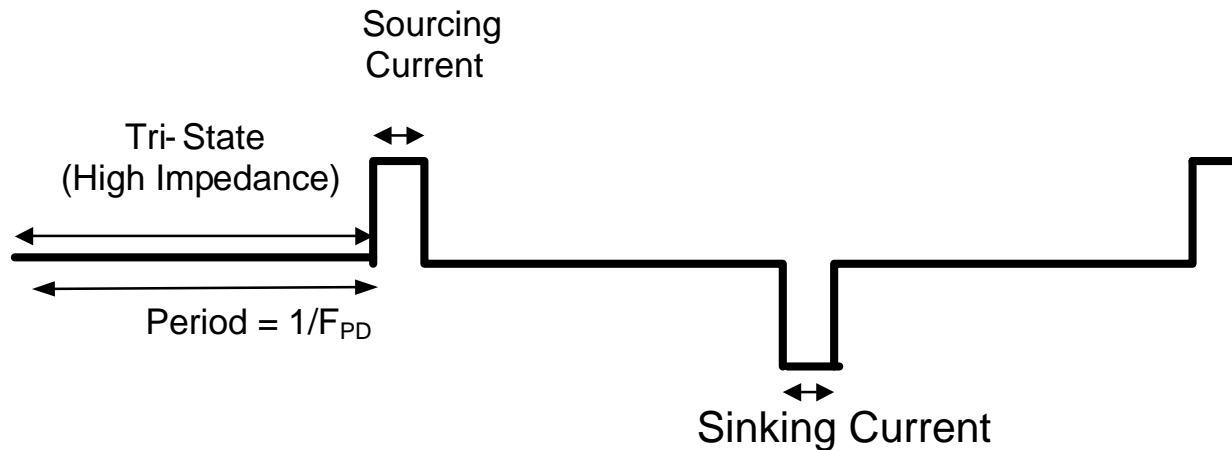
- **Phase Frequency Detector (PFD)**
  - Detects Frequency Error Between N and R Counter
- **Charge Pump**
  - Converts this frequency Error to a Correction Current
- **Usually, the PFD and Charge Pump are Integrated Together**

# Phase Frequency Detector/Charge Pump



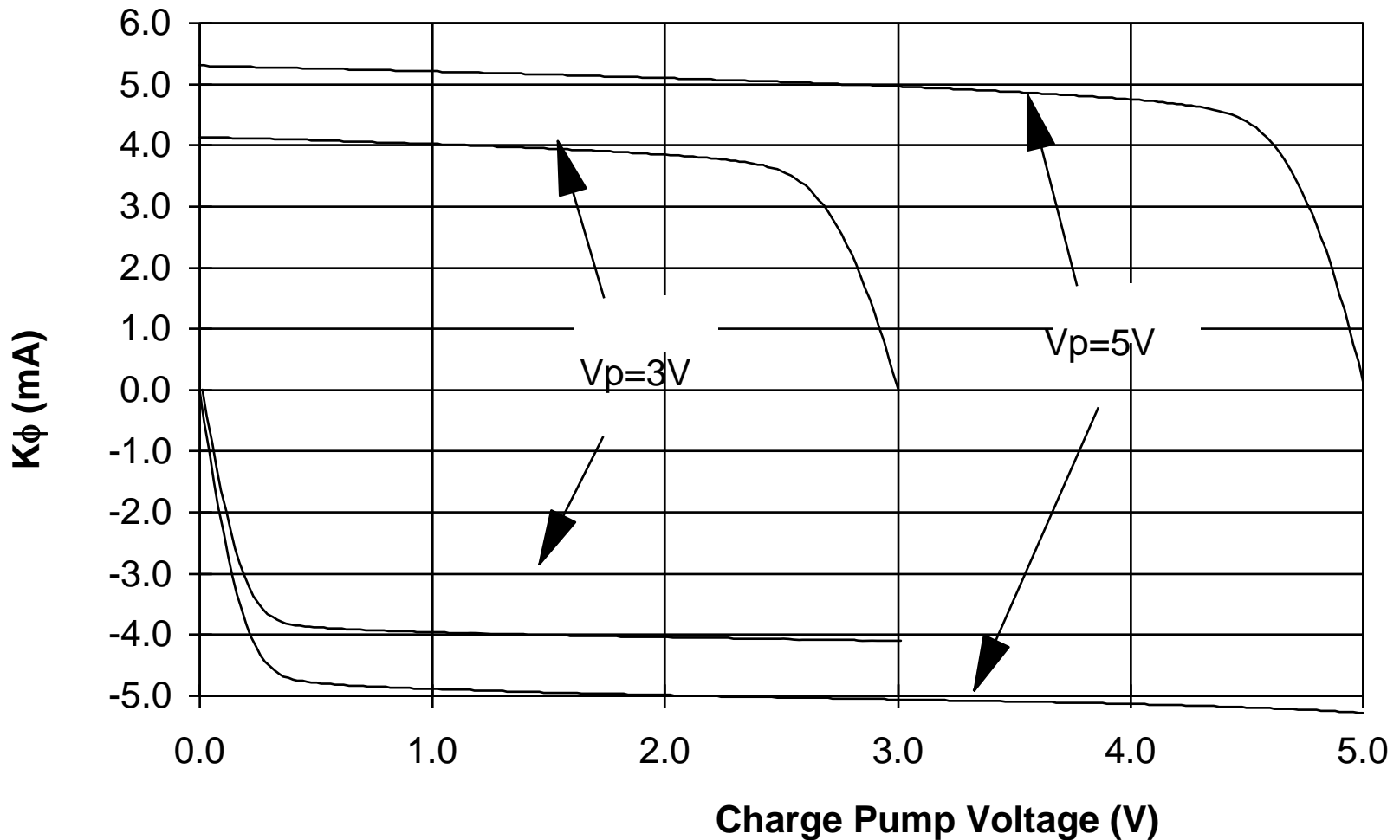
- **Detects differences in input signals**
  - Detects phase error between 2 input signals
  - Detects frequency error between 2 input signals
- **Outputs a voltage to the charge pump**
  - The average value of this voltage is proportional to the phase/frequency error.
  - Along with the rest of the system, ensures the 2 input signals are the same frequency and phase

# Phase Frequency Detector/Charge Pump

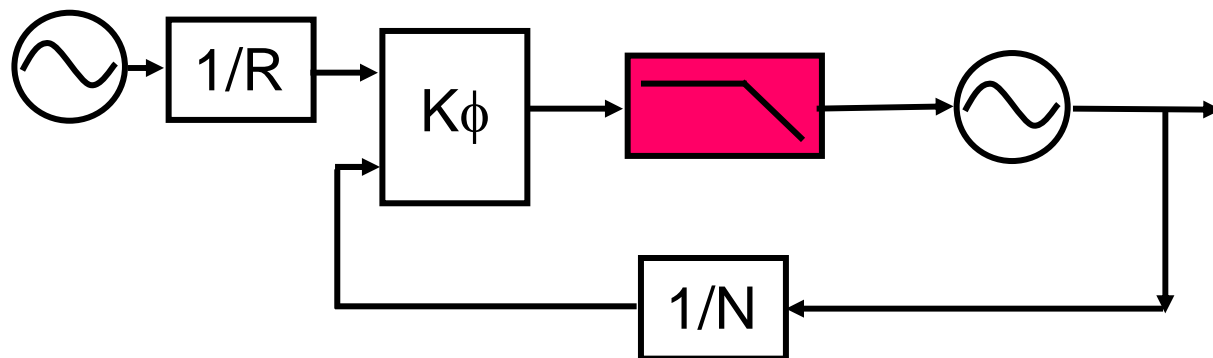


- **Charge Pump/Phase-Frequency Detector**
  - Sources Current if output frequency/phase is too low
  - Sinks Current if output frequency/phase is too high
  - High Impedance (tri-state) if output frequency/phase is correct (within tolerances)
- **Spurs Can Originate from the Charge Pump**
  - Want source and sink currents closely equal
  - Want tri-state to be very low leakage current

# Charge Pump Current



# Loop Filter



- **The loop filter is a low pass filter**
  - Accumulates correction currents from the Charge pump into a voltage
- **The loop filter has a dramatic effect on performance**
  - Determines the loop bandwidth
  - Impacts switching speed
  - Impacts spurs
  - Can impact phase noise
  - Many Design trade-offs involved
  - National has tools for this