



## Glossary of Terms

**Absolute maximum ratings:** The range of voltages, currents, temperatures, etc., outside of which the device's performance or reliability is expected to seriously degrade or the device will cease to function. Unless otherwise specified, these ratings are given for  $T_A = +25^\circ\text{C}$ . Combinations of maximum ratings may *not* be applied simultaneously.

**Accept number:** The maximum number of devices which may fail a sample test without causing rejection of the lot.

**Acceptor:** An impurity that can make a semiconductor P-type by accepting valence electrons, thereby leaving "holes" in the valence band of the semiconductor device. The holes act like carriers of positive charge.

**Active circuit area:** That area of a die or a hybrid substrate which contains all functional circuit elements, operating metallization or any connected combinations thereof, excluding beam leads.

**Active device:** A device which, when subjected to a current or voltage, exhibits either gain (amplification) and/or control characteristics, or a device which converts input signal energy into output signal energy through interaction with the energy from an auxiliary source(s).

**Alloying:** The step in the fabrication process immediately following evaporation. This process alloys the conductive metal which had been deposited on the die surface to that surface, thus providing ohmic contact with the active circuit elements.

**Alpha particles:** Helium nuclei emitted as a result of the radioactive decay of trace amounts of naturally occurring uranium and thorium found in semiconductor packaging materials. Alpha particles, if not properly controlled, can cause soft errors in dynamic memories.

**Analog device:** A microcircuit in which the output is a mathematical function of the input.

**Angstrom ( $\text{\AA}$ ):** A unit of length.  $10^4\text{\AA} = 1\mu$  (micron) or  $10^{10}\text{\AA} = 1\text{m}$  (meter).

**AOQL:** Average Outgoing Quality Level—The maximum acceptable reject percentage on the average for all outgoing lots.

**AQL:** Acceptable Quality Level—The maximum percent defective that can be considered acceptable as an average for

all lots screened. The sample size used with a given AQL will prevent acceptance of 95% of all lots having a greater percent defective.

**Architecture:** The functional design of a complex component, circuit or system, including both its hardware and its compatibility with external hardware and software.

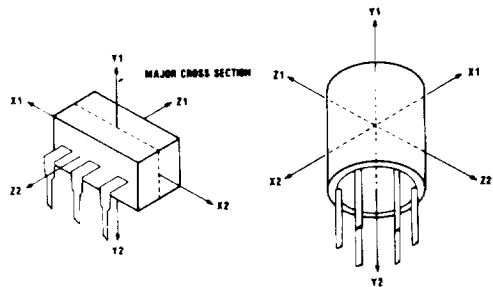
**ASIC:** Application Specific Integrated Circuit. A custom or semicustom integrated circuit, such as a cell or gate array, created for a specific application. The complexity of ASICs typically requires significant use of CAD techniques.

**ATP:** Acceptance Test Plan—A document developed for the purpose of detailing all of the testing involved in device and/or lot acceptance.

**Attributes data:** Gross quantitative data indicating the total number of devices subjected to and passing or failing the various screening steps in a test sequence.

**Audit:** Random surveillance of processes, specifications, etc.

**Axis:** A plane through a device established for the purpose of orienting the application of force during such stresses as constant acceleration.



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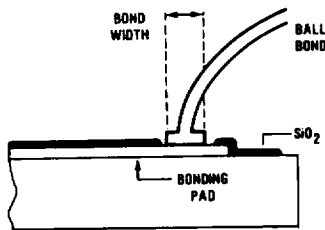
The most widely used axis is the  $Y^1$  axis, in which the application of force is such it will tend to lift the die off the mounting surface or the wires off the die.

**Back end:** A slang term frequently applied to the assembly and test portion of the semiconductor manufacturing process (see *Front end*).

**Backlapping:** Fine grinding or polishing of the bottom side of wafers prior to diffusion to reduce wafer stress and provide uniform thickness and planarity.

**Backside abrasion:** A process whereby the backside of a finished wafer is cleaned using a fine-granular powder under air pressure in order to remove all oxidation or any other materials. The resulting level of wafer cleanliness allows better die attach of dice from the wafer.

**Ball bonding:** Normally employed with gold wire, ball bonding employs a bonding head which compresses the end of the wire under high heat to flatten it onto a large area of the bonding pad.



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The term is derived from the round appearance of the bond when viewed from above. Ball bonding is frequently employed with small geometry die (such as transistors), since a ball bond of 1 mil wire can be accomplished with a 2.5-mil bond width, whereas an ultrasonic bond will typically be 4 mils in length. When ball bonding is employed, the opposite end of the wire will often be stitch bonded, since it is difficult to ball bond at both terminals.

**Baseline:** A detailed definition of a device's electrical and mechanical configuration, assembly, processing and testing used as a base from which to track subsequent changes.

**Bimetallic contamination:** A corrosion that results from the interaction of gold with aluminum that contains more than 2% silicon. At temperatures greater than 167°C, the silicon will act as a catalyst to create an aluminum-gold alloy. The resulting metallic migration results in gaps (called Kirkendall voids) in the gold-aluminum interface. Bimetallic contamination can decrease bond wire adhesion and can lower current carrying capability at the interface. In extreme cases, bond wires will actually lift from the pad. Bimetallic contamination is frequently referred to as "purple plague."

**Binary logic:** Logic using two logic states (ON and OFF, or Logic "0" and Logic "1").

**Bipolar:** Devices or processes in which current-carrying areas and substrates are of different polarities (such as the PNP and NPN transistors used to form TTL circuits). Both holes and electrons are transported in bipolar devices. Some technologies, such as BI-FET™, combine bipolar and unipolar elements.

**Bit:** One binary digit. In binary arithmetic all data is represented by 1's and 0's. In a semiconductor device, these logic levels are created by the presence or absence of electrons in a cell.

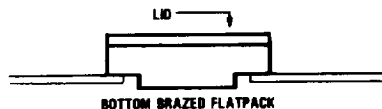
**Bit:** See *Built-in test*.

**Bonding pad:** An expanded metallization area on the surface of a die where the bonding wire will be placed.

**Bond-off:** An extra bond attached to the edge of the post or land area of a package (but never to the bonding pad on the die) for the purpose of clearing the bonding machine.

**Bond pull:** Pulling of the bond wires to destruction to determine the strength of the bonds. (See MIL-STD-883, Method 2011.) See also *Nondestructive bond pull*.

**Bottom-brazed flat:** A flat pack with the leads brazed to feedthroughs on the bottom of the package rather than passing through the package side.



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**Built-in test:** Subcircuitry designed into a circuit to allow that circuit to test itself either at a predetermined interval or upon external command.

**Bulk CMOS:** Conventional CMOS integrated circuit processes, so called because they are diffused into bulk silicon rather than on a substrate such as sapphire.

**Bulk impurities:** Random impurities of uncontrolled location and density present in the bulk silicon of the wafer prior to the diffusion processes. Bulk impurities are of concern because of the growth of the various oxide layers employed during the diffusion process can result in impurity relocations and concentrations. Concentrated impurities (which are typically oxygen, carbon, or sulphur) can create unwanted parasitics or various types of latent defects that can lead to premature failure.

**Burn-in:** The application of electrical biases to a device while operating it at an elevated temperature (usually 125°C), normally as a 100% screening test. Standard burn-in durations are 160 hours for Class B devices and 240 hours for Class S. This test is designed to "weed out" devices subject to infant mortality or excessive parametric drift. (See MIL-STD-883, Method 1015.)

**Burst radiation:** Large amounts of rapid dose rate ionizing radiation [normally in excess of 10<sup>8</sup> rads (Si)/sec] resulting in device latch-up, data upset, threshold shift or other performance degradation. Burst radiation is usually associated with nuclear weapon detonation.

**CAD:** Computer Aided Design. The use of computer automation in the implementation of all or a portion of a design for a complex circuit.

**CAM:** Computer Aided Manufacturing. The use of computer automation for all or a portion of the assembly process for a product.

**Candidate device:** A term used by MIL-M-38510 to designate a device which has been or will be subjected to a specified test or screening flow but has not yet successfully completed that testing.

**Capacitive decoupling:** Protection of a device from voltage transients or "spikes", or the isolation of a device from an AC voltage by decoupling the voltage source(s) to ground through a capacitor.

**CATE:** Computer Aided Test Engineering. The use of computer automation for the preparation of electronic test programs.

**Cavity device:** A semiconductor device containing an internal cavity (as opposed to a molded device).

**Cell array:** An integrated circuit formed through the positioning and interconnection of a number of functional blocks, or cells, on a die.

**Centralized processing:** In digital data systems, a system which utilizes a single large processor, normally in multiprocessing or multiprogramming modes, to perform all required system computations.

**Centrifuge:** See *Constant acceleration*.

**Cerdip:** Ceramic dual-in-line package with a glass seal. The conventional metal dual-in-line and the side-brazed dips both have a solder seal.

**Cerpac:** Ceramic flat package with a glass seal. (The conventional metal flat package and the bottom-brazed flat pack have solder seals.)

**Certificate of conformance:** A certificate provided by a manufacturer's QA department to the procuring activity with a lot of material to confirm that all material in the lot conforms with all applicable specifications.

**Change control:** See *Configuration control*.

**Channel:** A region of surface conduction opposite in type from that expected from the bulk doping. Channels are sometimes introduced unintentionally by surface ionic contamination. The type of channel (P or N) will be determined by the type of majority carrier introduced into the channel.

**Characterization:** Electrical testing performed for the purpose of determining typical device performance characteristics and/or parametric limits.

**Charge carrier:** A carrier of electrical charge within the crystal of a solid state device, such as an electron or a hole.

**Chip:** See *Die*.

**Chip carrier:** A leadless package used in the construction of both hybrids and boards. The chip carrier has a body configuration similar to a flat pack, but electrical connection is made through contacts on the package base rather than through conventional leads.

**Class (electrical classification testing):** Post assembly 100% electrical sort testing; not to be confused with the product assurance classes defined by MIL-STD-883.

**Class (product assurance class):** Per MIL-STD-883, there are two product assurance classes representing different levels of anticipated device reliability: Class B, which is intended for airborne equipment; and Class S, which is intended for space flight. For further details on these classes, see Chapter 4.

**Class 10, 100, etc:** See *Particle count*.

**CMOS (complementary MOS):** An MOS technology in which both P-channel and N-channel devices are fabricated on the same die.

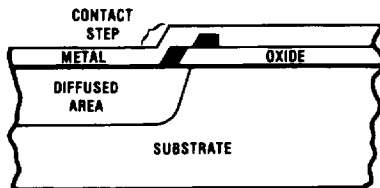
**Coefficient of thermal expansion:** The measurement (in %/°C or ppm/°C) of the rate at which a given material will expand or contract as the temperature changes. Where two materials with different rates of thermal expansion are joined, expansion or contraction will strain the bond interface between them. Continual straining of that bond could result in separation.

**Complex hybrid:** A hybrid having an inner seal perimeter (that is, cavity perimeter) of greater than 2 inches (as defined in MIL-STD-883, Method 5008).

**Compound bond:** In hybrids, the monometallic bonding of one band on top of another.

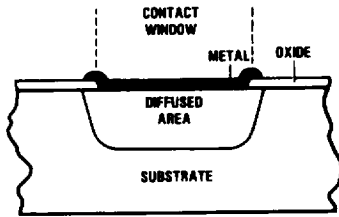
**Configuration control:** A requirement that a vendor notify the procuring and/or qualifying activity of a change in product manufacture or test. In some cases, the requirement will include delay of change implementation until after formal approval of the change.

**Contact step:** The drop from the surface of the passivation to the surface of the contact itself. (See Appendix A.)



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**Contact window:** The opening in the surface passivation through which the device metallization makes contact with the circuit elements. (See Appendix A.)



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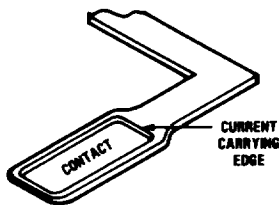
**Constant acceleration:** The subjecting of devices to a G force (typically 30,000 G's) in a centrifuge for a short duration in order to test die-attach, lead bond and package integrity. (See MIL-STD-883, Method 2001.)

**CPU:** Central Processing Unit.

**Crazing:** The propagation of small cracks in the glassivation layer of a semiconductor device.

**CSIC:** Customer Specific Integrated Circuit. An integrated circuit designed for one specific application for one customer. With the growth of semi-custom devices, such as gate arrays, this term has been discarded in favor of ASIC.

**Current carrying edge:** That portion of metal over a contact window that is closest to the point at which the metallization stripe enters the contact window.



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**Current density:** The amount of current flow per unit of cross-sectional area within device metallization. For example, a 1 mA current flowing through a metallization stripe that is  $3\mu$  wide and  $1\mu$  thick would result in a current density of  $0.33 \times 10^5$  A/cm<sup>2</sup>.

**Data check:** Analysis and review of data after devices have been read-and-recorded to ensure that all readings have been properly performed and all rejects have been removed from the lot.

**Data log:** Same as *Read-and-record*.

**Data pack:** The operation during which all of the various data generated during the process of screening a lot is verified and organized for shipment to the customer.

**Data upset:** The loss of stored data in a memory device as a result of burst radiation. The radiation either causes the activation of a parasitic circuit or the reversal of the stored data state.

**Date code:** A three- or four-digit number identifying the inspection lot from which material was selected. The first two digits (or first digit for a three-digit code) identify the year, the last two the week. Normally, the date code is based upon week of seal for the first subplot of the inspection lot.

**Delta ( $\Delta$ ):** A limit applied to the amount of parametric drift that a unit may display across a screen or series of screens (usually applied to burn-in).

**Depletion layer:** The region in a semiconductor where essentially all charge carriers have been swept out by the electrical field which exists there.

**Destructive testing:** Sample testing which is sufficiently severe to make further use of the tested devices questionable. Devices subjected to destructive testing may not actually be destroyed, but are sufficiently degraded that they should not be used in any system.

**Dice:** Plural of die (see *Die*).

**Die:** A single square or rectangular piece of silicon into which a specific semiconductor circuit has been diffused.

**Dielectric breakdown:** The damage occurring within an oxide layer when a voltage greater than its breakdown strength is applied across it.

**Dielectric isolation:** A semiconductor fabrication process in which each circuit element is enclosed within an oxide barrier that completely isolates the element from all other diffused elements. (See Appendix A.)

**Die-on-tape:** Dice mounted on flexible ribbon tape by bonding the bonding pads of each die to contacts on a lead frame on the tape, thus allowing electrical and other testing prior to assembly of the die into packages or onto hybrid substrates.

**Die shear:** The application of sufficient force to shear a die from the die attach medium in order to demonstrate die attach integrity. (See MIL-STD-883, Method 2019.)

**Die sort:** Electrically, a probe to sort the dice on a wafer according to predetermined electrical limits. Visually, a sort into Condition A, Condition B, or commercial grade dice.

**Diffused area:** A portion of the die where impurities have been diffused into the surface of the silicon at high temperature to change its electrical characteristics through the creation of a concentration of N or P charge carriers. (See Appendix A.)

**Digital device:** A microcircuit in which the inputs accept logic states (such as 0 or 1) and convert these to logic states at the output(s) according to a predetermined set of logic equations or function tables.

**DIP:** Abbreviation for dual-in-line package.

**Discrete:** A semiconductor or semiconductor die containing only one active device, such as a transistor or a diode.

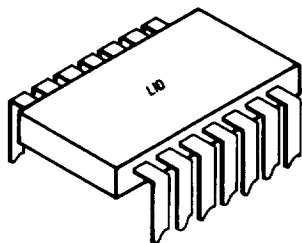
**Distributed processing:** In digital data systems, the utilization of a number of dedicated processors distributed throughout the system for the purpose of doing computation locally.

**Donor:** An impurity that can make a semiconductor N-type by donating extra "free" electrons to the conduction band. The free electrons are carriers of negative charge.

**Doping:** The introduction of an impurity into the crystal lattice of a semiconductor to modify its electrical properties by creating a concentration of N or P carriers.

**DPA (Destruction Physical Analysis):** A sample of finished devices that are destroyed in the process of opening and testing to assure that quality standards are met. This test is usually performed for internal visual, die shear strength, and bond pull strength.

**Dual-in-line package:** A package (either hermetic or molded) with its leads emanating from both sides of the package, then turning downward. (See also *Side-brazed dip*.)



Dual-In-Line

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**DUT:** Device Under Test.

**Dynamic RAM:** See *RAM*.

**EAROM:** Electronically Alterable Read Only Memory—Functionally similar to EEPROM.

**EEPROM (E<sup>2</sup>PROM):** Electronically Erasable-Programmable Read Only Memory—A memory device whose content can be established through a programming process (usually the tunneling of electrons across a thin layer of silicon dioxide to a floating gate. Each memory cell of an EEPROM can be individually erased by imposing a voltage to reverse the flow of electrons to move them away from the floating gate. That cell can then be reprogrammed. Both programming

and erasing can be performed without removal of the device from the system in which it is used.

**Effectivity date:** The date upon which a new military document or a new revision of an existing document goes into effect (see *Implementation date*).

**Electromigration:** Particle migration in aluminum thin-film or polysilicon conductors at grain boundaries as a result of high current densities. Electromigration can lead to either an open circuit condition in a conductor or a short between adjacent connectors.

**Electrostatic sensitivity:** Susceptibility to damage or degradation as the result of subjection to electrostatic discharge. Typically much higher for MOS devices than for bipolar.

**Electrostatic discharge:** The discharge of accumulated static charge (typically of high voltage at low current) from one collector to another, usually by jumping the air gap between the two.

**Element:** A topographically distinguishable part of a microcircuit which contributes directly to its electrical characteristics.

**Encapsulation:** The process of encapsulating or "potting" a molded device.

**EOL (end-of-line testing):** Those tests performed in assembly after the seal operation in order to confirm the quality of the device assembly. Testing would normally include such screens as stabilization bake, constant acceleration, temperature cycle, and hermeticity testing.

**Epi:** See *Epitaxial layer*.

**Epitaxial layer:** A monocrystalline layer of material deposited onto a substrate in such a manner that the layer being formed has the same crystal orientation as the substrate material. (Often referred to as "epi".)

**EPROM:** Erasable Programmable Read Only Memory—A memory device whose content can be established through a programming process (usually hot electron injection) and can be totally erased by exposure to ultraviolet light for sustained periods (typically 30 minutes). When properly erased, the device can be reprogrammed.

**Eutectic:** An alloy of two or more metals with the lowest melting point that is possible from any combination of those metals. The melting point of the eutectic will normally be lower than the melting point of either metal in its pure state.

**Evaporation:** One of the final steps in processing a wafer during which conductive metal, usually aluminum, is deposited on the surface of the wafer in order to provide electrical interconnection of the various active elements on each die. Metallization may also be accomplished through sputtering.

**Failure Analysis:** A post-mortem examination of failed devices for the purpose of verifying the reported failure and identifying the mode or mechanism of failure. Failure analysis techniques may range from simple electrical and/or visual examination to some of the more advanced techniques of physics, metallurgy, and chemistry. (See MIL-STD-883, Method 5003.)

**Failure rate:** The calculated rate at which device failures will occur within a total device population (normally expressed in terms of percent per thousand hours or devices per  $10^6$  unit hours).

**Fault isolation diagnostics:** A feature (normally associated with built-in test) that allows identification of a malfunctioning subcircuit or circuits within a complex device.

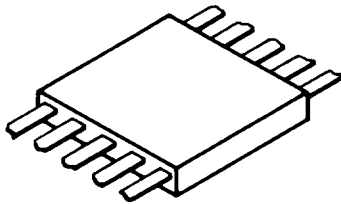
**Feature size:** The smallest controllable dimension on the surface of a die, usually determined by minimum line width.

**FID:** See *Fault isolation diagnostics*.

**Filament short:** The growth of a filament between two conductive areas as the result of high thermal or voltage stress, shorting the two areas together.

**Fine leak:** See *Hermeticity*.

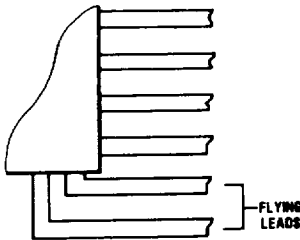
**Flat package:** A thin package with ribbon leads coming out opposite sides of the package. (See also *Bottom-brazed flat*.)



Flat Package

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**Flying lead:** On a flat pack device, a lead which exits from the end rather than the side of the package, then makes a right-angle turn to parallel the other leads.



FLYING LEADS

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**Forcing function:** The applied voltage(s) or current(s) at which a parametric or functional test is performed.

**Foreign material:** Any material that is foreign to a microcircuit or any non-foreign material that is displaced from its original or intended position within a microcircuit package.

**Frit seal:** Sealing accomplished through the melting and re-hardening of a glass seal ring (or frit) between the package base and lid. The package leads typically pass through the sealing area.

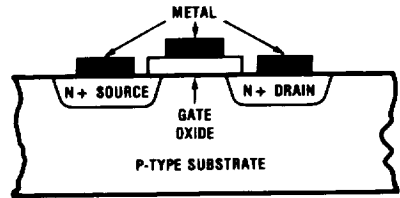
**Front end:** A slang term often applied to the wafer fabrication portion of the semiconductor manufacturing process.

**Gallium Arsenide (GaAs):** A semiconductor base material whose high electron mobility has led it to be used in the fabrication of high speed circuits. GaAs circuits are not considered as easy to manufacture as silicon circuits.

**Gate array:** An integrated circuit containing a large number of gates that can be interconnected in any number of combinations to satisfy specific individual applications (see *ASIC, CSIC*).

**Gate equivalent:** The basic unit of measure for digital circuit complexity, based upon the number of individual logic gates that would have to be interconnected to perform the same circuit function.

**Gate oxide:** A thin film of dielectric oxide material bridging the source and drain regions of an MOS semiconductor. (See Appendix A for more detail.)



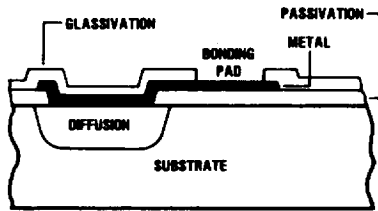
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**Generic data:** Qualification or quality conformance data on devices from the same generic product family as the device shipped.

**Generic family:** A group of devices manufactured and assembled on the same line(s), using the same processes and materials, and designed to perform the same basic function (e.g., operational amplifiers, TTL gates, etc.).

**Glass frit seal:** See *Frit seal*.

**Glassivation:** The protective coating (usually silicon dioxide or silicon nitride) placed on the entire die surface (exclusive of bonding pads).



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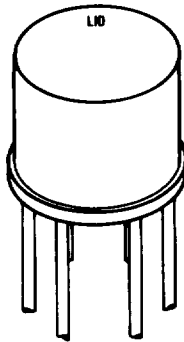
**Gross leak:** See *Hermeticity*.

**Grown junction:** A PN junction made by controlling the type of impurity in a single crystal while it is being grown from a melt.

**Hardware:** The physical elements and interfaces that constitute a component or system.

**HDL:** Hardware design language, a software tool used for hardware design (see CAD).

**Header:** Sometimes called metal can package—A cylindrical semiconductor package with a metal lid and with leads emanating from the package base. A header may or may not have a ceramic standoff to prevent contact with the mounting surface.



Header

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**Hermetic device:** See *Cavity device*.

**Hermeticity:** Leak or seal testing performed on all hermetic packages to confirm seal integrity. This is done in two steps, fine leak, which looks at leak rates in the  $5 \times 10^{-9}$  cc/sec range, and gross leak, which looks for devices with gross seal defects. (See MIL-STD-883, Method 1014.)

**High temperature storage:** A high temperature (150°C typically) bake performed for an extended period (usually 1000 hours) without electrical power applied. Notice 2 to Revision A of MIL-STD-883 deleted this test from Group C. (See MIL-STD-883, Method 1008.)

**Hole:** The absence of a valence electron in a semiconductor crystal. The movement of a hole is equivalent to the movement of a positive charge.

**HTOT:** High Temperature Operating Test—A burn-in performed at very high temperature (typically 250°C) for the purpose of determining long-term reliability of a lot of devices on a sample basis under extremely accelerated conditions. (See MIL-STD-883, Method 1005, Condition F.)

**Hybrid microcircuit:** A microcircuit composed of thin or thick film components and semiconductor chips (either integrated circuits or discretes) on a substrate.

**IC:** Abbreviation for integrated circuit.

**Implementation date:** The date by which a new military document or a new revision of an existing document must be implemented by those to whom its requirements apply. This date may be different than and later than the effectivity date.

**Ingot:** A cylindrical piece of semiconductor material from which individual wafers will subsequently be sliced.

**Ingot Growth:** The process through which an ingot of semiconductor material is created.

**Inspection:** Actual performance of a screening step, as opposed to surveillance.

**Inspection lot:** A lot of devices which is considered a single lot for qualification or quality conformance inspection purposes. An inspection lot may consist of more than one device type if they are from the same generic family. The most generally accepted definition of an inspection lot is a group of devices in a single package type, outline, and lead finish manufactured on the same production line(s) through final seal by the same production techniques, using the same materials, and sealed within the same 6-week period.

**Insulating layer:** A dielectric layer used to isolate multilevel conductive and resistive material or to protect top level conductive resistive material (see *Glassivation, Passivation*).

**Integrated circuit:** A semiconductor or semiconductor die containing multiple elements (which may be located on the die or on a hybrid substrate) which act together to form the completed device circuit.

**Interconnect:** The metallization connecting two or more active elements on the surface of a die; also, the wires connecting the die to the package leads.

**Internal visual:** Visual inspection of the device prior to seal to insure that die, wires and package conform to all applicable specifications. (See MIL-STD-883, Method 2010 and Method 2017.)

**Internal wafer vapor content:** The amount of residual moisture trapped within a semiconductor package cavity after device sealing, usually stated in ppm at 100°C.

**Ion implantation:** Introduction into a semiconductor of selected impurities in controlled regions (via high voltage ion bombardment) to achieve desired electronic properties.

**Isolation tub:** An area of the die surrounded by an isolation diffusion (normally P+) to prevent electrical leakage between adjacent circuit elements. (See Appendix A.)

**JAN:** Joint Army Navy—The trademarked designator used to indicate that a given device was manufactured and screened in accordance with a controlled government specification. The JAN mark is frequently abbreviated to J when used on smaller devices. (See Chapter 5.)

**Jump bond:** See *Skip bond*.

**Junction:** The boundary between a P-region and an N-region in a silicon substrate. (See Appendix A for further details.)

**Junction burnout:** See *Thermal secondary breakdown*.

**Kerf:** That portion of the resistor area of a microcircuit from which resistor material has been removed or modified by trimming.

**Kirkendall voids:** See *Bimetallic contamination*.

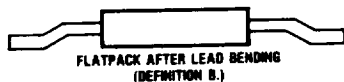
**Lambda ( $\lambda$ ):** Similar to an LTPD, except that it is expressed in percent per thousand hours.

**Land area:** That portion of the package lead which is inside the package cavity and to which the bonding wire will be connected to make electrical contact with the die.

**Latchup:** A condition where the output of a circuit has become fixed near one of the two voltage extremes and will no longer react to changes in the input signal. Latchup may be radiation induced, but can also result from voltage over-stresses and other causes.

**LCC:** See *Chip carrier*.

**Lead bend:** A. A torsion test for lead strength. (See *Lead fatigue*.) B. The process whereby flatpack leads are reformed to facilitate mounting on a PC board.



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**Lead fatigue:** Application of a repetitive bending force to the leads of sample devices to insure structural integrity of leads and packages. (See MIL-STD-883, Method 2004.)

**Lead integrity:** See *Lead fatigue*.

**Leadless package:** See *Chip carrier*.

**Leak test:** See *Hermeticity*.

**Lid torque:** A test which tests the integrity of the seal of a semiconductor device (usually one that employs a glass frit seal) by twisting the package and the lid in opposite but parallel directions.

**Line width:** A measure of the horizontal dimensions of surface features of a semiconductor die, such as the separation between gate and drain diffusions on an MOS die.

**LSI:** Large Scale Integration—LSI devices are generally accepted to be those that contain between 100 and 1000 gate equivalents, or other circuitry of similar complexity. (See *VLSI*.)

**LTPD:** Lot Tolerance Percent Defective—A single lot sampling concept that statistically ensures rejection of 90% of all lots having a greater percent defective than the specified LTPD.

**Macrocell:** A semiconductor building block containing a relatively complex electronic function that can be combined through CAD with other cells to perform a complex function with less design effort than a complete "ground-up" design.

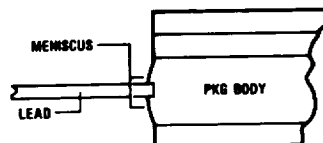
**Majority carrier:** The mobile charge carrier (hole or electron) that predominates in a semiconductor material. When a channel is created within the silicon, the channel will normally result from a change of majority carrier.

**Mask:** A patterned screen of any of several materials used to expose selected areas of a semiconductor covered with a light-sensitive photoresist to polymerizing light during the fabrication process.

**Mechanical shock:** An impact-type shock test to stress die attach, wire bonds, and seal integrity, normally performed on a sample basis. (See MIL-STD-883, Method 2002.)

**Megarad:** Capable of withstanding total dose radiation of  $10^6$  rads (Si) or greater without significant performance degradation.

**Meniscus:** The localized convex area of the package through which the lead protrudes.



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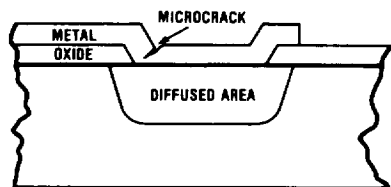
**Metal can package:** See *Header*.

**Metal gate:** An MOS process fabricated with a metal (usually aluminum) as the gate electrode.

**Metallization melt:** The melting of semiconductor metallization as a result of extreme power exposure, normally occurring as a result of short duration, high current pulses.

**Metallization run:** A lot of wafers metallized at the same time. Since the number of wafers accommodated by an evaporation (i.e., metallization) chamber is frequently less than the number of wafers accommodated by a diffusion chamber, it is possible to have several metallization runs which came from the same wafer run.

**Microcrack:** A very small crack within the metal or other material of a semiconductor device, typically not detectable using optical magnification. In the metallization area, microcracks most typically occur at contact steps. Microcracks can lead to discontinuities in the circuitry.

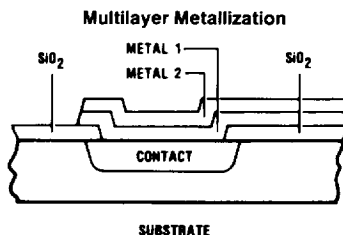


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**MTBF:** Mean Time Between Failure—The average number of operating hours after a device has failed that would pass before the next device failure would be expected to occur.

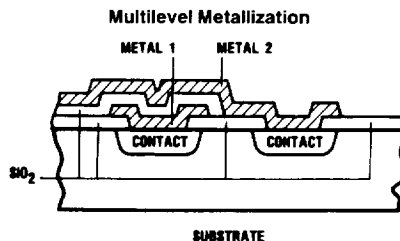
**Multichip device:** A device containing two or more die, but no thin or thick film components on the substrate (such as the LH2111, which consists of two LM111 chips in a single package).

**Multilayer metallization:** Metallization formed through the deposition of several layers of different metals to form a single metallization stripe on the surface of the device.



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**Multilevel metallization:** Metallization formed through the deposition of several layers of metal with dielectric (such as  $\text{SiO}_2$ ) separating the various levels except where interconnection of levels is required.



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**Microelectronic device:** See *Microcircuit*.

**Micron ( $\mu$ ):** A unit of length.  $10^6\mu = 1\text{m}$  (meter). [Note:  $\mu$  as a symbol of length should not be confused with  $\mu$  used as a prefix to indicate microunits, such as  $\mu\text{A}$  (microamps) or  $\mu\text{V}$  (microvolts). A micron is one micrometer.]

**Migration:** The relocation or movement of physical materials into or across other adjacent materials. (See *Electromigration*.)

**Minority carrier:** The nonpredominant mobile charge carrier in a semiconductor (such as electrons in a P-region, where the majority carrier would be holes).

**Moisture resistance:** Subjection of sample devices to a cycle of high humidity and temperature stresses to determine the ability of these devices to survive under severe environmental conditions. This is normally performed on a sample basis with 10 cycles of 24-hour duration. (See MIL-STD-883, Method 1004.)

**Molded device:** A device which is completely encapsulated in epoxy or an alternate molding compound, that is, with no internal cavity.

**Monolithic device:** A device whose circuitry is completed contained on a single die or chip.

**MSI:** Medium Scale Integration—MSI devices are generally accepted to be those that contain 12 or more gate equivalents, but less than 100. (See *LSI*.)

**N-channel:** An MOS process in which MOS transistors are formed by bridging two adjacent N-type diffusions (source and drain) with a dielectric (gate). When the source and the substrate are grounded and a positive voltage is applied to the gate, a conductive sheet of negative charge (N-channel) is created in the surface of the substrate under the dielectric. (See para A.5.1 of Appendix A.)

**Nailhead bonding:** An alternate term for *Ball bonding*.

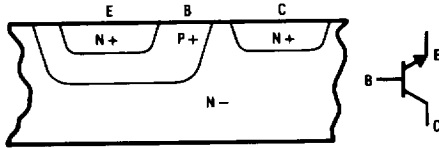
**Neutron radiation:** Exposure of a device to neutron radiation during fabrication in order to reduce minority carrier lifetime in the substrate. This minimizes the probability of circuit latchup during exposure to burst radiation.

**NMOS:** See *N-channel*.

**Non-destructive bond pull:** Pull stressing of all wires on all devices or a sample of devices from a given lot to a pull force which is lower than the minimum pull force limit imposed for destructive bond pull. (See MIL-STD-883, Method 2023.)

**Non-standard part:** A device procured to a contractor prepared specification rather than to a government prepared specification.

**NPN transistor:** A junction transistor constructed by placing a P-type base between an N-type emitter and an N-type collector. The emitter is normally negative with respect to the base and the collector is normally positive with respect to the base.



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**N-type:** Semiconductor material in which the majority carriers are electrons and are therefore negative.

**Operating life:** Burn-in (that is, exposure to high temperature with electrical bias applied) performed for extended duration (usually one thousand hours at 125°C). Normally a sample test. (See MIL-STD-883, Method 1005.)

**Oxide isolation:** The separation of circuit elements on a semiconductor device through the construction of a barrier oxide between the elements (not to be confused with dielectric isolation, in which the isolation passes completely under the circuit element).

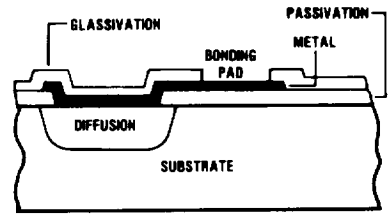
**Packaging density:** For integrated circuits, the number of semiconductor elements per unit area of chip size, frequently expressed in terms of number of gate equivalents.

**Parallel testing:** The testing of a number of devices at the same time (normally accomplished by mounting the devices on printed circuit boards which interface with the tester) as opposed to serial testing which tests one device at a time.

**Parasitic device or element:** An interaction between diffused circuit elements. A good example of a parasitic would be the collector series resistance ( $R_{SAT}$ ) of a transistor and the associated capacitance of the collector-to-substrate junction. In fact, the buried layer N+ diffusion is used to reduce collector resistance. The nature of current semiconductor technology makes it impossible to eliminate these parasitics. Where their effect on the circuit is significant, or when the circuit is designed to utilize these parasitics, they are shown on the schematic.

**Particle Count:** A measurement scale for gas or liquid cleanliness, normally stated in parts per cubic foot. For example, a Class 10 working area would be one which contained no more than 10 particles greater than one micron in size per cubic foot of air.

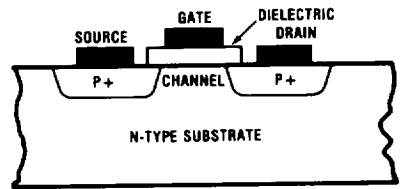
**Passivation:** The surface coating of the die (usually thermally grown silicon dioxide,  $SiO_2$ ) through which contact and diffusion windows are opened.



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**Passive device:** Devices such as resistors or capacitors which have no amplification or control characteristics.

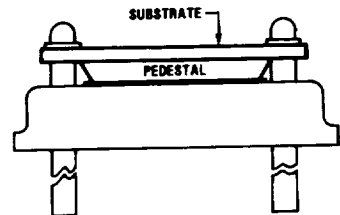
**P-channel:** An MOS process in which MOS transistors are formed by bridging two adjacent P-type diffusions (source and drain) with a dielectric (gate). When the source and the substrate are grounded and a negative voltage is applied to the gate, a conductive sheet of positive charge (P-channel) is created in the surface of the substrate under the dielectric.



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**PDA:** Perfect Defect Allowable: The maximum percentage of a lot which may fail a 100% screening step without rejecting the lot. The PDA is predicted on the possibility that a failure mechanism which appears in an abnormally high percentage of a lot might appear at a later time in the balance of the lot. It should, therefore, not be used for screens where all defective devices can be observed and removed (such as internal visual or X-ray).

**Pedestal:** The mounting portion of a hybrid substrate when it is smaller than the main portion of the substrate.



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**Peripheral device:** A device within a microprocessor device family whose function is required to support the operation of a CPU.

**Photolithographic process:** A technique utilized in the manufacture of microcircuits which uses light and selective masking to develop a fine-scaled pattern of areas of photoresist on the surface of the die.

**Photoresist:** A photosensitive material which, after polymerization through selective exposure to ultraviolet light, resists chemical etching action.

**PIND:** Particle Impact Noise Detection. A test performed by vibrating a device on a shock table with an acoustical sensor for the purpose of detecting loose particles within the device cavity (see MIL-STD-883, Method 2020). Other non-acoustical particle detection tests are specified in other documents.

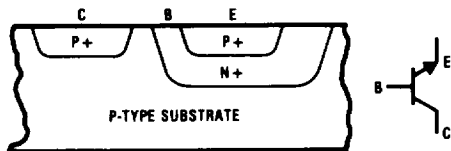
**Pinholes:** Small localized areas in the oxide layer with low dielectric strength, usually as a result of contamination.

**Pin-out:** The listing or diagrammatic description of the functions assigned to the various package pins of a semiconductor device.

**Planar structure:** A flat-surfaced device structure with the junctions terminating on a single plane.

**PMOS:** See *P-channel*.

**PNP transistor:** A junction transistor constructed by placing an N-type base between a P-type emitter and a P-type collector. The emitter is normally positive with respect to the base and the collector is normally negative with respect to the base.



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**Post:** See *Land area*.

**ppm:** Parts-per-million. A measurement scale for defect rates in components or impurity levels in materials.

**Precap:** See *Internal visual*.

**Probe:** Electrical test of semiconductor devices at the wafer level, so named because a metal probe is used to make electrical contact with each of the device's bonding pads.

**Procuring activity:** The government agency or original equipment manufacturer (OEM) that is responsible for placement and tracking of a given order for materials.

**PROM:** Programmable Read-Only Memory. A memory device whose stored data content is established on an individual device basis through a programming process (usually involving the blowing of fuse links on the surface of the die).

Unlike EPROMs and EEPROMs, PROMs cannot be erased and reprogrammed.

**Protective device:** A circuit element fabricated on a semiconductor device (usually adjacent to the device input) for the purpose of protecting portions of the device circuitry from transient overstress. A good example of a protective device would be an input diode on a CMOS device, which absorbs electrostatic discharge to prevent that discharge from rupturing the gate oxide.

**P-type:** Semiconductor material in which the majority carriers are holes and are therefore positive.

**Punch-through:** An unintended high current flow between two adjacent diffused areas created when sufficient voltage is applied to totally deplete both areas of majority carriers.

**Purple Plague:** See *Bimetallic contamination*.

**Qualification testing:** Testing performed one time only on a sample basis (see Appendix B of MIL-M-38510) to determine the suitability of a product or product family for usage against certain specifications or for certain programs.

**Qualifying activity:** The government agency or original equipment manufacturer (OEM) responsible for determining vendor qualification status with respect to a given specification or series of specifications. In many cases the qualifying activity will be different from the procuring activity.

**Quality:** Conformance to a set of predetermined design and workmanship standards. Quality and reliability are not synonymous.

**Quality conformance inspection:** Ongoing sample testing on a periodic basis to determine conformance with the quality and reliability standards established in Qualification. (See MIL-STD-883, Method 5005.)

**QPL:** Qualified Products List—A list of those suppliers and/or devices which have been qualified for a given program, specification or set of specifications. For further explanation of MIL-M-38510 QPL procedures, see Chapter 5.

**Radiation hardening:** Modification of the wafer fabrication process in order to improve a device's radiation tolerance characteristics.

**Radiation hardness:** The ability of a device to withstand radiation exposure without degradation or logic upset. Bipolar devices tend to be inherently harder than MOS devices.

**Radiation screening:** Testing of a device to determine its radiation tolerance (see MIL-STD-883, Method 2019).

**Radiation susceptibility:** The tendency inherent in a device to degrade as a result of exposure to radiation. MOS devices typically are more susceptible to radiation damage than bipolar devices.

**Radiography:** See *X-ray*.

**Rad (Si):** The quantity of any type of ionizing radiation that will impart 100 ergs of energy per gram of silicon.

**RAM:** Random Access Memory—A storage device in which the ability to access a randomly selected bit of stored data is independent of either the timing of the most recent access of that bit or the location of the most recently addressed bit. Data may be read nondestructively, but existing data is automatically erased when new data is written into a specific bit location. RAMs may be either static (that is, able to retain data when the power supplies are not biased) or dynamic (that is unable to retain data unless a "refresh" voltage is periodically applied).

**Read-and-Record:** The recording, by individual device serial number, of the actual parametric values measured for that device at a specific electrical test point. Read-and-record can be done for device characterization, drift (delta) measurement, or temperature coefficient computation.

**Rebonding:** The placement of a new bond on the same pad or post as a previously attempted bond. If the original bond has been removed, the new bond is still considered a rebond. A bond-off, that is, an extra bond placed at the edge of the post (never the pad) for the purpose of clearing the bonding machine, is not considered a rebond.

**Reject number:** For a sample test, the number of failed devices which will cause lot rejection. This will normally be one higher than the accept number.

**Reliability:** The anticipated lifetime of a device, how long it can be expected to "survive" in the user's system. This is normally defined as a failure rate (percent per 1000 hours) or as an MTBF (Mean Time Between Failures, expressed in hours).

**Resistance to solvents:** A test which requires immersion of sample devices in such solvents as trichlorotrifluoroethane and methylene chloride, followed by brushing to determine the durability of unit marking. (See MIL-STD-883, Method 2015.)

**RETS:** Rel Electrical Test Specification—A one page document used by National Semiconductor to detail the actual electrical testing for a given military device type.

**ROM:** Read Only Memory—A semiconductor device for storing data in permanent, nonerasable form, usually accomplished through the configuration of the metal mask pattern during wafer fabrication.

**Salt atmosphere:** Exposure of sample devices to a salt rich environment to determine long-term durability of the package materials (see MIL-STD-883, Method 1009).

**Sample:** A device or devices randomly chosen from a lot of material. Sampling assumes that randomly selected devices

will exhibit characteristics during testing that are typical of the lot as a whole.

**Sampling Plan:** A statistically derived set of sample sizes, accept numbers, and/or reject numbers which will confirm that a given lot of materials meets established AQLs or LTPDs.

**Schottky barrier:** A potential barrier formed between a metal and a semiconductor, frequently used in the creation of Schottky diodes.

**Screening:** 100% testing of a device, as opposed to sampling.

**Scribe grid:** The area separating two adjacent dice on a wafer through which the scribing tool will pass during the separation of the wafer into individual dice.

**Sealing:** The process whereby the lid is fastened onto a cavity (or hermetic) type semiconductor device. Sealing methods include solder (whereby a metal lid is soldered to a metal seal ring), weld (where a metal lid is welded to a metal package base), and glass (or ceramic) seal (where a ceramic lid is fastened to a ceramic base with reflowed glass).

**Selected item drawing:** Per MIL-STD-100, a drawing prepared for the purpose of procuring material which has been selected for parameters or characteristics differing from those to which the part is normally manufactured or tested.

**SEM:** Scanning Electron Microscope Inspection, which allows magnification several magnitudes higher than could be achieved with an optical microscope. (See MIL-STD-883, Method 2018.) A scanning electron microscope is typically capable of resolution to 250 Å or better and magnification of greater than 20000X.

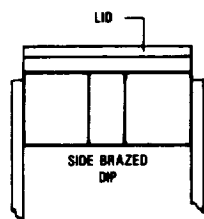
**Semiconductor:** An element, such as silicon or germanium, that is the intermediate in electrical conductivity between the conductors and the insulators.

**Serialization:** Application of a unique alphanumeric identifier to each unit of a lot of devices to afford traceability to variables data, individual radiographs, etc.

**Ship-to-stock:** A system whereby a component user develops a statistical evaluation of the quality of his vendors' products, enabling him to use the products of those vendors whose quality is acceptable without performing additional product testing upon receipt at his plant.

**Shrink:** The reduction of die size through conversion to a process within the same basic process family, but with smaller feature sizes.

**Side brazed dip:** A dual-in-line package with leads brazed to feedthroughs on the side of the package. Leads will normally come straight down rather than at angles as on other dual-in-line packages. No molded versions of this package are available.

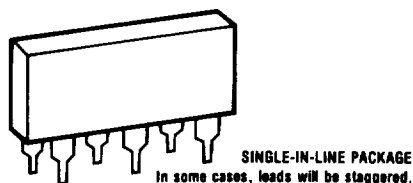


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**Silicon gate:** An MOS process fabricated with a polysilicon material as the gate electrode.

**Simple hybrid:** A hybrid device having an inner seal perimeter (i.e., a cavity perimeter) of less than 2 inches.

**Single-in-line package:** A package (either hermetic or molded) with all its leads emanating from one side of the package.



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**SIP:** Abbreviation for single-in-line package.

**Skip bond:** A bond placed between two metallization traces on a hybrid substrate.

**Slash sheet:** A MIL-M-38510 detail device specification giving the specific screening and electrical test requirements for a device or family of related devices (see Chapter 5). In a MIL-M-38510 part number, the first three digits after the slash indicate the slash sheet number. For example, M38510/02004 BDB would be device type 04 specified on slash sheet 20. (Note that a zero is prefixed to two digit slash sheet numbers and two zeros to one digit slash sheet numbers to create uniform 15-digit part numbers.)

**SMP:** See *Surface mounted packaging*.

**Soft error:** An error of a nonpermanent nature introduced into a cell or cells of a memory device as a result of either voltage or current transients or radiation exposures. Although soft errors may be corrected, the data previously stored in the cell may not be retrievable.

**Software:** The instructions which program or sequence the functioning of the hardware of a device or system. These instructions may be contained internally (in ROM, for example) or externally (on tape, disc, or any other suitable memory medium).

**Solderability testing:** Immersion of the leads of sample devices in solder, followed by visual inspection to determine that the quality of the finish is such that it will accept an even coating of solder. (See MIL-STD-883, Method 2003.)

**Solder dip:** Dipping of the leads of devices into molten solder in order to later facilitate soldering of the devices to circuit boards. Sometimes inaccurately referred to as "tin dip."

**Solder seal:** Semiconductor device sealing accomplished by soldering a metal lid to a metal seal ring.

**Source control drawing:** Similar to a specification control drawing except that purchase of the specified devices from manufacturing sources other than those listed on the drawing is prohibited.

**Source inspection:** Surveillance or inspection by a customer's quality representative or by a government inspector at the vendor's facility of material being assembled or screened by that vendor.

**Specification control drawing:** Per MIL-STD-100, a drawing prepared for the purpose of defining and controlling screening, electrical performance characteristics, and physical configuration of purchased material. By definition, the intent of a Source Control Drawing is to purchase controlled standard parts.

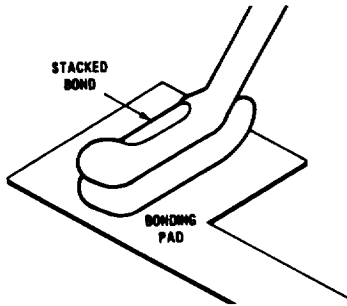
**Sputtering:** A method of producing thin films by freeing molecules from a solid source through ionic bombardment in order to deposit them on a nearby surface.

**SQC:** See *Statistical quality control*.

**SSI:** Small Scale Integration. SSI devices are those that contain less than 12 gate equivalents.

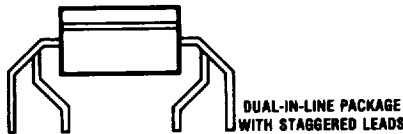
**Stabilization bake:** Placement of devices in a chamber at elevated temperature (normally 150°C) without electrical bias in order to test the construction of the devices. Sometimes this is performed prior to seal in order to bake out impurities on the die surface. (See MIL-STD-883, Method 1008.) Stabilization bake differs from high temperature storage only in that it is typically of shorter duration.

**Stacked bond:** A rebond placed directly over a previous bond.



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**Staggered leads:** Leads emanating from the same side of a package but bent in alternating directions such that they will insert into two or more parallel lines of mounting holes.

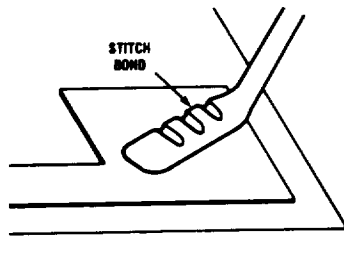


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**Static RAM:** See *RAM*.

**Statistical quality control:** A quality control system utilizing statistical analysis of process defect data to detect quality trends on a real time basis.

**Stitch bonding:** A bonding technique whereby the tip of the bonding wire is fed under the bonding head, which then applies heat and pressure to "stitch" the wire to the pad or post. Frequently several stitches will be employed on the same bond. Stitch bonding can be visually differentiated from ultrasonic bonding because the impressions normally run across the bond rather than along its length.



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**Substrate:** The physical material upon which an integrated circuit is fabricated or assembled. For a monolithic device,

this would be the silicon of the chip; for a hybrid it would be the alumina or ceramic surface upon which the die and other elements are deposited.

**Substrate bond:** See *Skip bond*.

**Surface mounted packaging:** Semiconductor packages mounted on the surface of a printed circuit board or other substrate material. (See also *Through-hole mounting*.)

**Surface states:** Extra donors, acceptors, or traps, usually undesired, which may occur on a semiconductor surface because of crystal imperfections or contamination. These may vary with time.

**Surveillance:** Random witnessing of testing or screening of devices to determine that the material meets all applicable requirements.

**Temperature cycle:** A test whereby devices are stored for short periods (15 minutes) alternately at high and low temperatures in gas filled chambers, with a maximum transfer time between chambers of one minute. Normally 10 cycles are performed from  $-65^{\circ}$  to  $+150^{\circ}\text{C}$ . This stresses device assembly because of the different thermal coefficients of expansion of the various materials used. (See MIL-STD-883, Method 1010.)

**Thermal resistance:** Normally stated in terms of  $^{\circ}\text{C}/\text{W}$ , it is the indicator of the package's ability to dissipate the heat generated by the chip during operation.  $\theta_{\text{JC}}$  is the indicator of the chip's ability to pass the heat generated by the semiconductor junctions to the package, that is the thermal resistance between the semiconductor junction and the case;  $\theta_{\text{JA}}$  is the thermal resistance between the semiconductor junction and the ambient environment, or the indicator of the case's ability to pass chip heat into the ambient air.

**Thermal secondary breakdown:** Burnout of a semiconductor junction area as the result of a reverse-bias voltage or current induced thermal runaway condition.

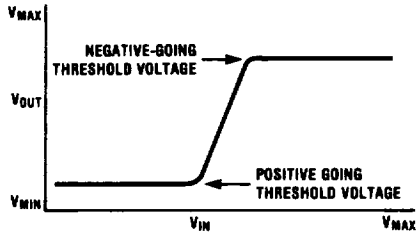
**Thermal shock:** Similar to Temperature Cycle except that the environments are liquid, and the transfer is immediate. Normally performed for 15 cycles from  $0^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ , this is a much more severe stress of the package seal and is normally employed only on a sample basis (see MIL-STD-883, Method 1011).

**Thermocompression bonding:** See *Ball bonding*.

**Thick film:** Any coating thickness greater than  $5\mu$  ( $5 \times 10^4 \text{ \AA}$ ), typically formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern.

**Thin film:** Any coating thickness less than  $5\mu$  ( $5 \times 10^4 \text{ \AA}$ ), typically formed by vacuum depositing or sputtering.

**Threshold voltage:** The voltage level at which a device will recognize a falling or rising voltage as a change in logic state.



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**Through-hole-mounting:** A mounting technique for semiconductor packages in which the device leads are passed through holes in the mounting surface. Attachment of leads may be accomplished with solder or with other mechanical means.

**Tin dip:** A term commonly misapplied to the solder dipping of device leads (see *Solder dip*).

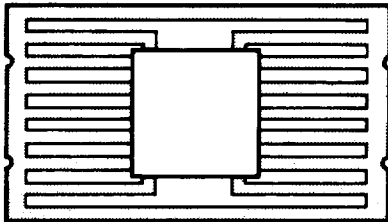
**Total dose:** The total accumulated amount of absorbed ionizing radiation specified at a particular dose rate exposure at +25°C.

**Transportability:** Those characteristics of hardware or software which allow its transferral from one system to another system and to interface compatibly with the hardware and software of the new system.

**Triboelectric effects:** The creation of electrostatic charge that occurs when two surfaces contact and then separate, leaving one positively charged and the other negatively charged (see Chapter 10).

**Trim and form:** The step in the assembly process for devices assembled on a lead frame (such as flatpacks and dual-in-line packages) where the lead frame is trimmed off and the leads bent or formed into their specified positions.

#### Untrimmed Leadforms



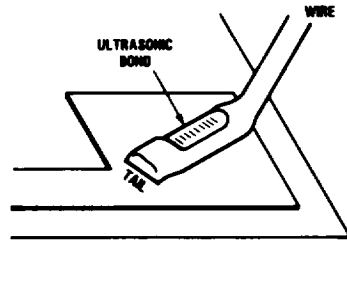
14 PIN FLATPACK

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**Truth table:** For a logic device, a table showing the output logic states that would result from each of the possible input logic combinations the device is designed to accept.

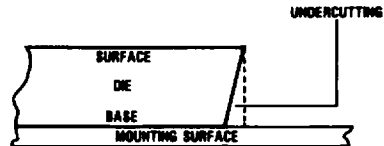
**ULSI:** Ultra Large Scale Integration. A term applied to devices with complexity levels in excess of 10,000 gates.

**Ultrasonic bonding:** A bonding technique which utilizes a bonding head to apply ultrasonic vibration to the bonding wire and to convert the vibration to heat through pressure and through the friction between the wire and the pad created by the scrubbing action of the head. Since this technique requires no external heating, it results in minimal oxidation of aluminum bond wire and bonding pads. Used normally with aluminum wire, this is the most commonly employed bonding technique.



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**Undercutting:** Inward sloping of die metallization or silicon such that its upper surface is wider than its base.



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**Unipolar:** Devices or processes in which current carrying areas and substrates are of similar polarities, usually MOS devices.

**Variables data:** Recorded parametric or delta values, traceable to individual devices, as opposed to lot data (or attributes data).

**VHSIC:** Very High Speed Integrated Circuits. The acronym applied to the Department of Defense sponsored research and development program to advance the state of the art in semiconductor device speeds, densities, power consumption, and system effectiveness. (See Chapter 7 for more detail.)

**Vibration, variable frequency:** A test which applies vibration to devices on a sample basis (since it is considered destructive) in order to subject them to the maximum possible construction stress. The device is vibrated with simple harmonic motion through a range of frequencies (see MIL-STD-883, Method 2007).

**VLSI:** Very Large Scale Integrated Circuits. VLSI devices are generally accepted to be those that contain more than 1000 gate equivalents, but less than 10,000.

**Wafer fabrication:** The process whereby semiconductor elements are manufactured on the surface of silicon wafers.

**Wafer lot:** A single lot of wafers processed through all processing steps including metallization together. A wafer run may consist of more than one device type, where the various device types differ only in the metallization pattern employed.

**Wafer lot acceptance testing:** Testing of an integrated circuit wafer lot to determine its acceptability for the assembly of Class S devices (see MIL-STD-883, Method 5007).

**Wafer probe:** See *Sort*.

**Wedge bonding:** See *Ultrasonic bonding* (although *Stitch bonding* is occasionally called wedge bonding as well).

**Weld Seal:** Semiconductor device sealing accomplished by welding a metal lid to a metal package (typically employed for metal can devices).

**Yield:** The total number of devices which are electrically and mechanically within applicable specifications, expressed as a percentage of the total population.

**X-ray:** Radiographic analysis of the construction of a device. This is a less useful technique for devices with aluminum bond wires since only die attach and seal defects can be evaluated. For devices with gold wire it is a more valuable screen as it can detect damage done to wires during centrifuge and other such tests, as well as most assembly defects. (See MIL-STD-883, Method 2012.)