Using At-Speed BIST to Test LVDS Serializer/Deserializer Function

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Abstract

LVDS is the acronym for Low-Voltage-Differential-Signaling and is described in both the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. High performance yet Low Power and EMI have made LVDS a popular choice for high-speed card-to-card serial links. A typical application is the serializer/deserializer (ser/des) function where wide TTL datastreams including clock is converted to a serial LVDS bit stream, sent over a cable, and deserialization and clock recovery performed on the receiving card. This is a powerful design technique but presents interesting challenges from a testability perspective. First, LVDS links have a much different fault spectrum than the well-established stuck-at models used for TTL logic levels. The LVDS interconnect is a transmission line model, where the signal carrying integrity of the cable, fault models and fault detection are very frequency dependent. In addition, the Ser/Des function with clock recovery requires the two devices to achieve synchronization, so efforts to test the link and ser/des functionality must meet the timing requirements of the internal logic. Ideally, any built-in-test capability for the link should be accessible via the JTAG port to take advantage of the existing industry tools and infrastructure.

This paper describes a JTAG activated at-speed BIST technique used to test a high-speed ser/des chip set and cable.

1. Introduction

The IEEE 1149.1 standard [3, 4] has proven highly effective as a tool for identifying and diagnosing manufacturing defects. These defects often result in gross opens and shorts, faults readily detected with ATPG (automated-test-pattern-generation) interconnect tests. Since IC design and board layouts are generally not optimized for high-speed boundary scan testing, such tests are typically run with a JTAG clock rate (TCK) less then 15 MHz. The detected fault spectrum is therefore considered to be DC faults. As adoption of the standard has become pervasive, users have discussed the advantages of extending the capability of the standard to include AC testing and delay faults. AC or delay testing would expand the fault coverage of IEEE 1149.1 and reduce the incidence of test escapes and NFF (No-Fault-Found). As described in [5] and [6] proposals have been made to modify the boundary scan registers and TAP to incorporate AC test capability into the standard.

Differential signaling is an area where boundary scan is not yet well established. As described in [7] and [8], the differential pair can be treated as a single signal or each of the lines can be considered individually. Each approach has advantages and disadvantages. However, the inadequacy of existing techniques to test High-Speed Differential Signals has been recognized. This is particularly true if the differential lines are AC coupled using capacitors, which is a common practice. At the time of writing this paper, an industry-working group is evaluating various proposals for adding an AC-EXTEST instruction to IEEE 1149.1. At present however, there is no established standard for AC boundary scan testing. Thus our challenge was to develop a test solution that would be compliant to the IEEE 1149.1 standard, yet provide at-speed testing of a differential medium, and the associated PLLs and logic.

From a system test standpoint, high-speed serial links provide an interesting challenge. There are three distinct areas where faults can occur, those being the

ICs, the connectors and the interconnect (e. g., a cable). The cable represents the transmission line environment, and in addition to actual hard defects, the cable quality may be insufficient for the high data-rates, typically in the hundreds of Mbit/s required. A marginal cable will result in intermittent failures and poor Bit-Error-Rates, (BER), the types of faults that are most difficult to detect and diagnose. Likewise, a multidrop or multipoint backplane with long stubs to the inputs on each card may effectively reduce the bandwidth of that interconnect below what is required for a safe operation [8]. Interconnect faults of the opens and shorts variety are more tangible and repeatable but in the case of high speed differential signals may be masked by the transmission line environment and the inherent fault tolerance of LVDS. The ICs are the third potential source of faults, and in the case of the popular serializer/deserializer (ser/des) function there is a considerable amount of complexity in the coding and decoding logic. In addition, embedding the clock and performing clock recovery requires critical timing and introduces other factors such as jitter. The most difficult condition to diagnose is the interaction of a marginal IC and a marginal cable resulting in non-repeatable intermittent failures. When developing a built-in-test solution for an LVDS ser/des chip set, the goal was to consistently detect all of the faults that would impair the performance of the chipset, and make the test compatible with the pervasive IEEE1149.1 JTAG test standard.

As we will describe, in a differential transmission line environment, the purpose of the test is not only fault detection but also ensuring operation at system speeds with acceptable bit-error-rates.

This paper will briefly describe LVDS technology, then review the various approaches to adding IEEE1149.1 to differential signals, describe the BIST technique we decided on, then present and discuss the actual test results.

2. LVDS Basics

LVDS is the acronym for Low-Voltage-Differential-Signaling which is described in both the ANSI/TIA/EIA-644 [1] and IEEE 1596.3 standards [2]. As the name implies, LVDS is a differential technology with very small signal swings. As a data communication standard, LVDS combines high data rates with low power consumption, low EMI emissions and excellent noise immunity. Hence its rapid increase in popularity as a signaling technology. As shown in Figure 1, in a basic point-to-point configuration, LVDS consists of a constant +/- 3.5mA current source that drives the differential pair. The receiver has high input impedance; therefore the 100-ohm termination resistor results in approximately 350 mV across the receiver inputs. The receiver is extremely sensitive and typically will respond to a differential of considerably less then 100 mV.

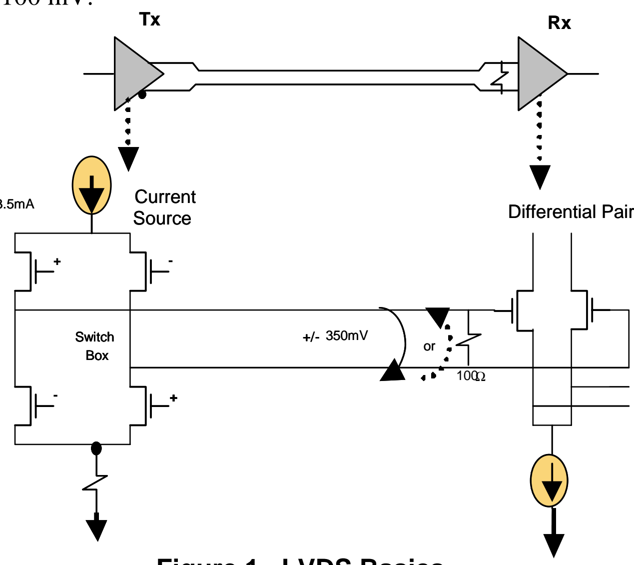

Figure 1. LVDS Basics

3. LVDS with IEEE1149.1 (JTAG)

How to best handle differential signals under the umbrella of the IEEE1149.1 (JTAG) standard, has been a point of discussion for some time. One approach is to consider both polarities of the differential pair as a separate signal and have a boundary Scan register for each of them. Potentially this could provide better resolution of faults but is complicated by the need to add digital test circuitry in the signal path of the very high performance analog transmitters and receivers. The added capacitance and potential source of noise is most unwelcome in the highly tuned LVDS circuitry. A second approach, more common and used in this particular device, considers the differential pair as a single channel and the boundary scan registers are "behind" the transmitter and receiver.

Many LVDS devices include a failsafe circuit in the receivers (see Figure 2), which provides a small weak voltage across the terminals. Since the receiver is very sensitive, the failsafe circuit is intended to prevent potentially destructive oscillations in the inadvertent event of no driver current, and therefore no voltage, across the receiver inputs. By introducing a known polarity in the event of no signal, the failsafe circuit can contribute to test escapes. For example, examining Figure 1, if the pull-up transistor in the + polarity is defective, the circuit could still pass a 1's and 0's test done at low speed. A low (0) would be driven by the

LVDS driver, and when the polarity was reversed, the high (1) would be provided by the failsafe circuit. Of course the failsafe would not be sufficient to operate at system speed.

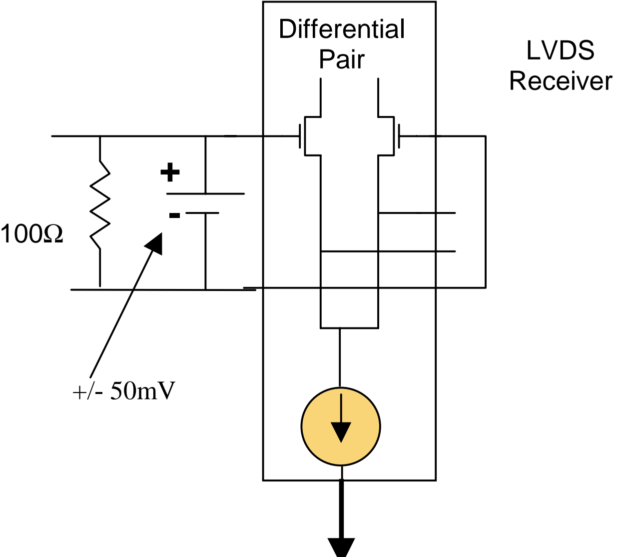

Figure 2. Failsafe

Although LVDS was initially developed for point-to-point, a variation of LVDS suitable for multi-point applications is also available and known as Bus LVDS. Bus LVDS has higher drive current, approximately 10 mA to provide the same +/-300mV swing as standard LVDS for a heavily loaded multipoint or multidrop bus that may have an effective impedance as low as 27ohms [9, 10].

4. LVDS Faults

LVDS is an extremely robust technology, and properly terminated and using appropriate media can operate at data rates well beyond 1Gbit/s. The technology is inherently fault tolerant. As the transmission environment deteriorates, due to factors such as non- optimized terminations or the introduction of faults, the signal quality and bandwidth degrade gradually. Eventually the circuit will become completely inoperable, however this is only in the event of the most severe interconnect problems. For this reason the preferred test solution is performed at-speed and with sufficient data payload to ensure mission mode operation.

The fault spectrum for differential signaling, such as used in LVDS, is considerably different than for single-ended technologies. Consider the faults shown in Figure 3. Faults F1, F2 & F3 are on the TTL side of the device and represent the standard opens and shorts expected in a stuck-at model. These faults are well understood and readily detected with standard ATPG patterns run at typical TCK speeds. However, consider F4, a short to Vcc or Gnd. This fault would certainly reduce the maximum potential performance of the chipset. But, due to common mode rejection and the sensitive receiver only requiring tens of mVs to switch, it is quite likely the LVDS link would still function, albeit only at a substantially reduced frequency.

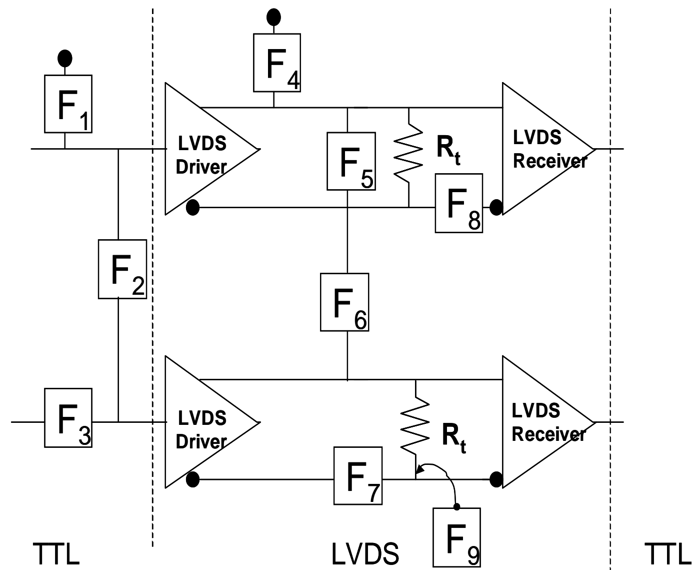

Figure 3. LVDS Faults

This type of fault would likely be missed by standard ATPG patterns run at TCK speeds. Another example is F9, which can be an out-of-tolerance, incorrect or missing resistor. Optimum performance is obtained with the correct termination resistor, while the wrong value will lead to either reduced noise margins (too low a resistor) or reduced bandwidth (too high a resistor). Once again this type of fault could pass typical ATPG patterns run at low speeds. Even F7, an open circuit on a single line, might escape detection depending on the transmission line characteristics of the cable, and the Tck frequency at which the test was conducted.

5. Serializer/Deserializer (Ser/Des) Function

A powerful application of LVDS is the ser/des function, where parallel TTL data-streams are serialized and converted to LVDS for card-to-card transmission, then deserialized and converted back to TTL. To minimize clock skew, in some cases the clock is also embedded in the serial data and then recovered at the

receiver. The chipset discussed in this paper is the SCAN921023/921224 from National Semiconductor [11], which is a 10 to 1 ser/des with embedded clock.

When providing testability for the chipset, standard IEEE1149.1 was included on the TTL pins, and the LVDS differential pair was treated as a single bit and included in the boundary scan register. However as we have discussed, standard ATPG patterns generated for TTL networks and run at TCK speeds, will not detect many of the faults likely to impair the performance of the LVDS link. To ensure operation at system speed, it was determined that additional LVDS testing needed to be performed at system clock frequencies, and for sufficient duration, to verify the transmission media and the respective encoding and decoding circuits.

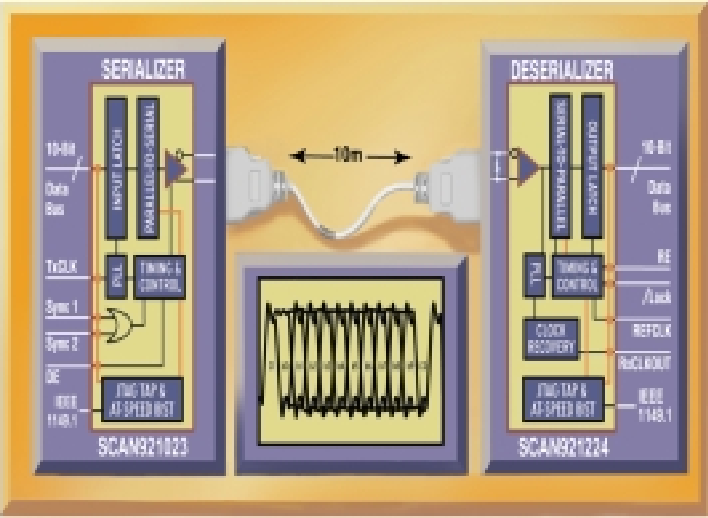

Figure 4. BIST test setup

Therefore the following BIST scheme was decided upon (see Figure 4 above) a RUNBIST command is simultaneously executed in both the transmitter and receiver, where either of the transmitter or receiver could be test equipment containing a golden unit, or another board. A RUNBIST initiates the synchronization sequence followed by pseudo-random pattern generation (PRPG) in both devices. After sync is established, the pseudo-random patterns are serialized along with the system clock, transmitted over the LVDS link, and then deserialized at the receiver and compared to the expected result. A standard 10-bit PRPG was selected [12]. Patterns are generated for 2k clock cycles and then repeated until the test is complete. As a compromise between test duration and suitable Bit-Error-Rate, enough bits are transmitted such that a passing test guarantees a BER of 10^{-7}. This results in a test time of approximately 33 ms at 20 MHz clock rate. Two bits are used to monitor the test, TEST_COMPLETE and a PASS/FAIL bit. After completion of the test these bits are then shifted out through the JTAG chain. This approach provides a comprehensive test of the entire chipset, since the test verifies the sync generation, data serialization and embedding of the clock in the transmitter, the integrity of the interconnect, and also the PLL, decode logic and clock recovery in the receiver.

6. Evaluation of BIST

To verify the operation of the BIST circuit and compare its results to standard open/shorts tests, an evaluation board was built with the ability to introduce faults. Common faults were considered, those being an open at the connector/cable, short at the connector/cable and missing termination resistor. (See Figure 3, F4, F7, F9.) Missing termination resistor also represents the incorrect (and >>larger value) resistor case, as resistors significantly larger then the 27 ohms recommended produce similar results to the missing resistor condition. The transmission media used was approximately 3 feet of category 5 cable.

The methodology was very straightforward. The circuit was tested at speed and verified as good. Then a fault was introduced and tests were run to establish if the fault could be detected by either static interconnect tests or at-speed BIST. First interconnect tests were run using patterns of ones and zeros and then the at-speed BIST was exercised.

7. Discussion of Results

Table 1 provides a summary of the faults evaluated and the results of both the standard interconnect tests and the at-speed BIST. As would be expected, the inter-connect tests detected the gross failures such as no cable and reversed polarity on the cable. In addition, some conditions of open and short circuits were detected. However, faults associated with the termination resistor passed, such as wrong or missing resistor. In addition certain open and short conditions escaped detection, such as open on the positive terminal of the driver cable and short to Ground in the positive channel in the cable. Note that the opens/shorts testing was not exhaustive or quantitative and hence should not be generalized. Testing was done to the extent of proving that certain conditions would consistently

Table 1. Summary of Fault Conditions & Results

generate a pass or fail. At the time of writing this report there were too many variables to attempt to accurately

Fault	IEEE 1149.1 Opens/Shorts	At-Speed BIST @30 MHz	At-Speed BIST @ 45MHz
No Connector	Detected	Detected	Detected
Polarity Reversed Connector	Detected	Detected	Detected
Open + Terminal of Transmitter	Not Detected	Detected	Detected
Open – Terminal of Transmitter	Detected	Detected	Detected
Short + Terminal of Transmitter	Not Detected	Detected	Detected
Short – Terminal of Transmitter	Detected	Detected	Detected
No Termination Resistor	Not Detected	Not Detected	Detected

quantify what precise conditions were necessary to establish a pass or fail.

As we had hoped, the at-speed BIST detected the gross interconnect faults as well as more of the resistor faults and opens/shorts which had escaped detection with simple interconnect patterns. However, the at-speed BIST is a functional test, and will in some cases pass, even with defects such as incorrect termination resistor. The test verifies successful transmission of a data payload with zero errors, but does not guarantee function at higher clock speeds.

Figures 5, 6 and 7 are scope plots of three test conditions.

Figure 5 represents the no-fault set-up. The upper signal is the 45 MHz clock and the lower signal is the LVDS data-stream. As expected, the signal swing is several hundred mV and the data exhibits clear so-called eye patterns, indicating a properly terminated signal with low noise and jitter.

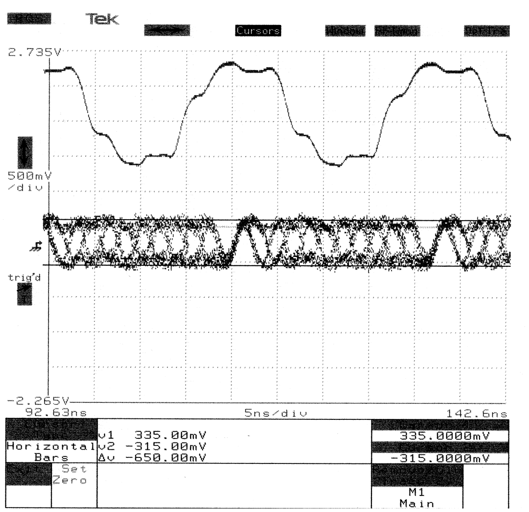

Figure 5. No-fault set-up @ 45MHz

In Figure 6, the termination resistor has been removed. (See Figure 3, F9.) Without any load, the signal swing is the full rail of the drivers, approximately 2 volts. The correct signal is still being transmitted, however the large swing is causing distortion to the eye patterns. Nevertheless, at a 30 MHz clock rate the chipset is passing BIST with no errors. Above this frequency the test fails, significantly below the guaranteed (with proper termination) 66 MHz max clock frequency specified for the chipset.

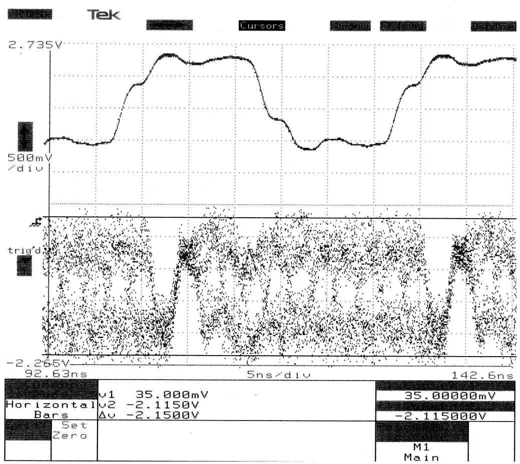

Figure 6. Missing Rt@30MHz

Figure 7 is the same set-up but with a clock frequency of 45MHz. Here the signal distortion is too great and BIST is failing.

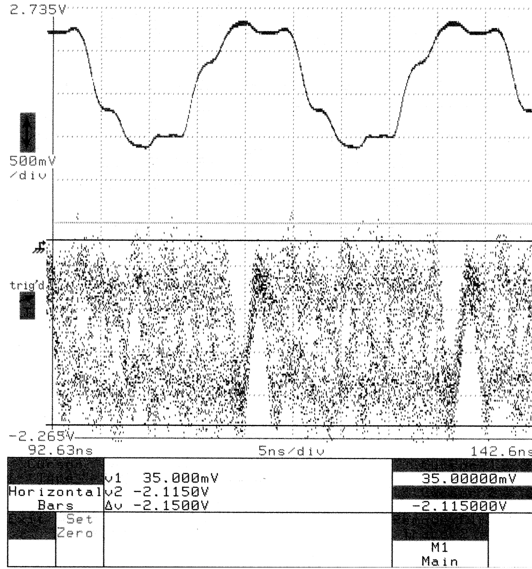

Figure 7. Missing Rt@45MHz

8. Summary and Conclusions

Differential signaling technologies such as LVDS present unique challenges to automated boundary scan testing. Transmission line effects and failsafe circuits can combine to defeat interconnect tests generated using stuck-at models. IEEE1149.1 type interconnect tests will detect gross faults and some percentage of shorts and opens on a single line of the differential pair. Interconnect tests will not detect missing or incorrect resistor faults.

At-Speed BIST combined with Bit-Error-Rate testing will detect most additional faults which escaped detection during interconnect tests.

Interconnect tests alone are insufficient in detecting all common manufacturing defects or predicting performance at system speed. Interconnect tests combined with an at-speed BIST test is an effective way to detect manufacturing defects and ensure error free transmission at system speed. Moreover, we have shown that 1149.1 supported test can be expanded to cover interconnect between two boards. This can be seen as a 'first step' towards System level testing, while still adhering to 1149.1 rules and with this consequently be able to rely on support from ATPG tools and vendors.

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