National Semiconductor
Hi-Rel Operations Radiation Engineering/RHA Programs
2900 Semiconductor Drive
Santa Clara, CA 95052

Single Event Effect Report

Micro Power
12 b Digital to Analog Converter

DAC121S101WGRQV
(5962R0722601VZA)

Date: August 9, 2010
Rev: C (updated product numbers and added Weibull fit parameters)

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PowerWise

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I. Abstract

The DAC121S101WGRQV was evaluated for Single Event Latchup (SEL), Single Event Functional Interrupt (SEFI), and Single Event Transients (SET) due to heavy-ion strikes. The DAC was found to be immune to SEL and SEFI at the highest tested linear energy transfer (LET) tested, which was120 MeV/mg/cm^2 for SET and 99 MeV/mg/cm^2 for SEFI. The worst case SET cross section over the entire range of ion energies and operating conditions was calculated at 4.24×10^{-4} cm^2. The longest transient lasted 4220 ns and the maximum transient amplitude was +1.6 V. The transient amplitude and lengths were highly dependent on the operating conditions, supply voltage and input code. The total outage time due to single-event induced transients for the DAC was 47.7 ns/month. The total number of events/month was 1.13×10^{-2}.

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II. Product Description

Main Characteristics: The DAC121S101WGRQV is a full-featured, general purpose 12 bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7 to 5.5 V supply and consumes just 145 µA of current at 3.6 V [1]. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 20 MHz over the specified supply voltage range. The supply voltage (V_A) for the DAC121S101WGRQV serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than one µW.

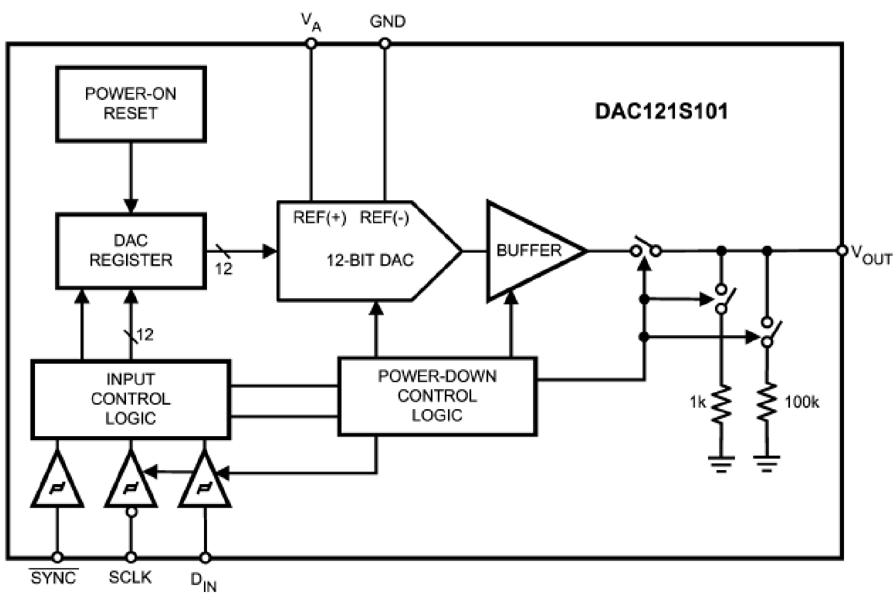

Fig. 1 Block Diagram of DAC121S101WGRQV

Pins: As shown in Fig. 1, serial data input (through D_{IN}) is clocked into the 16-bit DAC registers (12 for the data, 2 for power down options and 2 don't care) on the falling edges of SCLK. The DAC is updated on the 16th clock cycle. The code and output are held until the $\overline{SYNC}$ pin is toggled high and then low and another 16 bits are clocked into the D_{IN} pin.

Functional Blocks: The DAC section is fabricated on National's 0.5 µm CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The conversion section consists of a string of equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The switches are operated by the code loaded in the DAC registers. The buffer amplifier (rail-to-rail type) stage is followed by the switch resistor combinations of the power down stages, enabling 3 different power down modes (1 KΩ, 100 KΩ and high impedance) – determined by the 13th and 14th bits of the DAC registers.

III. Test Method

Testing was done according to JESD57 (EIA/JEDEC Standard No. 57), "Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation" [2].

A. Test Circuit:

The devices under test (DUT) were DAC121S101WGRQV die assembled into 8 pin open cavity plastic packages, with no lid to expose the die surface to the ion beam. Each decapped unit was soldered to a separate DAC121S101EVAL Board (Fig. 2) [3]. The jumper on each board was set so that the DUT would be directly powered by a dedicated power supply in order that the current could be monitored during testing for SEL detection. The output capacitor on the evaluation board for AC coupling was replaced by a short circuit for the DC test.

Fig. 2 DAC121S101EVAL Board

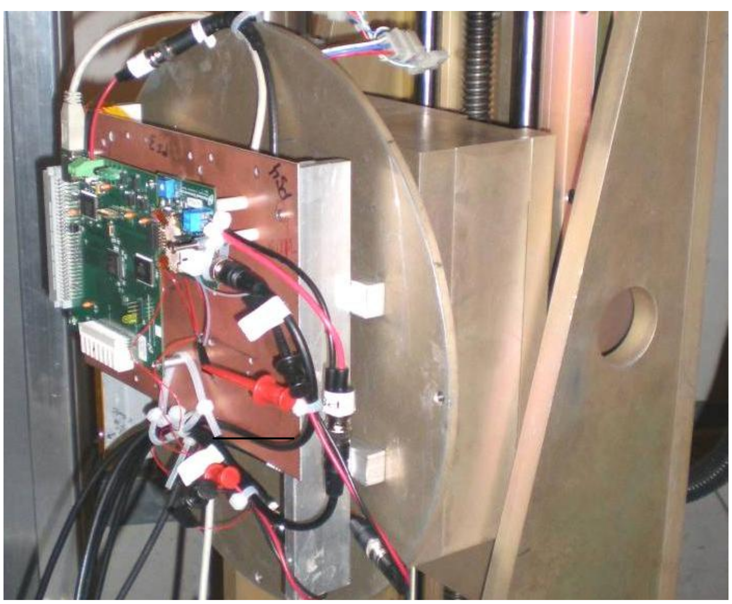

Fig. 3 DAC121S101EVAL and WaveVision boards inside the vacuum chamber

The DAC121EVAL boards were connected to and driven by a WaveVision board and WaveVision4 software (Fig. 3) [4]. The WaveVision board supplies the input clock, and sync signals, along with the input code.

The SEL and SET testing were done in a dynamic mode. The input clock was set to 20 MHz. The SYNC pin was toggled high and then low every 1 μs for a sample rate of 1 MS/s. For the SEFI test, the part was tested in a static mode where the code was inputted once and never updated.

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B. Test Setup:

B1. SEL and SET Power Supplies:

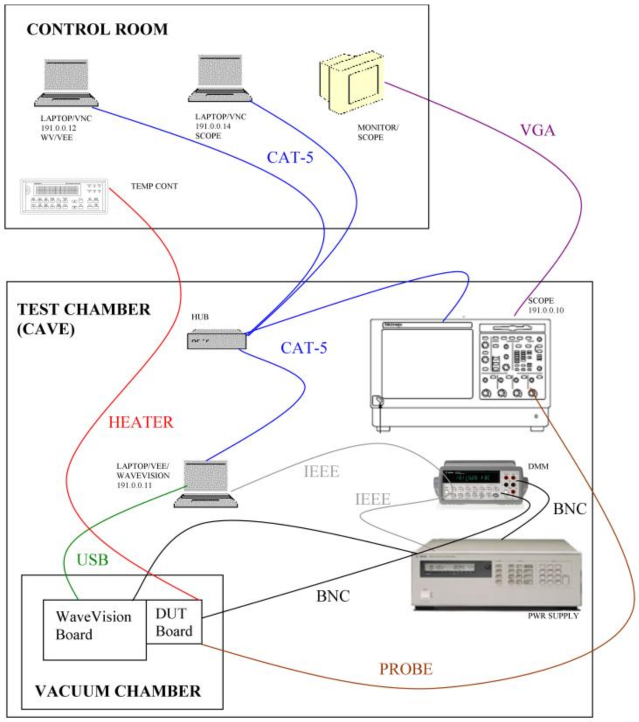

Fig. 4 Equipment setup for SEL and SET testing

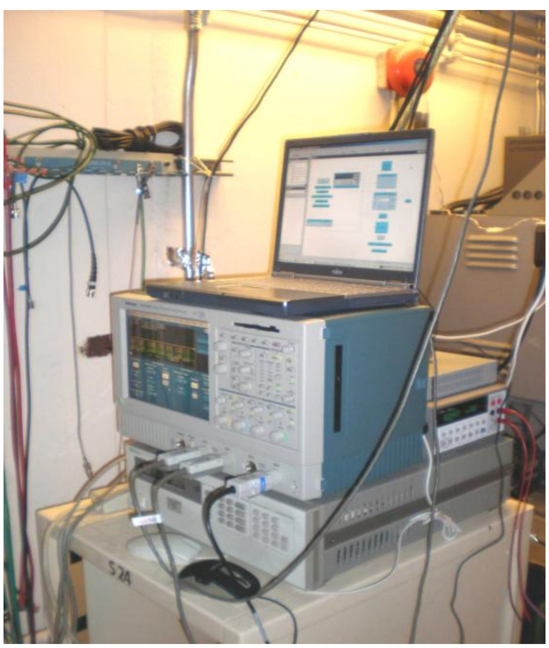

Fig. 5 Measurement setup in the test chamber

The DUT was powered by an HP 6624AP power supply. The input current was monitored through the Agilent 34401A and both instruments were interfaced to the monitoring laptop computer using an IEEE 488 digital communications bus (Fig. 5). The monitoring laptop was controlled by remote access (though a hub) from a second computer in the control room. The power up and power down sequences were executed using Agilent VEE Pro's software routines, minimizing the necessity of physically accessing the test chamber. Supply voltage level to the DUT was verified by measuring voltage at the DAC121S101EVAL V_A input before the vacuum chamber was sealed.

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Observation of normal operation of the DAC over the entire range of operating conditions had shown the maximum input current to be less than 3.5 mA. Any sudden operating current increase of more than 10 µA would be considered a latchup condition. In addition to manual monitoring, a software routine was written in VEE Pro 8.0 to automatically power down the device in case of Single Event Latchup (increase in operating current above 3 mA).

For elevated temperature testing, a resistive heater was attached to the backside side of the DAC121S101EVAL board, directly under the DUT. A thermister was epoxied close to the DUT to monitor the board temperature. The thermister and heaters were connected to a Lakeshore temperature controller.

B2. SEFI Power Supply:

The DUT was powered by an HP6114A precision power supply and the current was monitored by a Fluke 8050A multimeter. The power supply and multimeter were located in the control room and connected to the DUT through 25 feet of cable. Supply voltage level to the DUT was verified by measuring voltage at the DAC121S101EVAL V_A input before the vacuum chamber was sealed. Any sudden operating current increase of more than 10 µA would be considered a latchup or possible SEFI condition.

B3. Output Monitor:

The output of the DUT was connected to either a Tektronix TDS 5104B or 7404B oscilloscope, depending on the test date. The scope, which was located in the test chamber, was also interfaced to the network through a IEEE 488 digital communications bus and controlled by a third laptop located in the control room. The scope output was viewed through a remote monitor located in the control room.

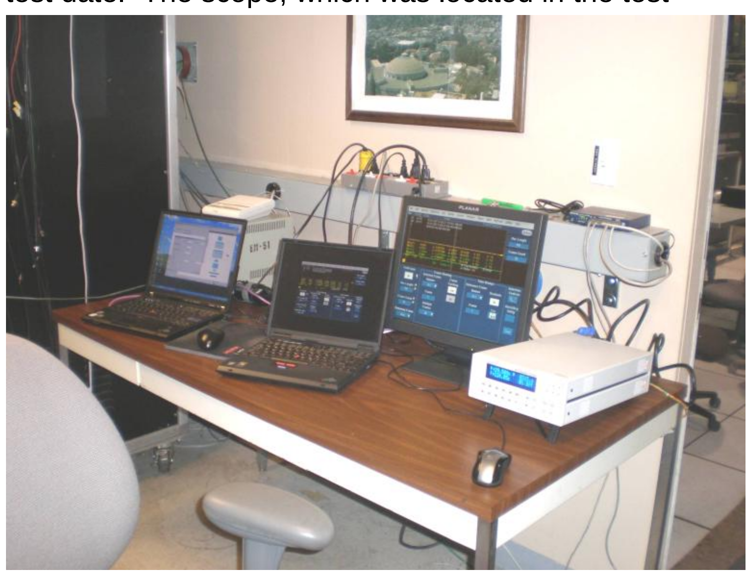

Fig. 6 Setup in the control room

For the SET monitoring of DUT 1, a Tektronix TDS5104B 1 GHz scope was used in “high resolution” mode. This allowed for the most sensitive detection of a transient, while still allowing for the full amplitude range of the transient to be displayed and recorded. A TDS7404B 4 GHz oscilloscope was used in the SET and SEFI testing of the DUT 2 and 3. This scope would not capture transients in a “high resolution” mode and had to be set to a higher screen resolution. This caused the measurement and recording of any transients higher than 0.43 V to be truncated at 0.43 V. However, the higher speed TDS7404B

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scope did capture some shorter transients that appeared to be missed by the slower TDS5404B.

In normal operating conditions, the background noise due to the data acquisition system of the oscilloscope (Tektronix TDS 5104B or 7404B) and the long BNC cables (connecting the scope to the DUT in the vacuum chamber) was roughly 10 mV. The limits for the scope trigger window were set 20 mV above and below the nominal voltage reading of the scope. The scope was set up to record the voltage waveform for 1 µs (at a 20ns resolution) following the occurrence of the trigger (duration and resolution being decided based on the longest and shortest transients observed in a few trial runs). The recorded waveforms allowed detailed analysis of the SET signatures.

B4. Input Code and Supply Voltage:

On the first DUT tested, testing was done for 2 different supply voltages (2.7 and 5.5 V) and for three different digital input codes, 15 %, 50 % and 85 % of full-scale (Table I). Testing was done slightly higher than zero scale and slightly lower than full scale so that both positive-going and negative-going transients could be seen. The remaining two DUTs were tested under the condition that created the worst case condition in terms of the highest SET cross section.

TABLE I
Supply voltage and input codes used during testing.

Supply Voltage (V)	Input			Output	
	Word	% Full Scale	Binary	Expected (V)	Actual (V)
2.7	614	15	001001100110	0.405	0.46
2.7	2048	50	100000000000	1.35	1.42
2.7	3482	85	110110011010	2.295	2.37
5.5	3482	85	110110011010	4.675	4.74

C. Test Sequence:

Testing was done in three sessions, SEL testing and SET characterization of DUT 1, SEL and SET testing of DUT 2 and 4 and SEFI testing of DUT 2.

In the first session, DUT 1 was run in dynamic mode with an input clock of 20 MHz and a sample rate of 1 MS/s. It was first tested at room temperature at the supply voltages and input codes listed in Table I. All ion energies were run for each set of operating conditions. Each ion was run until 100 output errors were seen, or until the fluence reached 1 x 10^7 ions/cm^2, which ever came first.

For SEL testing, the supply voltage was set to the maximum operating value (5.5 V) and the input code was set to 3482. The board was then heated to 125°C and testing with Bismuth at 35° incident angle was repeated for an effective LET of 121.89 MeV/mg/cm^2. Finally, testing with Bi was done at normal incidence, following which the DUT was powered down.

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The SET data from DUT 1 was evaluated to determine in the worst case operating conditions, resulting in the highest probability of an SET. It was found that the worst case conditions were at the highest supply voltage and the highest input code.

At the second session, DUT 2 and 4 were tested under dynamic mode with an input clock of 20 MHz and a sample rate of 1 MS/s. For SET testing, the supply voltage was set at 5.5 V and the input code was set at 3482. All ion energies were run for each set of operating conditions. Each ion was run until 100 output errors were seen, or until the fluence reached 1 x 10^7 ions/cm^2, which ever came first.

For SEL testing, the supply voltage was set to the maximum operating value (5.5 V) and the input code was set to 3482. The board was then heated to 125°C and testing with Bismuth at 35° incident angle was repeated for an effective LET of 121.89 MeV/mg/cm^2. Finally, testing with Bismuth was done at normal incidence, following which the DUT was powered down.

At the third session, SEFI testing was performed on DUT 2. Supply voltage was set to 5.5 V and the input code was set to 3482. The part was initially tested in a dynamic mode with the clock set at 20 MHz and the sample rate at 1 MS/s. The part was then tested in a static mode. After the input code was loaded into the part, the WaveVision board was powered down, so that the clock signal was shut off to the part and the input code did not get refreshed. Testing was done at room temperature with bismuth for an LET of 99.74 MeV/mg/cm^2.

D. Test Equipment

1. DAC121S101EVAL Boards (nos. 1, 2 and 4).
2. WaveVision board.
3. Power Supply with current display HP 6624A
4. Oscilloscopes Tektronix TDS 5104 and TDS 7404
5. Lakeshore Temperature Controller, Model 332
6. Laptop Computer with WaveVision 4 Software
7. Digital Multimeter Agilent 34401A
8. Digital Multimeter Fluke 8050A
9. Precision Power Supply HP 6114A

E. Test Facility and Ion Beams

Testing was done using the 88" cyclotron at the Berkeley Accelerated Space Effect facility at the Lawrence Berkeley National Laboratory.

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The 4.5MeV/nucleon cocktail with the following ions were used in the testing:
Ne, Ar, Cu, Kr, Xe, Tb, Ta and Bi

The energies and penetration depths are shown in Appendices A and B. On the DAC121S101WGRQV it is 11 µm from the top of the passivation layer, through the active area to the bottom of the epi layer and the top of the highly doped substrate.

F. Test dates

DUT 1 (SEL and SET characterization):	October 16 and 17, 2007
DUT 2 and 4 (SEL and SET):	December 12, 2007
DUT2 (SEFI):	August 23, 2008

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IV. Test Results

A. SEL

Specific SEL testing was done with the DUT heated to 125°C and under maximum operating voltage (5.5 V), with the DUT oriented 35° to the beam during a Bi ion run to a fluence of 1 x 10^7 for an effective LET of 121.89 MeV/mg/cm^2. However, the supply current and DUT functionality were monitored during every ion run.

No incidences of SEL or any hard errors were detected. No surges in supply current were seen and the supply current variation was less than 10 µA during every ion run. The DUT continued to operate properly after every ion run.

B. SEFI

No evidence of a SEFI was seen while the part was being tested in dynamic mode.

To ensure that a possible SEFI might not have been detected due to the input and control code being updated every 1 µs, one unit was also tested in a static mode, where the where the input and control codes were inputted once and never updated. The DUT was tested with the Bi ion for an LET of 99.74 MeV/mg/cm^2 to a fluence of 1.4 x 10^7 cm^2.

No evidence of a SEFI was seen while the part was tested in static mode. The output always returned to the expected voltage after an SET and the DUT never went into shutdown mode.

C. SET

SETs of a fairly wide range of amplitude and duration were recorded. The SET signatures varied greatly with operating conditions.

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V. Analysis of SETs

A. Figure of Merit:

The Weibull distribution [5] was used to statistically characterize the failure behavior of the device. Furthermore, a figure of merit equation [6] was used to predict the monthly upset rate of the DAC.

A1: Weibull Distribution:

The integral form of the distribution that describes the event cross-sections as a function of LET is:

$$F(L) = A\left(1 - \exp\left\{-\left[\frac{L - L_0}{W}\right]^s\right\}\right); L > L_0$$

$$F(L) = 0; L < L_0$$

where, **F(L)** is the event cross-section for a particular LET
A is the limiting cross-section
W is the width of the distribution
L_0 is the threshold LET
s is the shape parameter

For the ease of calculation, L_0 was set to 0 and W was set to 100. The values of A and s were adjusted to fit the actual data.

A2: Monthly Events:

The following figure of merit was used to characterize the monthly number of transients in a geosynchronous orbit from the DAC output:

$$FOM = 30 \times 200 \times \frac{\sigma_{limit}}{L_{0.25}^2}$$

where, **σ_{lim}** is the limiting cross-section
$L_{0.25}$ is the LET at 25% of the limiting cross-section

The multiplication by 30 in the FOM was used to get the monthly number of events.

A3: Total Monthly Accumulated Event Time:

The total monthly accumulated event time, i.e. monthly outage time, was calculated by multiplying the FOM with the average of the longest upset lengths for all the ion strikes.

B.SET Data Analysis:

DUT 1 was tested under the 4 conditions listed in Table I. The worst case condition, resulting in the highest cross section and probability of a transient, was with the supply current at 5.5 V and the input at 85% of full scale. At 2.7 V, 15 % of full scale, the cross

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section is the smallest. Despite a few exceptions, the general trend seems to be one of increasing cross section with increasing voltage, which is somewhat counter intuitive. The remaining units were only tested at a supply voltage of 5.5 V and an input code at 85 % of full scale.

The SET cross sections vs. LET are plotted in Fig. 7 for the four conditions tested. The Weibull fits are also shown. The Weibull fit parameters are listed in Table II. Deviation from the data is significant for almost all runs with Copper. Anecdotal reports of anomalies with copper have been reported before.

Almost all the transients observed had a duration exceeding 20ns. The longest one was 4220 ns and a large majority were between 200 to 2000 ns. Such transients are normally observed due to strikes in analog components. Strikes in digital circuitry like DAC registers typically recover in less than 2 ns, unless clocked onto the next stage, in which case a dc (flat) error equal to the entire length of the clock cycle is generated. About 10 to 20% of the transients belonged to the first kind and none of the second kind were observed, indicating that the digital input stages and the DAC registers were fairly immune to Single Event strikes. The other critical components are the switches on the DAC resistor string and the analog buffer amplifier. These are the most likely sources of nearly all observed transients. The time between two successive transients varied between 100 microseconds to 2 seconds.

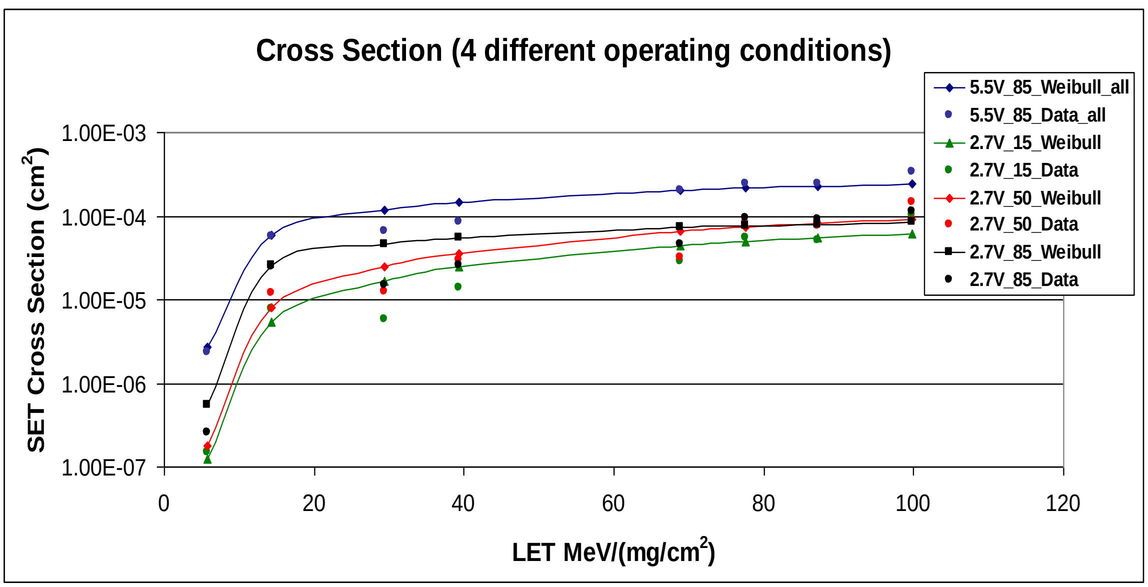

Fig. 7 SET Cross section vs. LET for the four conditions tested, along with Weibull fits of the data. The data labels indicate the supply voltage, followed by the percent of full scale of the input code. Data from all 3 units is included in the 5.5V plot. Only DUT 1 was tested at 2.7 V.

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TABLE II
Weibull Fit Parameters for SET Cross Sections (Fig. 7)

Vsupply	Input	A	Lo	W	s
2.7	15%	1.02e-4	5.40	100	1.2
2.7	50%	1.48e-4	5.40	100	1.3
2.7	85%	1.12e-4	5.74	60	0.8
5.5	85%	1.69e-4	5.60	60	0.6

B1. Important figures from SET Data Analysis:

1. Highest cross-section: 4.24×10^{-4} cm^2, for Bi, LET of 99.74MeV/(mg/cm^2), at 5.5 V, 85 % (for DUT 4).
2. Maximum transient amplitude: +1.6 V, for Bi, LET of 99.7MeV/(mg/cm^2), at 2.7 V, 15 % (DUT 1).
3. Number of transients with amplitude higher than 1 V: 21 (out of 3240 total per board).
4. Maximum transient duration: 4.22 μs, for Bi, at 2.7 V, 85 % (DUT 1).
5. Number of transients with duration higher than 2 μs: 197 (out of 3240 total per board).

C. SET Signatures:

The analysis of the test data was done to generate distributions of length, amplitude or direction of transients. The transients were principally of 5 types:

1) Slow Positive Transients, mostly with durations between 0 – 150 ns. Amplitude of these transients showed very little correlation with transient duration (Fig. 8).

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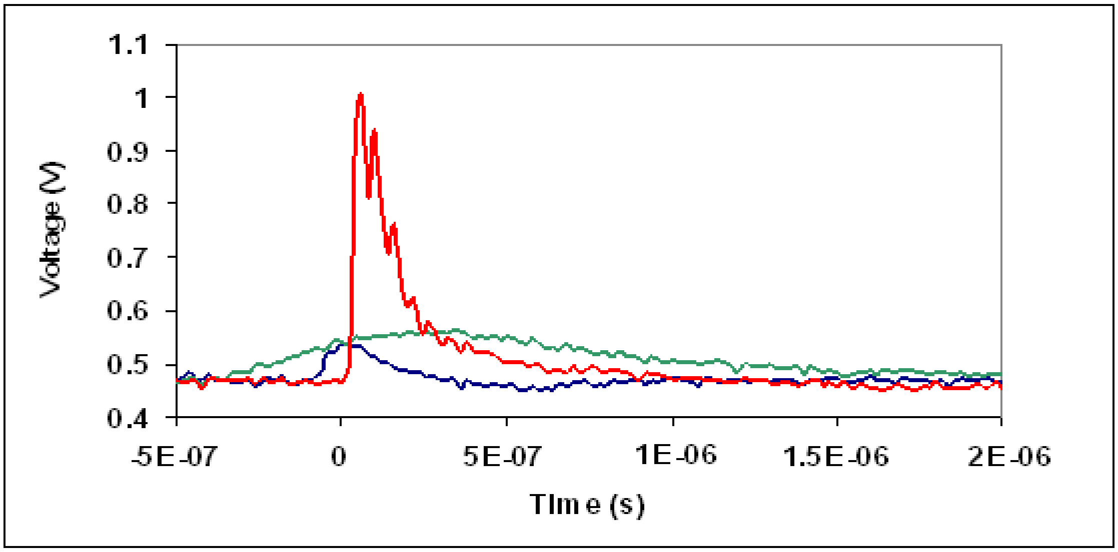

Fig. 8 Type 1 SET (slow positive transient). Examples are from a Ta run for DUT1 with supply voltage at 2.7 V and input code at 15 % of full scale.

2) Fast Positive Transients, with some negative jitter. These are mostly of very short duration (Fig. 9):

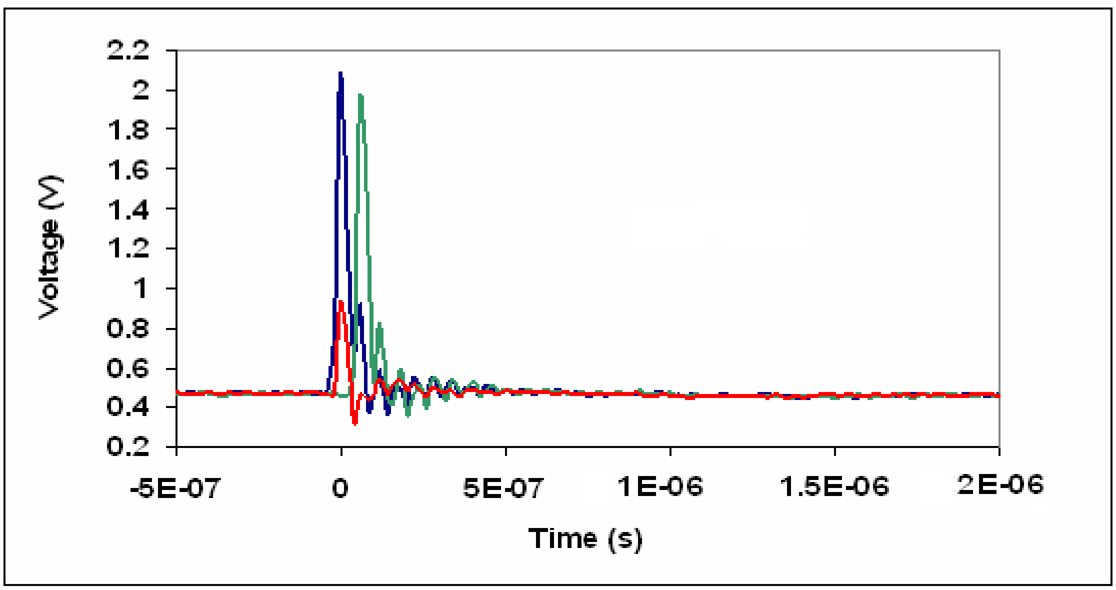

Fig. 9 Type 2 SET (fast positive transient with some negative jitter). Examples are from a Ta run for DUT1 with supply voltage at 2.7 V and input code at 15 % of full scale.

3) Oscillations, usually of very short duration. These are more frequent at input codes representing higher voltages. We choose to define a transient as an oscillation if the dominant half of the transient (positive or negative) occupies less than 75 % of the transient period (Fig.10).

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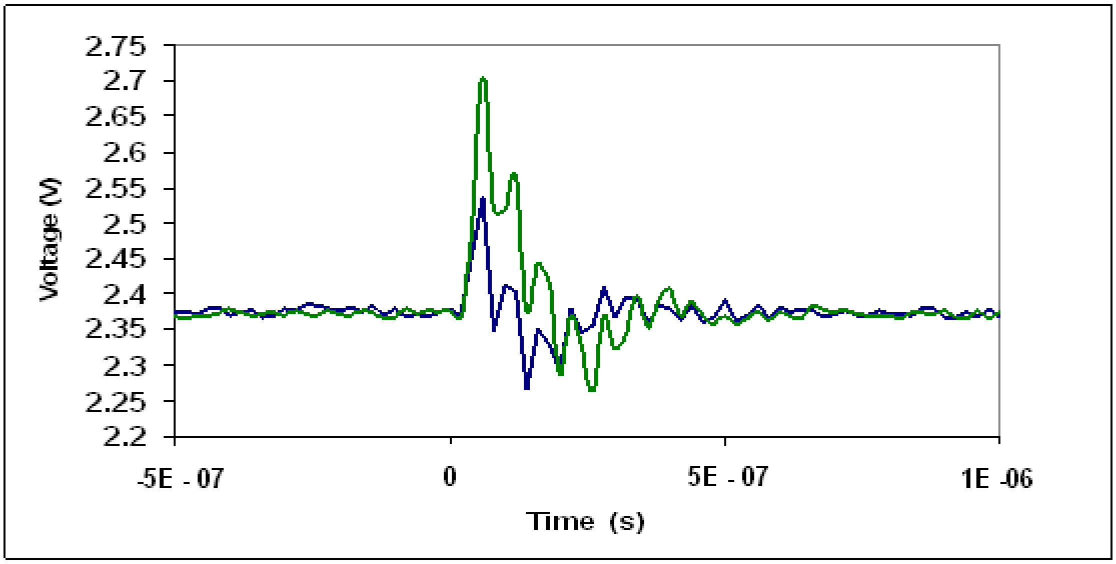

Fig. 10 Type 3 SET (short duration oscillations). Examples are from a Tb run for DUT 1 with supply voltage at 2.7 V and input code at 85 % of full scale.

4) Negative Transients, with or without jitter. This is the most common type of transient, seen frequently at all codes. On an average, these transients are of much longer duration than positive ones. The negative transients are generally small amplitude (less than 0.6 V). The duration of these transients increases with amplitude (Fig. 11).

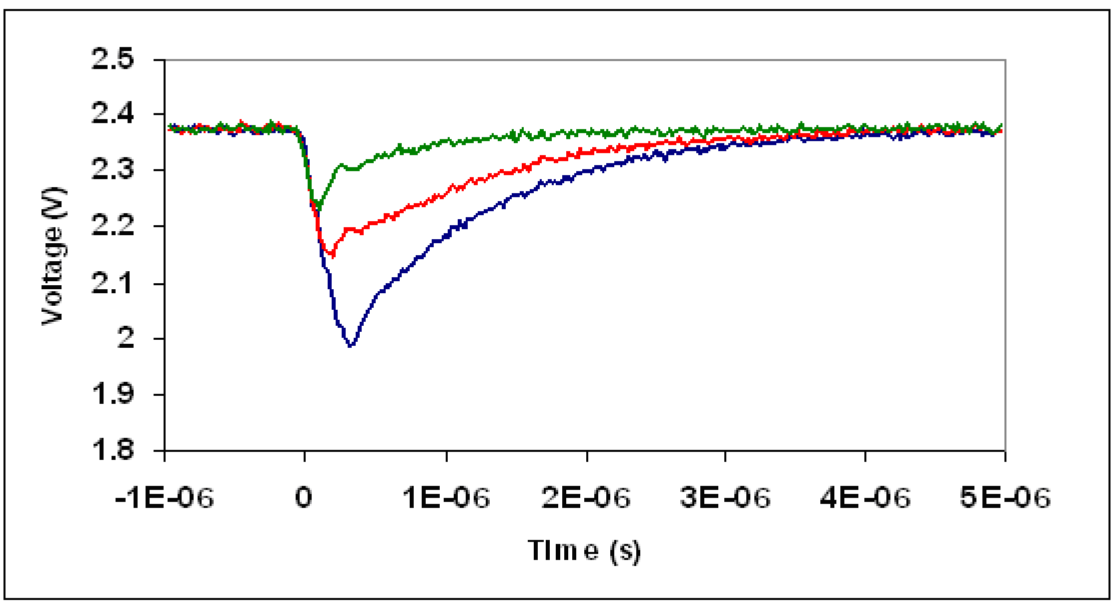

Fig. 11 Type 3 SET (negative transients). Examples are from a Bi run for DUT 1 with the supply voltage at 2.7 V and the input code at 85% of full scale.

5) Transients with slow rise time. These were very rare, only 2 of these were observed out of 3240 total transients. Both these transients were at 50 % full scale input code at 2.7 V operating voltage. These were widely out of trend (duration and amplitude) from the remaining transients in the same input conditions (Fig. 12).

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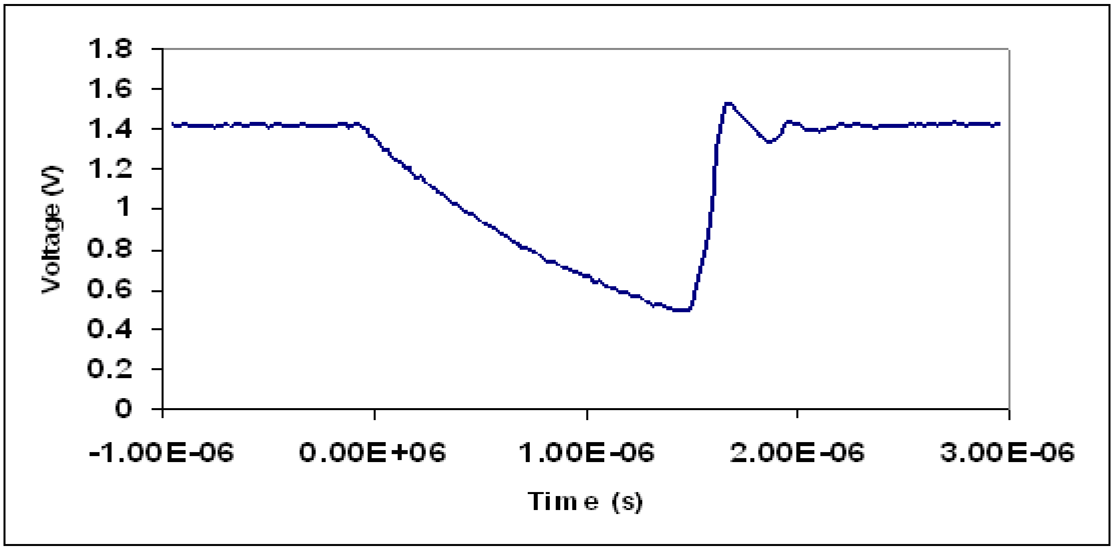

Fig. 12 Type 5 SET (transients with slow rise time). Example is from a Ta run of DUT 1 with supply voltage at 2.7 V and input code at 50% of full scale.

D. Transient distributions in time, amplitude, direction:

The probability of a transient varied with transient type. The most dominate type of SET was the negative transient (Type 3). This is illustrated in the cross section curves for Type 4, negative transients (Fig. 13) and the amplitude vs. pulse widths plots (Fig. 16-19 and 22-23).

There was a higher incidence of negative transients with the higher input code (Fig. 13).

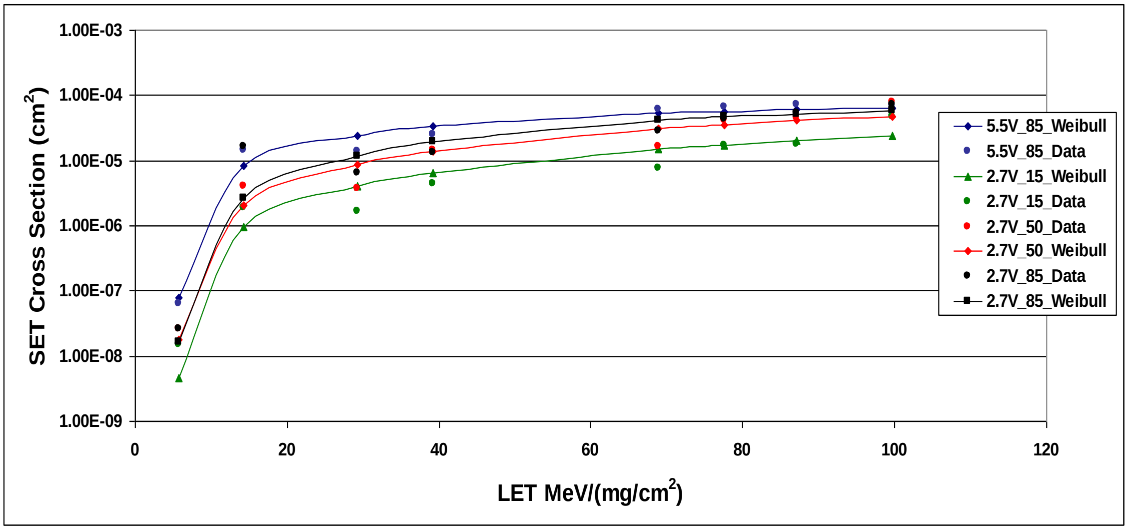

Fig. 13 Cross section vs. LET for negative transients (Type 4) for DUT 1.

The positive transients (Type 1 and 2), which account for roughly a quarter of the total number of transients, have a cross-section 2-3 times smaller than the corresponding negative transient cross section (Fig. 14).

Unlike the negative transients, the cross section of the positive transients decreased with increasing input code (Fig. 14).

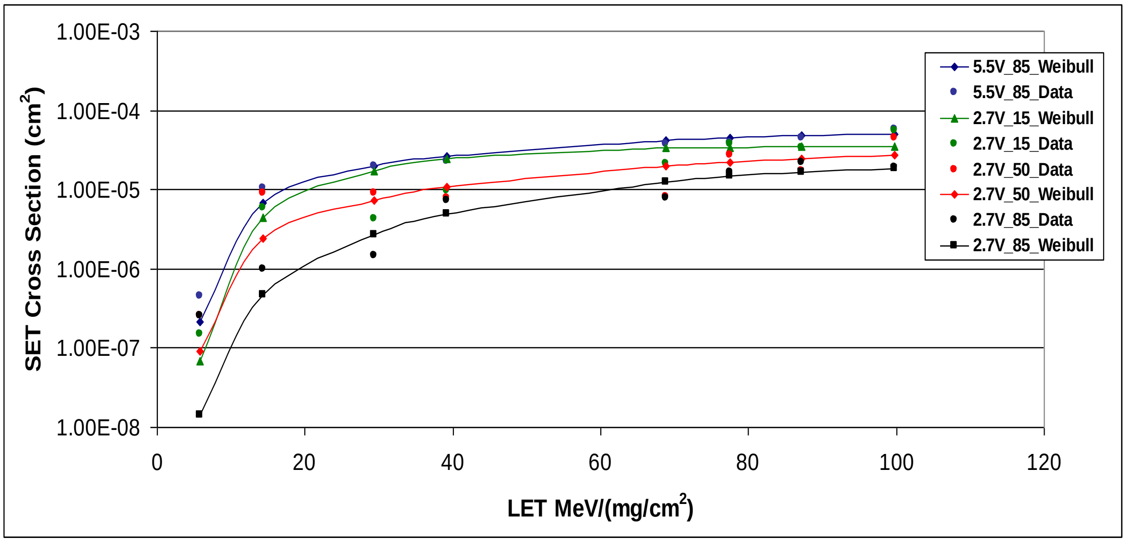

Fig. 14 Cross section vs. LET for positive transients (Type 1 and 2) for DUT 1

A fairly significant fraction of the transients are oscillatory (Type 3). However, at an input code of 15 % of full scale, no oscillatory SET was seen (Fig. 15).

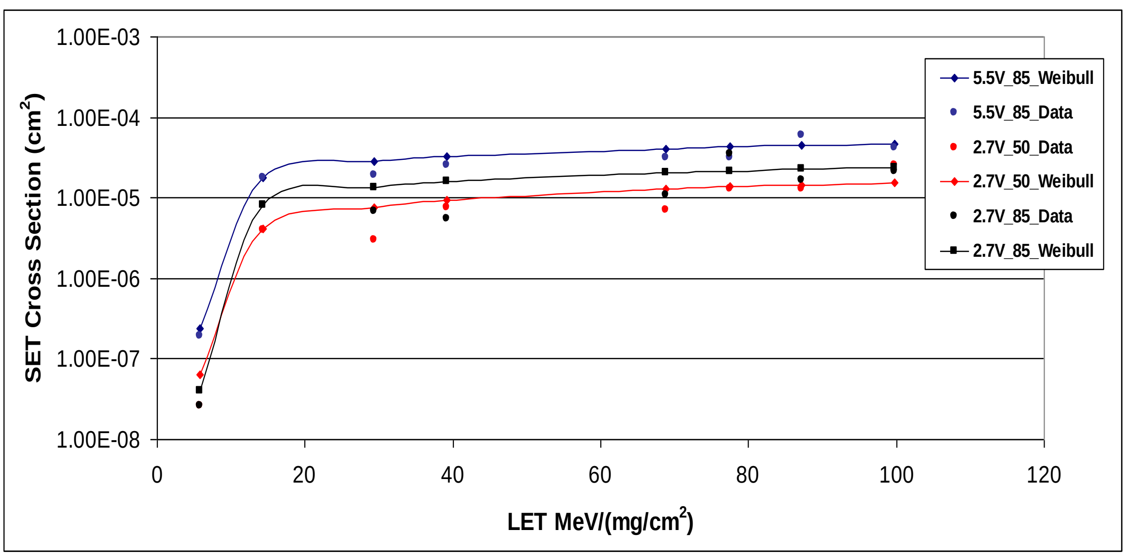

Fig. 15 Cross section vs. LET for oscillatory (Type 3) transients for DUT 1. No Type 3 transients were seen when the input code was set at 15 % of full scale.

D1. Transient distributions in time, amplitude: The distribution of transient duration and amplitude showed the following major features:

1) Negative transients showed more variation in duration. Positive transients show a wider range of amplitude (Fig. 16-19 and 21-22).

2) At 2.7 V, 85 % of full scale code operation, average transient length is the highest (Fig. 17).

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3) At 2.7 V, 15 % full scale code operation, average transient amplitude is the highest (Fig. 19).

4) At 2.7 V, 50 % full scale code operation, the transient duration and amplitudes are noticeably small compared to other operating conditions (Fig. 18).

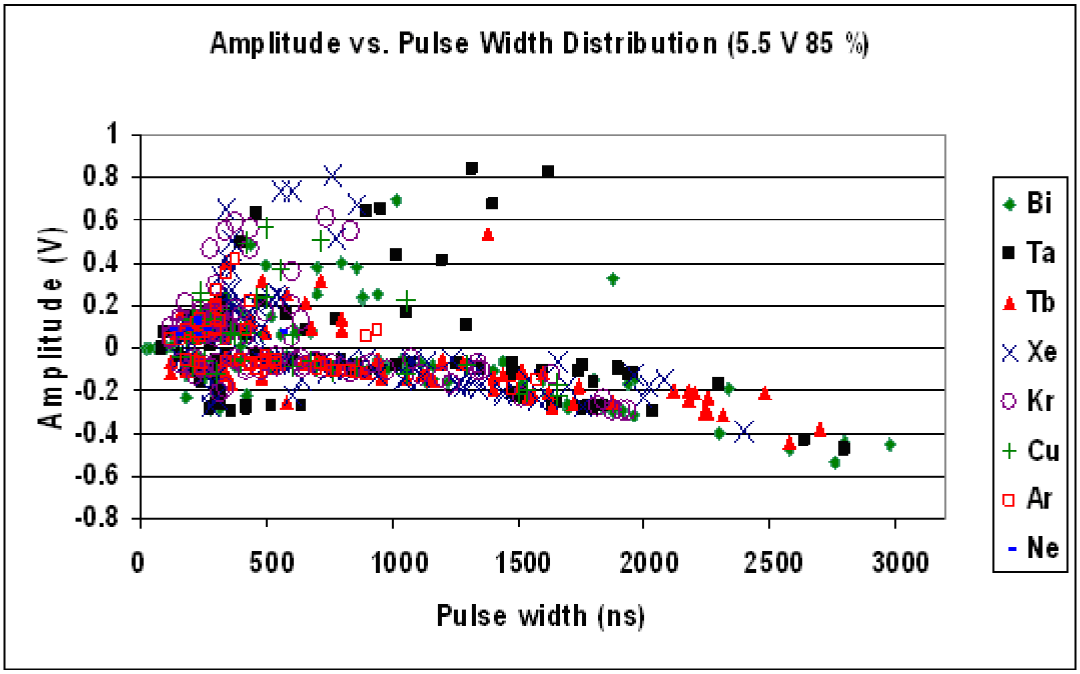

Fig. 16 Amplitude vs. Pulse Width Distribution for DUT 1 with the supply voltage at 5.5 V and the input code at 85 % of full scale.

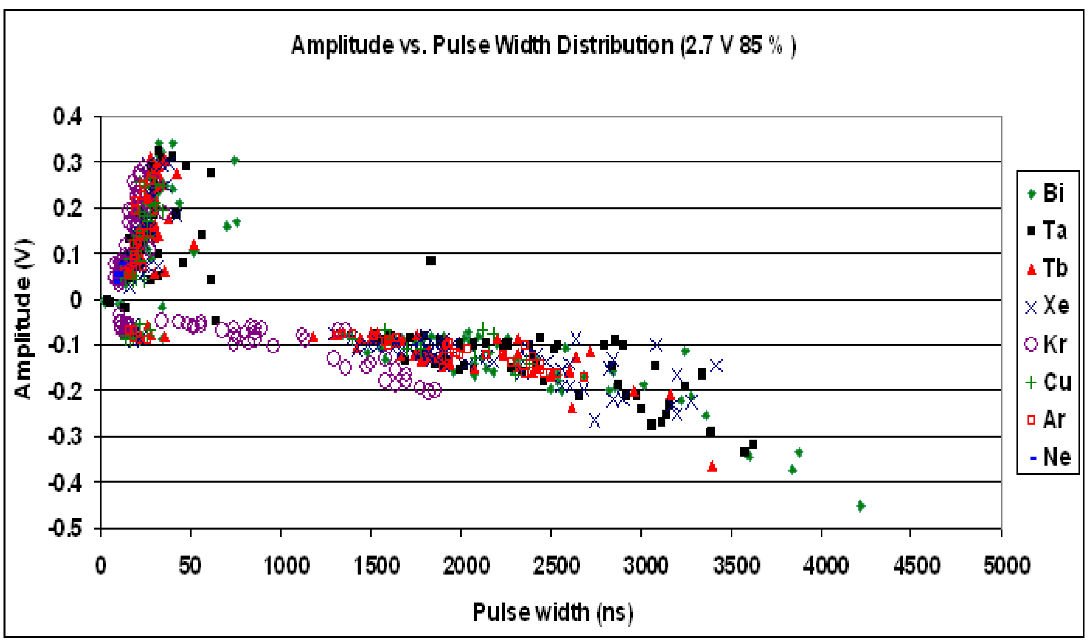

Fig. 17 Amplitude vs. Pulse Width Distribution for DUT 1 with the supply voltage at 2.7 V and the input code at 85 % of full scale.

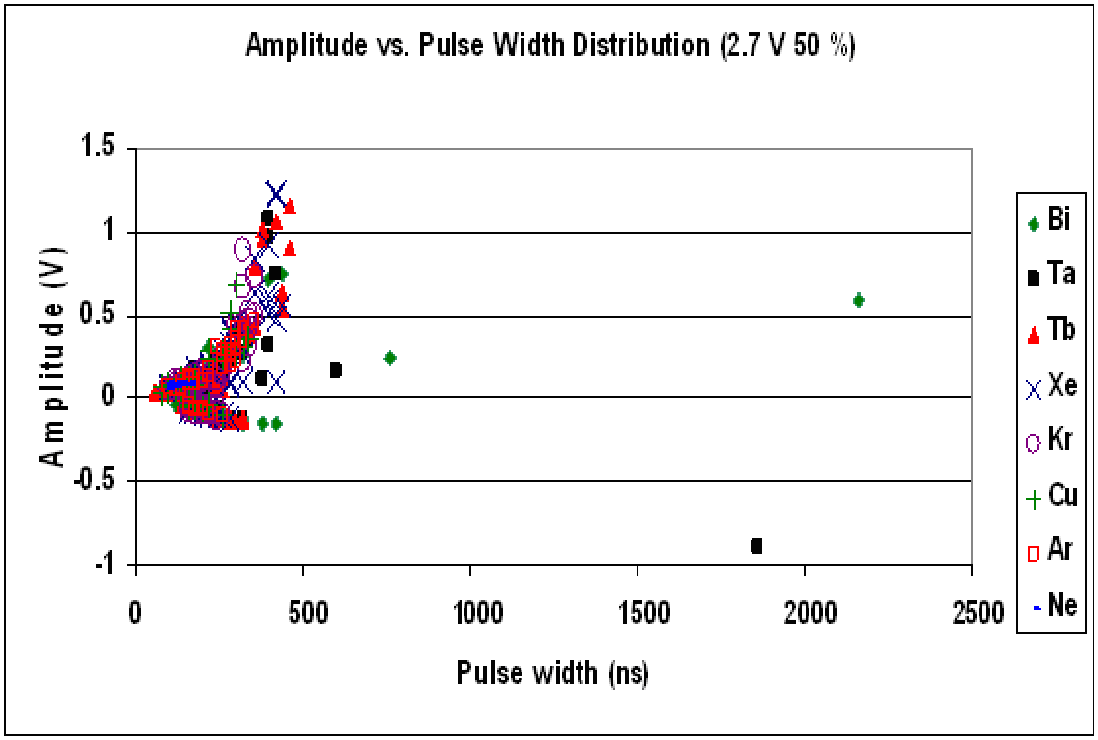

Fig. 18 Amplitude vs. Pulse Width Distribution for DUT 1 with the supply voltage at 2.7 V and the input code at 50 % of full scale.

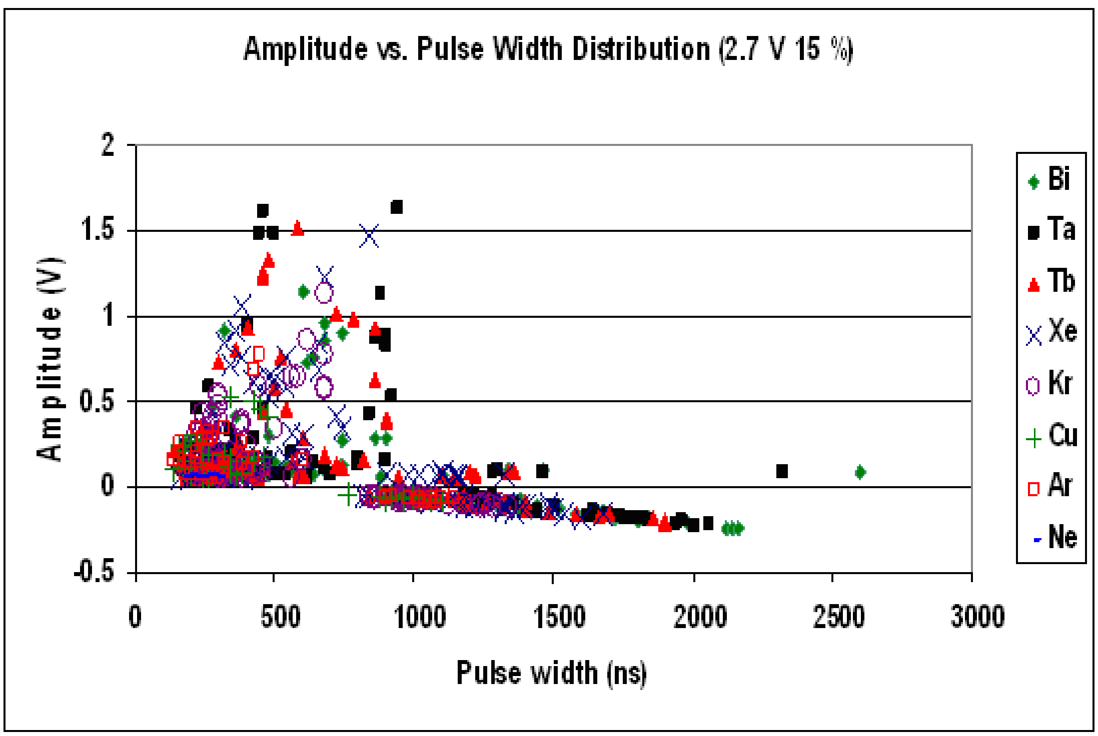

Fig. 19 Amplitude vs. Pulse Width Distribution for DUT 1 with the supply voltage at 2.7 V and the input code at 15 % of full scale.

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VII. Part to part SET variation

All 3 DUTs were tested at the worst case condition for the highest SET cross section, which was with the supply voltage at 5.5 V and the input code at 85% of full scale. DUT 1 was tested using a different oscilloscope than used with the other two DUT's. DUT 2 and DUT 4 cross sections are within 20 % of each other in the terminal part of the curve (Fig. 20). DUT 1 had a cross section that was roughly 50 % lower than the other two DUT's, but most of that variation is likely due to the differences in oscilloscopes. The faster oscilloscope used with DUT 2 and DUT 4 most likely captured some fast transients that were missed by the slower oscilloscope used with DUT 1.

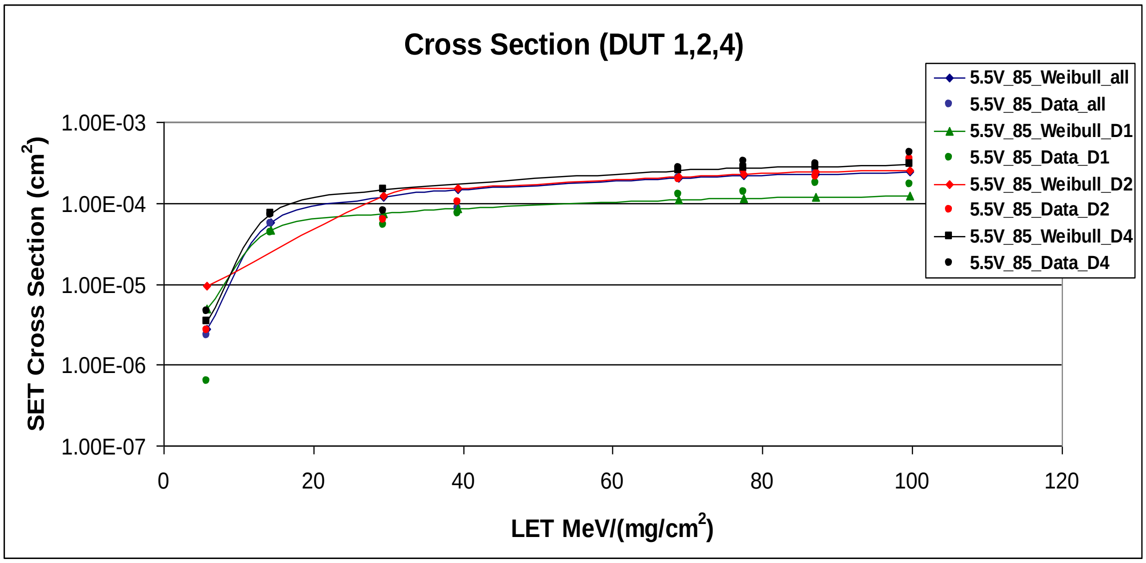

Fig. 20 Cross section vs. LET curves for the 3 DUT's tested with supply voltage at 5.5 V and the input code at 85 % of full scale.

The SET signatures were generally the same for all three DUTS (Fig. 16, 21 and 22). Note that for DUT 2 and 4, the positive transient readings were truncated at roughly 0.43 V due to the range limitations of the oscilloscope.

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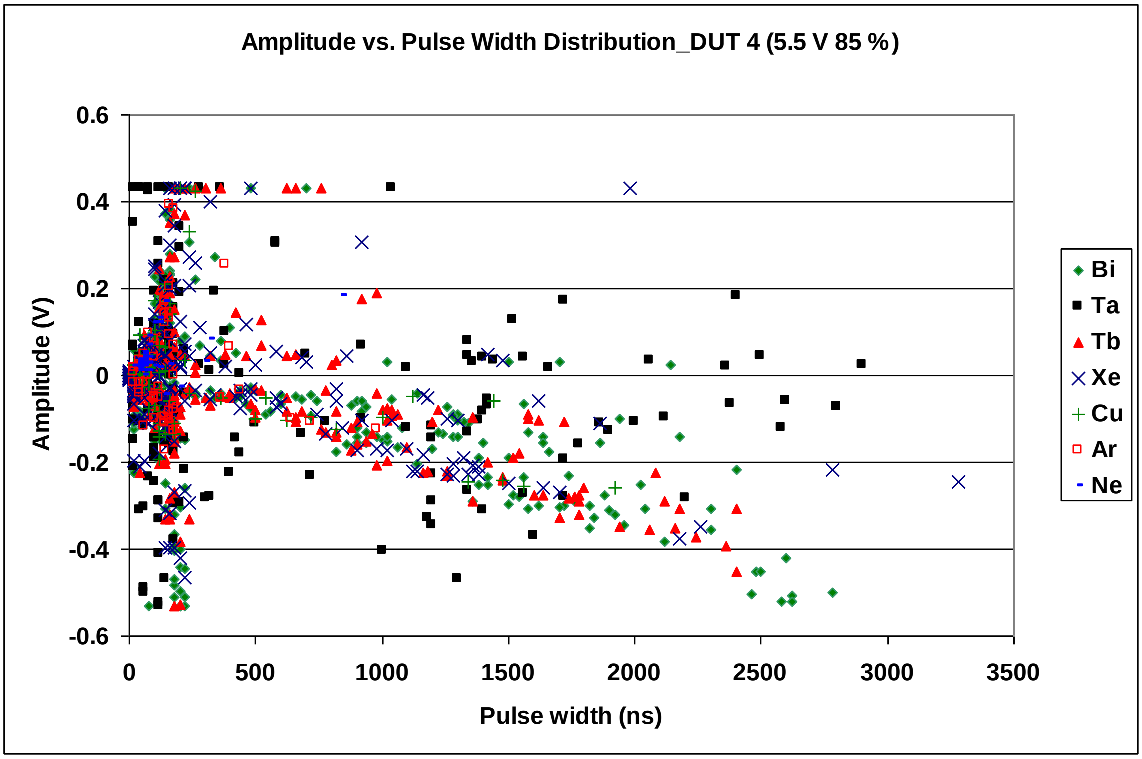

Fig. 21 Amplitude vs. Pulse Width Distribution for DUT 2 with the supply voltage at 5.5 V and the input code at 85 % of full scale.

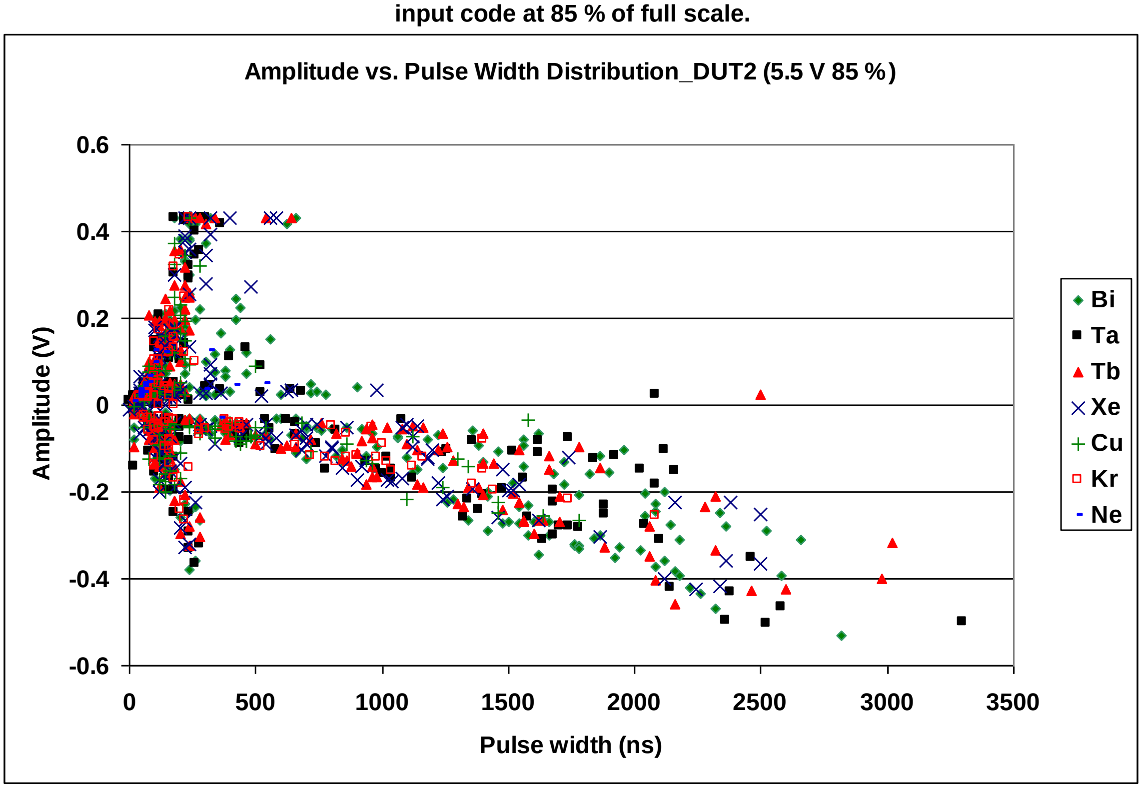

Fig. 22 Amplitude vs. Pulse Width Distribution for DUT 4 with the supply voltage at 5.5 V and the input code at 85 % of full scale.

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VIII. Conclusions

The space level DA121S101WGRQV/MLS is immune to Single Event Latchup to an LET of greater than 121 MeV/mg/cm^2 and SEFI greater than 99 MeV/mg/cm^2. Latchup immunity was verified both at room temperature (300 K) and high temperature (398 K), both at normal incidence and 35 degree angles.

A variety of Single Event Transients are observed which have a worst case cross section of 4×10^{-4} cm^2. The transient signatures are highly dependent upon operating conditions. Input code can have a significant impact on transient amplitude and duration. The total outage time due to single-event induced transients for the DAC was 47.7 ns/month. The total number of events/month was $1.13\text{x}10^{-2}$.

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Appendix A

Heavy-Ion Cocktail Bragg Curves

Fig. A1 is a Bragg curve plot from the Lawrence Berkeley National Laboratory that shows the depth of penetration and energy for each ion used in the experiment [7]. The DAC121S100WGRQV has a thickness of 11 µm from the top of the passivation to the bottom of the epi layer. From Fig. A1, one can see that at 11 µm, none of the ions start to lose energy and some have a slight increase in energy. Thus, the LET value of the ion is almost constant as it passes through the sensitive charge collection region of the transistor. As a result, the need to correct LET magnitudes used in the report (for penetration depth) was eliminated.

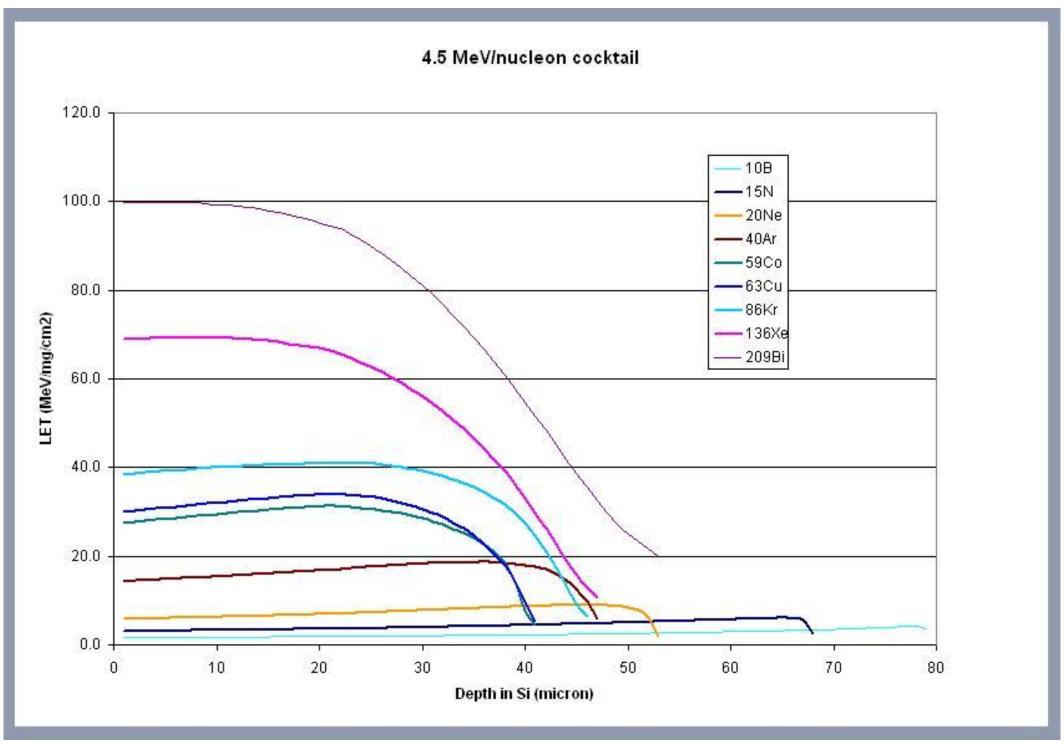

Fig. A1. LET vs. penetration profile for various ion species used in the heavy-ion experiments

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Appendix B

4.5 MeV/nucleon cocktail (HeH^{+1} to Bi)

This cocktail, based on a tune-up of the ion source and Cyclotron using $^{40}Ar^{+8}$, has an A/q ratio of 5 and energy of 4.5 MeV/nucleon. All of the above information was obtained from LBNL.

Table B1. Heavy-ion cocktail used in the SEE experiments.

Cocktail	Ion	Ion Energy	Mass	Charge State	LET	Range in Si
~MeV/u		MeV	amu		(MeV/(mg/cm^2))	microns
4.5	B*	45	10	+2	1.64	79
4.5	N	67	15	+3	3.08	67
4.5	Ne	90	20	+4	5.73	53
4.5	Ar	180	40	+8	14.33	48
4.5	Cu	293	65	+13	29.91	44
4.5	Kr*	325	78	+15	39.54	41
4.5	Kr	378	86	+17	39.25	47
4.5	Ag	464	107	+21	58.19	46
4.5	Xe	603	136	+27	68.46	48
4.5	Tb	724	159	+32	77.50	52
4.5	Ta	805	181	+36	87.20	53
4.5	Bi*	940	209	+41	99.70	54

* = by special request

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