# Single Event Transient Response Dependence on Operating Conditions for a Digital to Analog Converter

Kirby Kruckmeyer, *Member, IEEE,* James S. Prater, Bill Brown and Sandeepan DasGupta

***Abstract*—The Single Event Effect (SEE) characterization of a Digital to Analog Converter (DAC) showed an unexpected Single Event Transient (SET) dependence on operating conditions. The worst case condition resulting in the highest probability of an SET was at the highest supply voltage. The SET signatures were dependent on the input code, with some signatures not present when the input code was at mid scale. The SET characterization results are presented, along with a simulation study that explains the SET response dependence on the operating conditions. These results emphasize the importance of running an SEE characterization on a mixed signal product and monitoring all aspects of the SET signatures, including probability, amplitude, pulse width and oscillatory behavior, to determine the worst case operating conditions.**

***Index Terms*—digital to analog converter (DAC), mixed signal, single event transient (SET), single event upset (SEU)**

## I. INTRODUCTION

FOR most product types, the worst case operating condition for Single Event Upsets (SEU) is with the product running at the minimum operating voltage. This is the operating condition where the probability of an upset due to an ion strike would be the highest. The test standards for measuring Single Event Effects (SEE), EIA/JEDEC Standard JESD57 [1] and the ASTM Standard Guide F1192 [2], both suggest that minimum operating voltage is usually the worst case, although JESD57 does recommend that steps be taken with each product to ascertain worst case conditions. Neither test standard gives guidance for test conditions for Single Event Transients (SET). Previous testing on comparators and amplifiers has produced mixed results, with different supply voltages and inputs being worst case [3] – [9].

SEE characterization of a Digital to Analog Converter (DAC) showed that the maximum operating voltage is actually the worst case condition for this product, resulting in the highest probability of an SET. In addition, the SET signatures, pulse widths, and amplitudes were highly dependent upon the input code, and less dependent upon the output voltage.

A simulation study was run to help locate the areas of the circuit sensitive to an ion strike and explain why transient amplitudes and pulse widths were dependent upon the input code.

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Kirby Kruckmeyer is with National Semiconductor, Santa Clara, CA 95052 (telephone: 408-721-3548, email: kirby.kruckmeyer@nsc.com).

James S. Prater is with National Semiconductor, Fort Collins, Colorado 80525 (telephone: 970-225-7580, email: james.s.prater@nsc.com).

Bill Brown is with National Semiconductor, South Portland, Maine 04106 (telephone: 207-541-8647, email: bill.brown@nsc.com).

Sandeepan DasGupta is with Vanderbilt University, Nashville, TN 37235 (email: sandeepan.dasgupta@vanderbilt.edu).

## II. DEVICE DESCRIPTION

The product tested in this study was National Semiconductor's DAC121S101WGRQV, a 12 bit DAC with a serial input. It can operate with supply voltages ($V_A$) from 2.7 to 5.5 V and has a rail-to-rail output [10]. With a supply voltage of 2.7 V and a full-scale input code of 4095, the output will be close to 2.7 V. The product is manufactured on a 500 nm CMOS process, using National Semiconductor's PowerWise Technology for ultra low power consumption, typically consuming 177 µA at a 3.6 V supply. The DAC is immune to Single Event Latchups (SEL) and Single Event Functional Interrupts (SEFI) to 120 MeV-cm$^2$/mg and passes Total Ionizing Dose (TID) testing at 100 krad(Si) [10].

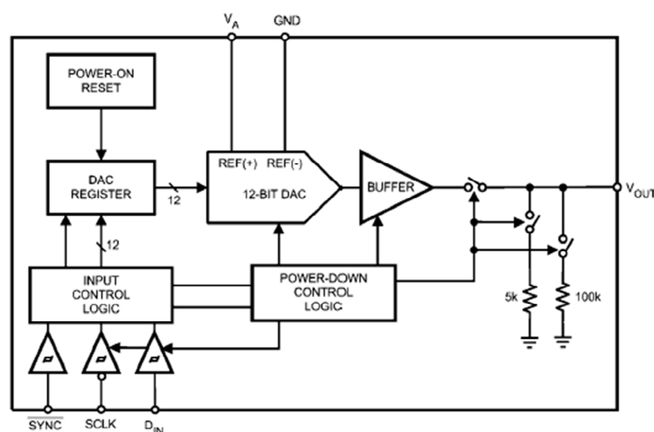


Fig. 1 DAC121S101WGRQV block diagram.

The input to the device is through a 3 pin serial interface, consisting of an input pin ($D_{IN}$), a clock pin (SCLK), and a sync pin ($\overline{SYNC}$) (Fig. 1). A write sequence begins by

toggling the sync pin to the low logic state. Once the clock pin is low, the data on the input line is clocked into the 16-bit serial input register on the falling edges of the clock. On the 16th falling clock edge, the last data bit is clocked in, the data are transferred into the DAC register and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. The first two bits are "don't care" bits and the second two bits control the power down options. The code to be converted to the output voltage is contained in the remaining 12 bits. The data remain in the DAC register until the sync pin is toggled between the high and low logic states. The clock can operate up to 20 MHz.

The DAC121S101WGRQV is built with a resistor string DAC architecture (Fig. 1). The code held in the DAC register is converted to voltage in the DAC section which consists of two resistor strings, one course and one fine (Fig. 2). The output is driven through a buffer amplifier that has a rail-to-rail swing (Fig. 3).

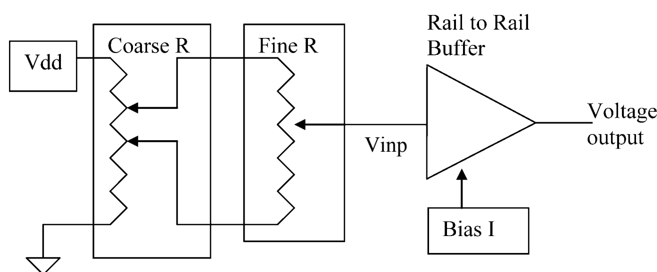


Fig. 2 The analog blocks of the DAC121S101WGRQV: the resistor strings of the DAC and the rail to rail buffer.

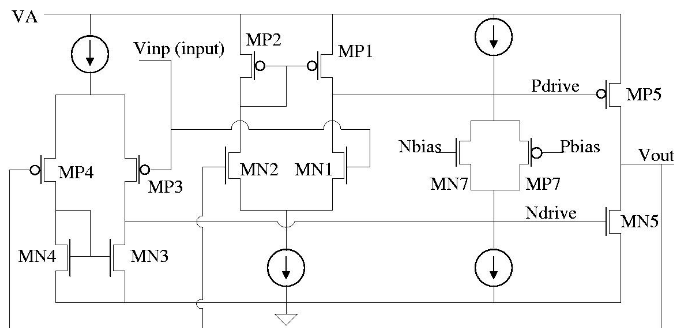


Fig. 3 Simplified schematic of the output buffer.

## III. Test Method

SEE testing was done in accordance with JESD57, using the Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) [11], during three different sessions. The 4.5 MeV/nucleon cocktail was used during the testing, with all testing done at normal incidence. The ions available, linear energy transfers (LET) and penetration depths are listed in Table I [11]. Not all ions were used at each test session. The ion beam penetration at the LBNL facility is sufficient for this product. The distance from the surface of the die, down through the active area to the interface of the highly doped substrate is less 12 μm.

TABLE I
Ions Used During Testing

| Ion | LET ($MeV\text{-}cm^2/mg$) | Penetration Depth (μm) |
|---|---|---|
| Ne | 5.77 | 53.1 |
| Ar | 14.32 | 48.3 |
| Cu | 29.33 | 45.6 |
| Kr | 39.25 | 47.1 |
| Xe | 68.84 | 48.3 |
| Tb | 77.52 | 52.4 |
| Ta | 87.15 | 53.0 |
| Bi | 99.74 | 52.9 |

For this testing, the device under test (DUT) was assembled into a plastic MSOP package, which was decapped to expose the surface of the die to the ion beam. The DUT was soldered to a DAC121S101 Evaluation Board [12], which was connected to a WaveVision Board [13] to drive the DUT. The WaveVision board provided the clock signal and input code and drove the sync pin. The output of the DAC was connected to a 2 kΩ load and a 200 pF capacitor. Three different DUT's were tested, using different operating conditions.

DUT 1 and 4 were tested in a dynamic sampling mode. The serial interface clock was run at 20 MHz, the maximum operating frequency. Previous testing on data converters has shown that either clock speed does not make a difference in the probability of an SEU [14] or maximum clock speed is worst case [15]. The sync pin was toggled high and then low every 1 μs for a sample rate of 1 MS/s. This was less than the maximum sampling rate of 1.25 MS/s, but was used due to a limitation in the WaveVision software. To confirm that maximum clock frequency was worst case, DUT 2 was tested under two different sampling modes. One mode was the dynamic sampling mode with the same conditions as used for DUT 1 and 4. The other mode was a static sampling mode, where the serial interface was written to once, and then the WaveVision board was powered down, so that there was no input to the serial interface and no refresh of the input code in the DAC register during the testing.

Testing was started on DUT 1 with $V_A$ at 2.7 V because the standards JESD57 [1] and F1192 [2] suggest that lowest supply voltage is the worst case, resulting in the highest probability of an SEU. Testing was done at three different input codes: low scale (15% of full scale), mid scale (50% of full scale) and high scale (85% of full scale). The low and high scale input codes were chosen so that they would be near the extremes of the input range, but not too close to the extremes so that the output voltage would be too close to the rails that negative-going and positive-going transients would not be seen. DUT 1 was also tested with $V_A$ at 5.5 V and the high scale input code (85% of full scale), as this input code resulted in a highest number of SETs when $V_A$ was at 2.7 V. TABLE II lists the different conditions used, including the supply voltage, input word, input percent of full scale, the binary input code and the actual output voltage. For a 12 bit

DAC, a code of 4095 represents full scale input, which would result in an output close to the supply voltage.

TABLE II
OPERATING CONDITIONS USED DURING TESTING FOR DUT 1

| Supply | Input | | | Output |
|---|---|---|---|---|
| Voltage (V) | Word | % Full Scale | Binary | (V) |
| 2.7 | 614 | 15 | 001001100110 | 0.46 |
| 2.7 | 2048 | 50 | 100000000000 | 1.42 |
| 2.7 | 3482 | 85 | 110110011010 | 2.37 |
| 5.5 | 3482 | 85 | 110110011010 | 4.74 |

Post test processing of the data showed that the SET signatures with the input code at mid scale were different than the SET signatures at the other two input codes. The binary code for the mid scale input, 2048 is mostly zeroes (100000000000). To determine if the SET transients were dependent upon whether the input bits were high or low, the testing was repeated at a later date on DUT 4 with an input codes of 2047, which is a binary of code of mostly ones (011111111111), and 2048. The test conditions for DUT 4 are shown in TABLE III. This testing was only done with the Ne and Ta ions.

TABLE III
OPERATING CONDITIONS USED DURING TESTING FOR DUT 4

| Supply | Input | | |
|---|---|---|---|
| Voltage (V) | Word | % Full Scale | Binary |
| 2.7 | 2047 | 49.99 | 011111111111 |
| 2.7 | 2048 | 50.01 | 100000000000 |

At a separate test session, DUT 2 was tested in the dynamic and static sampling modes with $V_A$ at 5.5 V and the high scale input code of 3482 (85% of full scale). Due beam availability limitations, testing was only done with the Bi ion.

To monitor for SETs on DUT 1, the output of the DUT was connected to a Tektronix TDS5104 oscilloscope. The trigger limits were set at 20 mV above and below the nominal output voltage for each set of supply voltages and input codes. Due to the configuration of the test facility, with the DUT residing in a vacuum chamber and power supplies and oscilloscope outside the chamber, the background noise during testing is much greater than it would be with the product in a typical application. The trigger limits were set based on the noise of the test system environment, so that they were as tight as possible without recording invalid transients. For DUT 2 and 4, a Tektronix TDS7404 oscilloscope was used. During the test session for DUT 4, the background noise was higher, the trigger limits had to be widened to 30 mV above and below the nominal output and the scope resolution had to be set so that some of the high speed, low amplitude transients were not captured. The waveform of each transient was captured and downloaded to a laptop computer for later analysis. Each ion run was done until at least 100 SETs were recorded or a fluence of at least 1 x $10^7$ ions/cm$^2$ was reached, whichever happened first.

## IV. DEPENDENCE ON SAMPLING MODE

The SET cross section represents the relative probability of an SET and is calculated by dividing the number of SETs recorded by the total fluence (measured in ions per cm$^2$) the DUT received at each LET. The SET cross sections were calculated for DUT 2, with the DUT in dynamic sampling mode and in static sampling mode for the Bi ion runs. The difference in the SET cross sections for the dynamic and static sampling modes was less than 14%, and within the error of the experiment, based on the SET sample size. The results are shown in TABLE IV.

TABLE IV
DUT 2 SET CROSS SECTION FOR BI RUN FOR DIFFERENT SAMPLING MODES

| Sampling Mode | SET Cross Section (cm$^2$) |
|---|---|
| Dynamic | 5.5x$10^{-5}$ |
| Static | 4.8x$10^{-5}$ |

## V. DEPENDENCE ON SUPPLY VOLTAGE

### *A. Results*

The SET cross sections at each LET for the input code of 3482 were compared for the different supply voltages, 2.7 V and 5.5 V (Fig 4). For the 2.7 V cross section calculations, all errors outside the ±20 mV trigger limits were counted. For the 5.5 V cross sections, errors outside the limits of ±40 mV were used in the calculation. The wider limits were used for the 5.5 V condition to allow for any scaling factors of the error amplitudes due to the higher supply voltage. This normalized the trigger range to ±30 Least Significant Bits (LSB) for both supply voltages.

For a given LET, the cross section at 5.5 V was 1.5 to 3.5 times higher than at 2.7 V. The cross section vs. LET for the two supply voltages with the input code at 3482 are plotted in Fig. 4, with the cross section on a linear scale to help discern if the difference in response is due to differences in the critical LET or the saturated cross section [16]. At 2.7 V, the cross section may have been reached at an LET of 77 MeV-cm$^2$/mg, while at 5.5 V the cross section does not appear to be nearing saturation. Additional data are needed for it to be conclusive.

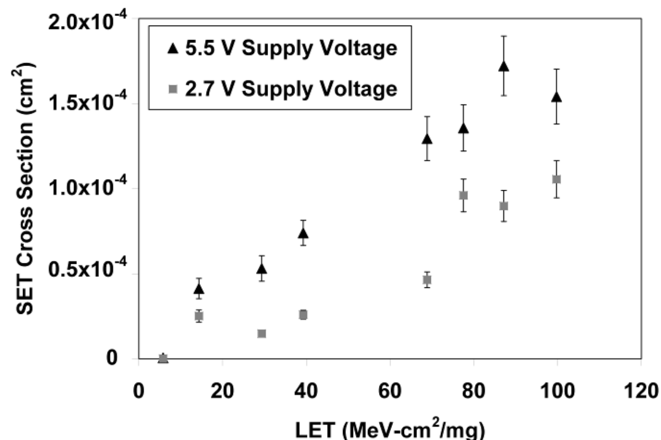


Fig. 4 SET cross section vs. LET with error bars for DUT 1 for supply voltages of 2.7 and 5.5 V. The input code was set at 3482.

### B. Simulation and Analysis of the Supply Voltage Effect

Many nodes were subjected to simulated ion strikes using a current injection model. The ion strike was modeled as a dual exponential current source with 50 ps rising τ, 500 ps falling τ and 1 mA peak current, which delivered 1 pC to the node under test. This is a first order model for a high LET ion strike [17][18]. When this current pulse was applied to nodes within the DAC, changes in output varied from a few mV to several hundred mV. The output variation was generally a voltage pulse, often with ringing. Nodes were tested within the resistor string, output buffer, and bias current source. In some cases, a node was equally sensitive with $V_A$ at either 2.7 or 5.5 V. In other cases, the change in output scaled with $V_A$. Several cases were found where the output disturbance with $V_A$ at 5.5 V was at least three times greater than with $V_A$ at 2.7 V, due to changes in the output buffer operating point. Examples are given in TABLE V, where the midscale input code was used.

TABLE V
VOUT CHANGES FOR SIMULATED ION STRIKE vs. $V_A$ (SUPPLY)

| Node | Pulse Amplitude $V_A$=5.5V | $V_A$=2.7V | Pulse Shape | Scaling |
|---|---|---|---|---|
| Pdriver | - 206 mV | - 131 mV | Pulse w/ ringing | Scales w/ $V_A$ |
| Ndriver | - 429 mV | - 144 mV | Pulse w/ ringing | Changes > $V_A$ |
| Top of Fine R | +121 mV | + 95 mV | Short pulse | Almost constant |
| Bias I input | - 12 mV | + 65 mV | Polarity changes | Changes >> $V_A$ |

Simulations showed that low impedance nodes tended to have small responses to the injected charge, since the charge could dissipate very quickly. Also, nodes within the resistor array that were not connected directly to the buffer showed small responses. This led to concentration on several high impedance nodes in the system, which included the buffer input (node Vinp in Fig. 3) and the output driver gates (nodes Pdrive and Ndrive in Fig. 3).

Consider the simplified buffer schematic in Fig. 3. Here the NMOS input pair MN1 and MN2 drives mirror-connected loads MP1 and MP2. All devices have adequate $V_{ds}$, at a $V_A$ of 5.5 V. However with $V_A$ at 2.7 V the load devices MP1 and MP2 move towards the knee between saturation and triode operation. This lowers their output impedances, which reduces both gain and the time constant at node Pdrive. Likewise, the PMOS input pair MP3 and MP4 drives NMOS mirrors MN3 and MN4 whose $V_{ds}$ drops with $V_A$ at 2.7V. This also reduces gain and the time constant at node Ndrive. With slower time constants and less gain, the amplifier responds more slowly to fast transients. This, along with the fact that charge from an ion strike can more easily dissipate with reduced device impedances, means the 2.7 V operating point has fewer detectable SETs than the 5.5 V supply voltage.

## VI. DEPENDENCE ON INPUT CODE

### A. Results

During the heavy ion testing, several different output transient signatures were seen. There were several types of positive-going transients, with examples shown in Figs. 5 and 6. There was just one type of negative-going transient (Fig. 7). For the negative-going transients, the pulse width was dependent upon the amplitude. Long pulse width negative-going transients were seen with the input at a lower scale (input code 614; 15% of full scale) and with the input at a higher scale (input code 3482; 85% of full scale), but were not seen at mid scale (input code 2048; 50% of full scale). The amplitude vs. pulse width for all of the transients from all ion runs for each of the input codes for DUT 1 are plotted in Figs. 8 to 10. The amplitude was calculated from the largest magnitude deviation from the nominal output. The pulse width was calculated from the number of samplings outside of the 20 mV window around the nominal output. This method resulted in some minor errors in the pulse width calculation of the positive-going transients with some oscillatory behavior but did not impact the pulse width calculations for the negative-going transients.

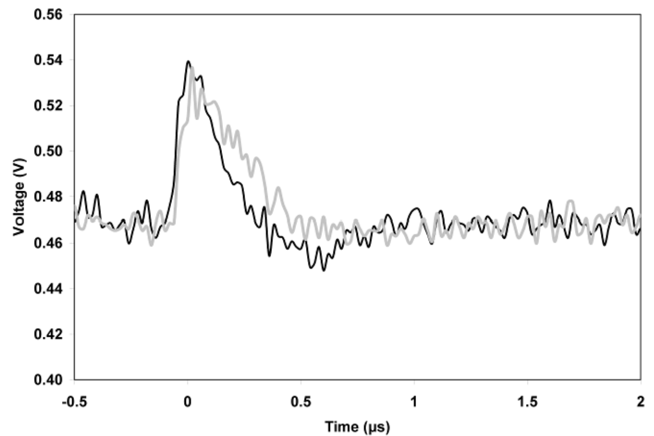


Fig. 5 Examples of long positive-going transients. These two transients were for a Ta run DUT 1 with $V_A$ = 2.7 V and input code = 614.

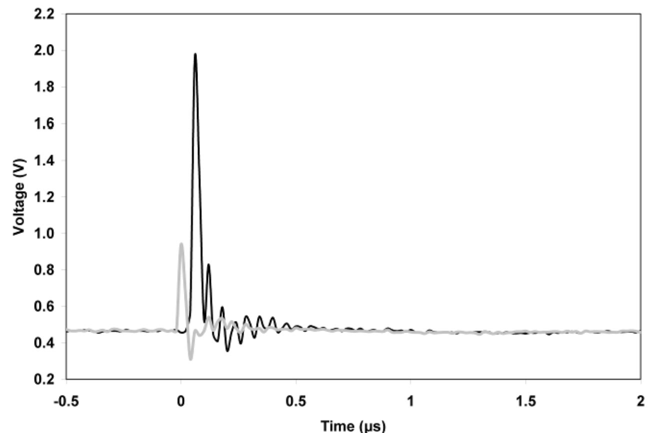


Fig. 6 Examples of short positive-going transients, followed by ringing. These two transients were for a Ta ion run for DUT 1 with $V_A$ = 2.7 V and input code = 614.

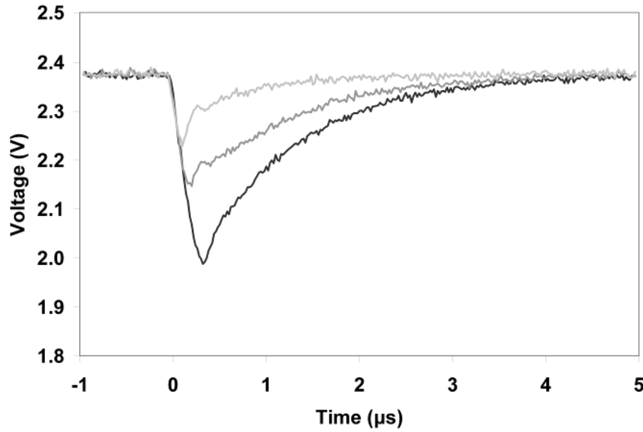


Fig. 7 Examples of negative-going transients. These three transients were from a Bi ion for DUT 1 with $V_A$ = 2.7 V and input code = 3482.

The binary code for the mid scale input, 2048 is mostly zeroes (100000000000). To determine if the long negative-going transients were dependent upon whether the input bits were high or low, the testing was repeated on DUT 4 with an input of 2047, which is a binary of code of mostly ones (011111111111). This testing was only done with the Ne and Ta ions. No long negative-going transients were seen with either of the input codes, 2047 or 2048 (Figs. 11 and 12).

While the major difference seen in Figs. 8 to 10 relates to long negative going transients, a smaller change is also present in Fig. 10. The short positive going transients at 85% of full scale are limited to about +0.4 V. This limit is simply imposed by $V_A$ as the output cannot exceed the supply, while at lower codes (and therefore lower output voltages) in Figs. 8 and 9 the short positive transients are not limited by $V_A$.

### *B. Simulation and Analysis of the Input Code Effect*

Simulations were run to investigate the long negative transients. Current injection was done to simulate an ion strike, using the current source model (dual exponential source, as described in section V.B.). Fig. 2 shows the basic chip architecture, and the point of current injection (Vinp). This node was suspect since many short channel length devices are connected together there. Simulations of ion strikes at other buffer nodes (Ndrive, Pdrive, Vout, Nbias and Pbias) did not produce long negative output transients regardless of input code. With 1 pC injected at node Vinp between the resistor string DAC and the output buffer, negative transients were observed lasting from 1 to 4 µs for input codes 614 and 3483 (15% and 85% of full scale). Fig. 13 shows the simulation waveforms at the chip output. With input code 2048 (50% of full scale) the negative transients were short pulses followed by ringing. Much of the ringing would be buried in noise during SEE testing, so only short negative transients were observed at mid scale.

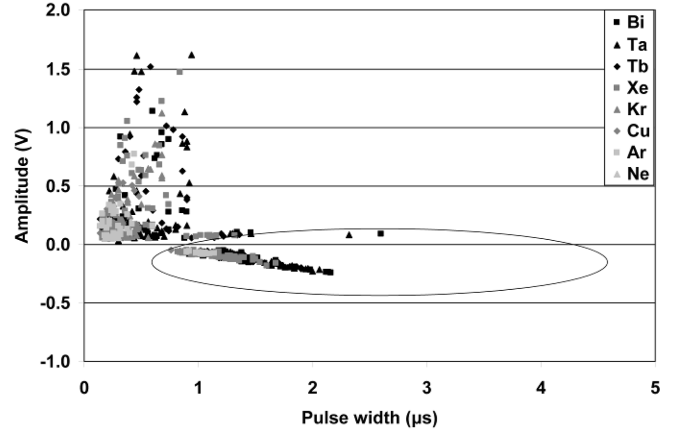


Fig. 8 SET amplitude vs. pulse width for input code 614, which is 15% of full scale, for DUT 1. Supply voltage was set at 2.7 V. Long negative-going transients are circled.

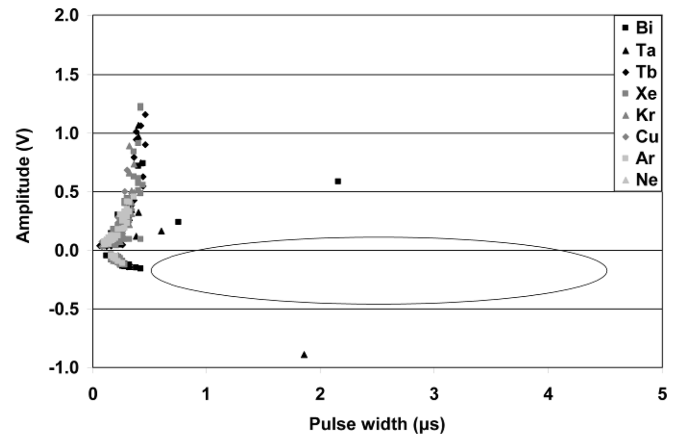


Fig. 9 SET amplitude vs. pulse width for input code 2048, which is 50% of full scale, for DUT 1. Supply voltage was set at 2.7 V. There were no long negative-going transients as were seen at lower and higher input codes.

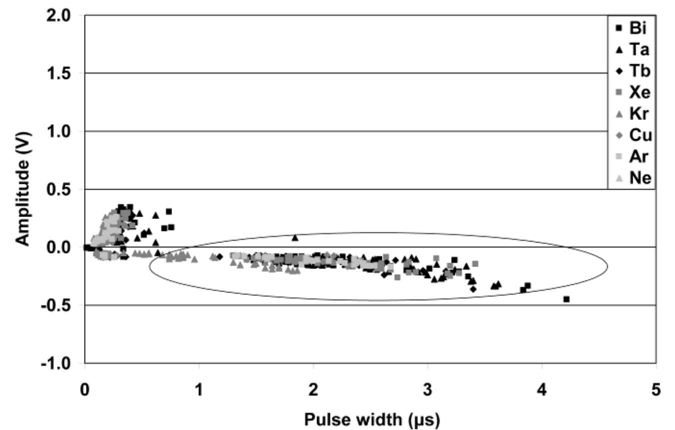


Fig. 10 SET amplitude vs. pulse width for input code 3482, which is 85% of full scale, for DUT 1. Supply voltage was set at 2.7 V. Long negative-going transients are circled. Amplitude of the positive transients is limited by the supply voltage.

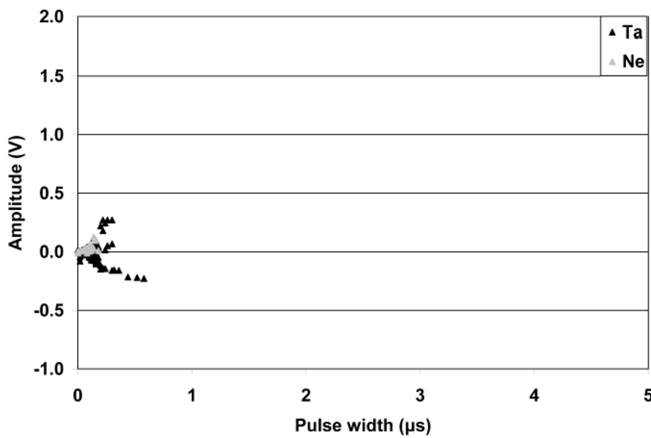


Fig. 11 SET amplitude vs. pulse width for input code 2047, which is binary code 011111111111, for DUT 4. Supply voltage was set at 2.7 V. No long negative-going transients were seen.

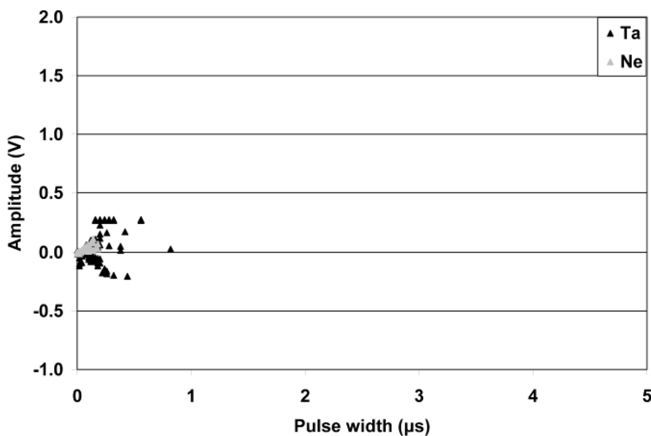


Fig. 12 SET amplitude vs. pulse width for input code 2048, which is binary code 100000000000, for DUT 4. Supply voltage was set at 2.7 V. No long negative-going transients were seen.

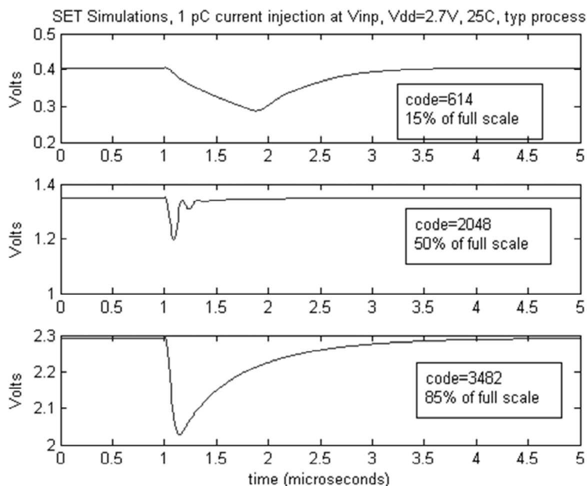


Fig. 13 Simulations of output voltage versus time for charge injection on node Vinp in Fig. 2 for three different input codes.

Near full scale only the NMOS input pair of the rail-to-rail buffer is active, while near zero scale only the PMOS input pair is active, so buffer gain-bandwidth is reduced in those regions of operation. The rail-to-rail buffer is fastest at mid scale, having both NMOS and PMOS input pairs active. At the same time, the impedance of the resistor string DAC is roughly 4 times lower at mid scale than that at 15% or 85% of full scale. Given the faster time constants at the buffer input (Vinp in Figs. 2 and 3), the system recovers faster at mid scale, so the negative transients have much shorter duration.

## VII. Conclusions

A mixed signal CMOS product, consisting of both digital and analog elements, has been shown to have unique and unexpected responses to single events. Through both testing and simulation, the analog circuit architecture was seen to have a significant impact on SET signatures.

For the DAC121S101WGRQV, the highest supply voltage is the worst case operating condition, resulting in the highest probability of an SET occurring. Simulations show that the dependence on supply voltage is due to differences in internal impedances and gain bandwidth.

The signatures of the SETs, especially the pulse width, are dependent on the input code but are not monotonic with the changes in code. This is due to the three operating regions of the output buffer. As indicated by the simulations, the system responds faster at mid scale, so transient pulse width is greatly reduced.

Other investigators have recently reported unexpected variation in SET response with supply voltage and operating point for high speed bipolar amplifiers [18]. While the changes in SET response due to operating conditions were not as abrupt as those seen in the CMOS DAC121S101QMLV, the presence of such changes emphasizes the need to characterize SET response in mixed signal devices over the range of operating conditions, guided by knowledge of the circuit architecture.

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