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## Single Event Upset Report

8 b Analog to Digital Converter  
2 Channel, 1.5 GS/s, 2.5 GHz Input Bandwidth, 1 W/Channel

**ADC08D1520WGFQV**  
**(5962F0721401VZC)**



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**Rev. B: Added Proton Testing and Clarified Test Method**

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## I. Abstract

The ADC08D1520WGFQV was evaluated for Single Event Upsets (SEU) under heavy ions and protons. The device was exposed to heavy ions with a linear energy transfer (LET) of up to 100 MeV/mg/cm<sup>2</sup> and to protons with energy of 198 MeV. The sample size for the testing was 3 units.

The ADC data output was monitored under both heavy ion and proton testing. The highest SEU cross section seen for the ADC data output was 7 x 10<sup>-4</sup> cm<sup>2</sup> per channel at 100 MeV/mg/cm<sup>2</sup>. Under heavy ion testing, an LET threshold was not determined as upsets were seen at the lowest LET tested (6 MeV/mg/cm<sup>2</sup>). Since the LET threshold was not determined, the ADC data output was also monitored under proton testing. No upsets were seen during the proton testing with energy of 198 MeV and fluence of 1x10<sup>10</sup> p/cm<sup>2</sup>. The total outage time due to single-event induced upsets for the data path was **6 ns/channel/month**. The total number of **events/channel/month** was **4x10<sup>-3</sup>**. The threshold for this calculation was set at 6 LSB. The longest event in the data path lasted **2460ns**.

The ADC output clock was monitored under heavy ion testing. The highest SEU cross section seen for the ADC clock output was 1x10<sup>-5</sup> cm<sup>2</sup>. The LET threshold for the ADC clock output was between 6 and 14 MeV/mg/cm<sup>2</sup>. Since an LET threshold was determined for the ADC clock output under the heavy ion testing, it was not monitored during the proton testing. The outage time for the LVDS clock was **2 ps/month**. The total number of events/month was **5x10<sup>-5</sup>**. The longest event in the clock path lasted for **198 ns**.

The ADC08D1520WGFQV was also tested under heavy ions for Single Event “hard errors”; those errors that result in permanent damage to the part or required the part to be reset to operate properly, such as Single Event Latchup (SEL) and Single Event Functional Interrupt (SEFI). The product was found to be immune to hard errors to the maximum LET tested (120 MeV/mg/cm<sup>2</sup>). The details of that testing are covered in a separate report [1].

## II. Product Description

The ADC08D1520WGFQV is a dual, high performance, low power monolithic analog to digital converter capable of converting analog input signals into 8-bit words at 1.5 GS/s (Gigasamples per second) [2]. It employs two 1.9 V dc power supplies (1.8 V to 2.0 V normal operating supply voltage range).  $V_{DR}$  is the power supply line for the output drivers and  $V_A$  powers the rest of the chip. Power consumption is 1 W per channel.

The ADC08D1520WGFQV has two control mode options, to set up the various configurations of the part, such as sampling mode, full scale range, offsets, and output clock settings. In “normal control mode”, the set up configuration is done through the control pins and the serial interface is disabled. In “extended control mode” the control pins are disabled and the part is configured through the serial interface.

Each channel (I and Q) has a differential input that supports frequencies up to 2 GHz. The differential inputs provide a full scale differential swing, selectable, of 650 mVp-p or 870 mVp-p input, or 560 mV to 840 mV in 512 steps when using extended control mode.

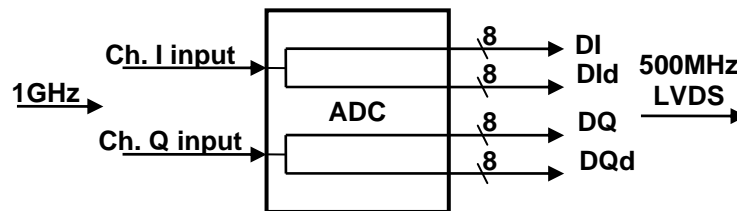
For optimal performance, the ADC08D1520WGFQV employs a calibration scheme. The part is automatically calibrated upon power up and can be calibrated on command through the CAL pin. The output format is offset binary. The output voltage is selectable to either 3 mA (normal LVDS drive) or 2.2 mA (reduced drive for reduced power consumption) into a 100  $\Omega$  differential load. There is also a Low Voltage Differential Signal (LVDS) clock output that runs at half the frequency of the input clock.

As shown in Fig. 1, the two independently operating 8 bit ADC's, called I and Q, convert the input synchronously using a single input clock.

Each of these converters has a 1:2 demultiplexer that feeds two LVDS output buses, called DI and DI<sub>d</sub>, and DQ and DQ<sub>d</sub>, for I and Q channel respectively.

The DI<sub>d</sub> and DQ<sub>d</sub> outputs are delayed by one clock cycle with respect to the DI and DQ outputs. Thus the digital outputs from the two ADCs are available on 4 separate LVDS 8-bit buses (current and previous sample for each channel clocked out at  $\frac{1}{2}$  the sampling rate).

The ADC08D1520WGFQV is fabricated using National Semiconductor's 180 nm CMOS9 process. The active areas are on a thin EPI layer on top of a very low resistivity substrate. From the top of the upper passivation layer, through the metal layers, active areas and EPI to the substrate is less than 11 microns.



**Fig. 1: ADC08D1520 input and output each channel has a 1:2 demultiplexer that feeds two LVDS output buses.**

### III. Test Method

JESD57 (EIA/JEDEC Standard No. 57), “Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation” was strictly adhered to for test procedures and definitions [3]. In addition, ESCC 25100 test procedures were also followed [4]. All testing was done at the ambient temperature of the facility. Due to self heating of the part during operation, the junction temperature of the device under test (DUT) was between 40°C and 50°C as measured by an on chip temperature diode.

#### A. ADC Data Output Test – Code Error and Beat Frequency Test Method

SEU of the ADC data output was monitored using a beat frequency and code error test method [5]. This allowed the ADC08D1520WGFQV to be tested at a sampling speed of 1 GS/s and with a dynamic input very close to 1GHz.

The device under test (DUT) was soldered to an ADC08D1000DEV board (Fig. 2) [6]. The output of the DUT was monitored by a Xilinx Vertex4 FPGA. The board was connected to a laptop computer through USB interface and was driven with National's WaveVision4 software, which also programmed the FPGA. The FPGA is in close proximity to the DUT and both are powered by an on board regulator to reduce noise and improve the integrity of the output signals. The DUT clock and inputs were driven by separate signal generators (Fig. 3). For heavy ion testing, a separate signal generator was used for each input, while for the proton testing a single signal generator was used, with the signal being split right before inputs. This setup enabled fast data acquisition, Fast Fourier Transform (FFT) and calculation of other critical parameters. Code Error Rate (CER) software was specifically incorporated into a dedicated version of WaveVision4 software to detect and record any SEU errors that occurred during the testing.



Fig. 2: ADC08D1000DEV board with decapped DUT.

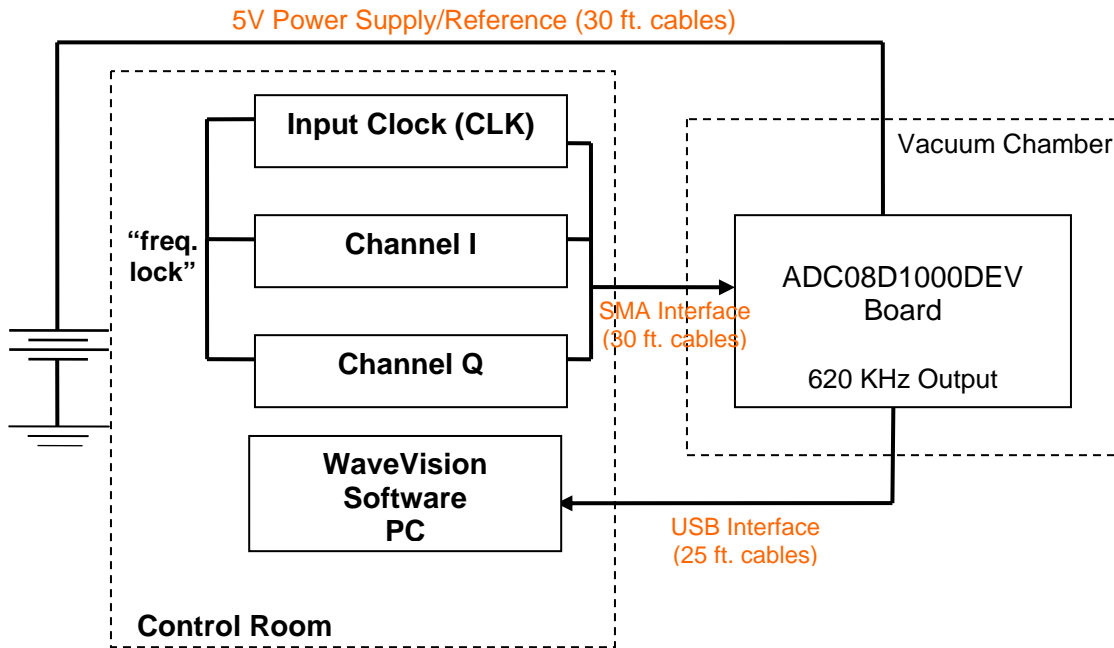


Fig. 3: Block Diagram of the CER test setup.

### A1. Code Error Rate Software

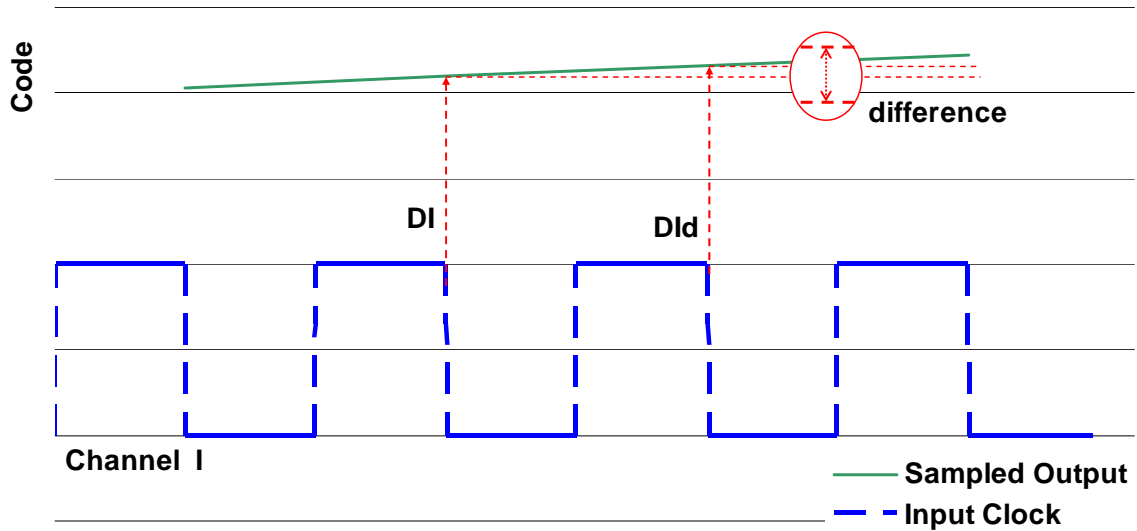
To trigger when an upset occurred, a Code Error Rate (CER) routine was programmed into the FPGA. The output of one channel was compared to the previous output. For instance, for the I channel, the DI output would be compared to the DI<sub>old</sub> output (Fig.4). If the difference between the two outputs was greater than a preset threshold, an error would be logged, that would include a timestamp in terms of the clock pulses (in this case 1ns), the current output reading and the previous output reading in binary code.

For the CER test, it was necessary to keep the expected change in the dynamic output to less than 1LSB, otherwise an invalid error would be recorded. The following equation was used to determine the output frequency required to get 1LSB change per clock cycle:

$$f_{\text{out}} = \frac{f_s}{2^N \pi}$$

where  $f_s$  was the sampling rate and N is the resolution of the ADC in bits.

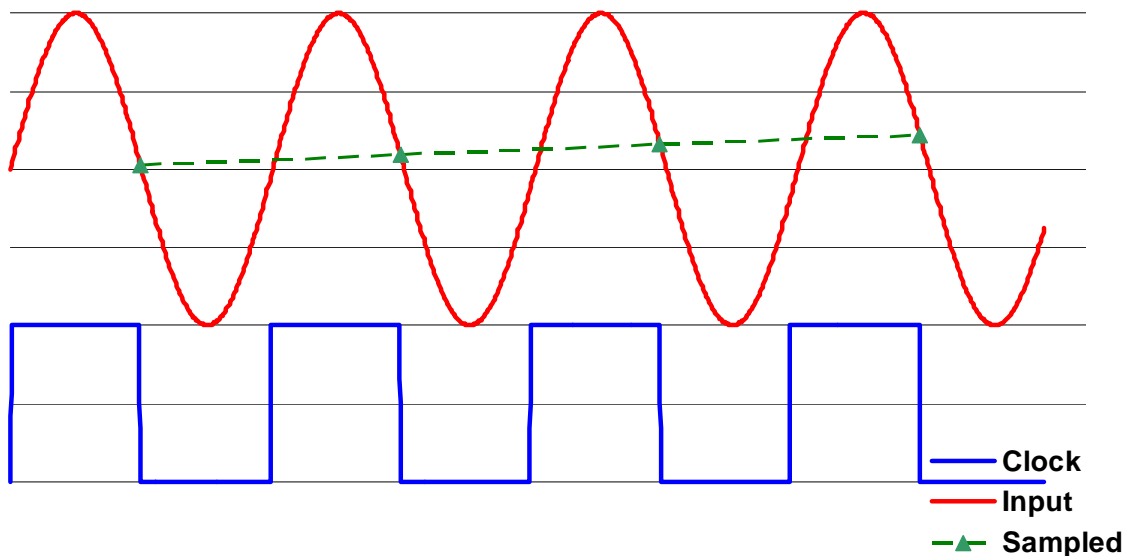
In this study, the ADC clock was run at 1 GHz for a sampling rate of 1 GS/s. According to the equation, the output frequency needs to be less than 1.24MHz. This was the output used for the proton testing. For the heavy ion testing, to compensate for the noisier environment and to have sufficient safety margin to be able to capture the code errors, the expected sampled output was cut in half to 620KHz. For proton testing, an output of 1.24 MHz was used.



**Fig. 4: Code Error Rate (CER) routine compares current output to previous output and records an error if the difference is greater than a preset threshold.**

## A2. Beat Frequency

If the input to an ADC is a constant frequency, the output, or beat frequency, will be the difference between the sample rate and the input frequency (Fig. 5). In this case with a sample rate of 1 GS/s and a desired output of 620 KHz, the input frequency was set to 999.38 MHz for the testing for the heavy ion testing. For the proton testing, with a desired output of 1.24 MHz, the input was set at 998.76 MHz.



**Fig. 5: Beat Frequency: Output or sampled frequency is the difference between the sample frequency and the input frequency.**

### **A3. Test sequence**

The clock and signal generators were powered up, the ADC08D1000DEV test board was powered up, and the WaveVision4 software loaded into the board through the laptop PC. The input generator levels were adjusted until the over range light on the ADC08D1000DEV board would blink and then were backed off until the light stopped blinking. An FFT would be run, using the WaveVision software, to verify that the board was running properly and the input levels were at full range.

The CER program was then loaded into the FPGA. The CER program was run without the DUT being exposed to the beam with the LSB threshold set at different values to determine the background noise. The test environment at Lawrence Berkeley National Labs, with the DUT inside a vacuum chamber, was very noisy, and it was necessary to set the LSB threshold at 6 (recording errors that were 7 LSB or greater) in order to avoid errors being registered from background noise. For proton testing, the LSB threshold was kept at 6 to maintain consistency in the testing.

The CER program is limited to 1000 error recordings per channel per run. At higher heavy ion energies, some single events could last many clock cycles. To ensure that a significant number of single events were captured, several ion runs were done for each ion at the higher ion energies.

### **A4. Test equipment**

- ADC08D1000DEV Board
- Function Generators:
  - 2 Rohde Schwarz SME 05
  - HP 8662A
- Oscilloscope Tektronix 744A with current probe
- Laptop computer with WaveVision4 software

### **A5. Test Condition Summary**

Normal mode configuration

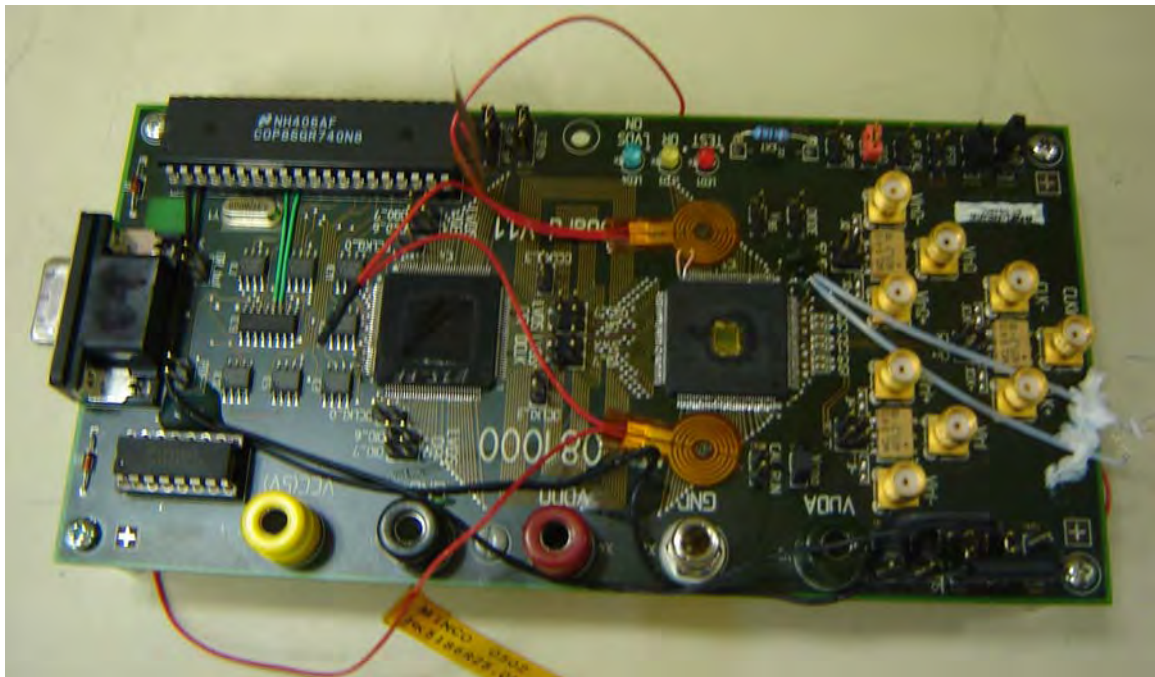
- Single Data Rate
- Input full scale 870 mV<sub>P-P</sub>
- No calibration delay

Clock: 1 GHz  
Inputs: 999.38 MHz Heavy Ion Testing  
998.76 MHz Proton Testing  
Outputs: 620 KHz Heavy Ion Testing  
1.24 MHz Proton Testing  
Power Supply: On board regulator (1.9 V nominal)  
CER Threshold: 6 LSB

## B. Output Clock Test

A different set up was used for monitoring the output clock than was used for monitoring the ADC data output. The ADC08D1000DEV board used to monitor the ADC data output did not have an easy access to the output clock, and adding any extra peripheral connections to the board would have added additional noise and degraded the ADC data output.

For the clock test, the DUT was soldered to an ADC081000 Eval Board V1.1 (Fig. 6). Separate power supplies were connected to the two supply lines,  $V_{DR}$  and  $V_A$ . The power supplies were adjusted until the supply lines at the input to the board were at 2.0V. The supply currents were monitored on the power supply current readouts, and with current probes on the supply cables that ran from the power supply to the board. The ADC081000 Eval Board V1.1 was powered by an independent 5V source.



**Fig. 6: ADC081000 Eval Board V1.1 with decapped DUT.**

Separate signal generators were connected to the ADC clock and I and Q channel inputs (Fig. 7). The I channel input was set at 373 MHz, while the Q channel input was set at 173 MHz. Different frequencies were used to reduce any effects from harmonics and cross talk.

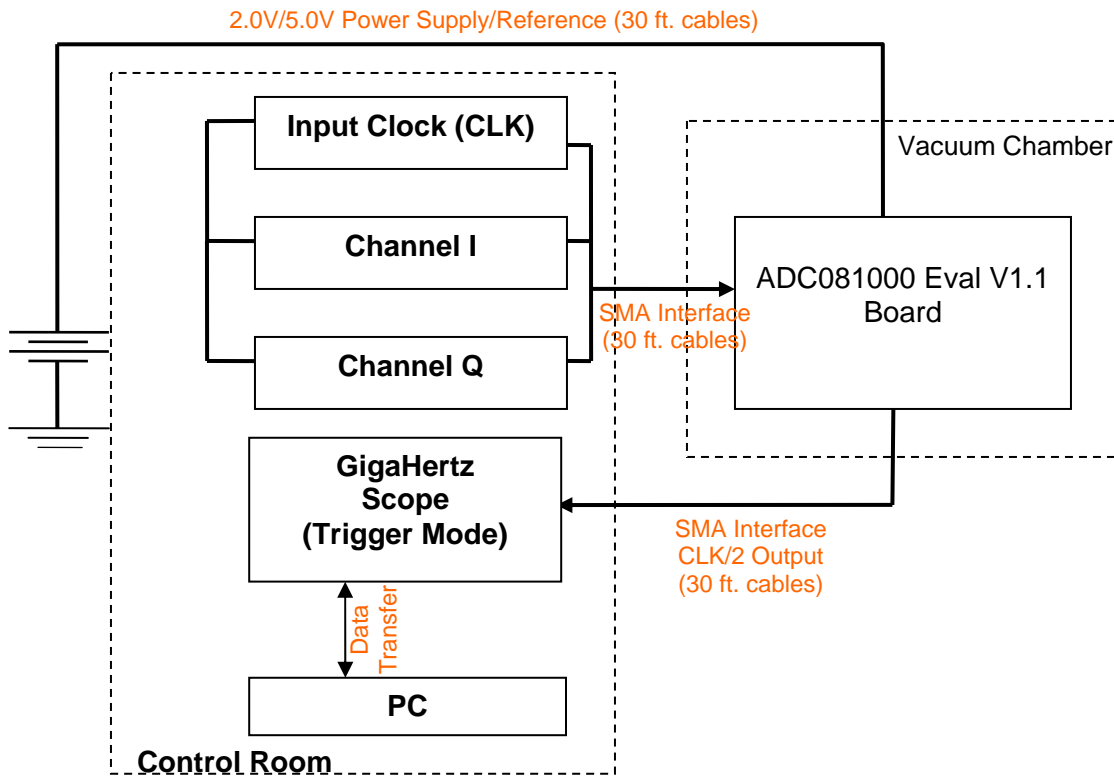


Fig. 7: Block Diagram of the Setup for Clock Test.

### B1. Clock Output Monitor

A differential probe was connected to the LVDS clock output. The probe was connected to the Tektronix 7404B oscilloscope through a probe amplifier. The clock output provides a signal that is identical to the clock input and locked at half of the frequency. Since a differential probe and a probe amplifier were used, and the amplifier was connected to scope through a 30 foot cable, the output signal was centered at 0 V and was scaled down to  $\pm 0.25$  V. In order to capture the single event upsets at the LVDS clock output, the scope was set on a “width” trigger mode. A  $\pm 5\%$  margin of the clock output signal was used to determine the *upper* and *lower limits* (Fig. 8). Since the clock output was at 500 MHz, the upper and lower limits were set at 1100ps and 900ps respectively.

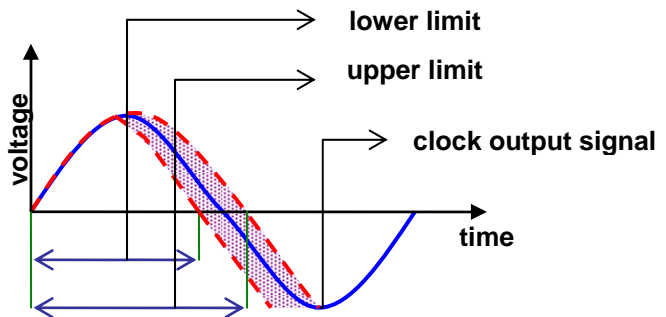


Fig. 8: Trigger setting for LVDS clock output.

## **B2. Test Sequence**

At the beginning of each run, the scope memory was cleared by pressing the reset button. The scope was then set to “width” trigger mode with appropriate upper and lower limits. The sampling resolution was set to 200 ps per data point. A total of 2000 samples were taken, i.e. the total length of the captured window was 400ns during a trigger event.

The ion beam was shut off after reaching a fluence level of  $1 \times 10^7$  ions/cm<sup>2</sup>. The output data for the triggered events, and time stamp for all the triggers, were then uploaded to the computer.

## **B3. Test Equipment**

- ADC081000 Eval Board V1.1
- Function Generators:
  - 2 Rohde Schwarz SME 05
  - HP 8662A
- Oscilloscope Tektronix 744A with current probe
- Tektronix TDS 7404B Digital Phosphor Oscilloscope
- Triple power supply with current display for 2 channels - Instek PC 3030D
- 5 Digital Multi-meter - Fluke 8050A

## **B4. Test Condition Summary**

Normal mode configuration

- Single Data Rate
- Input full scale 870 mV<sub>P-P</sub>
- No calibration delay

Clock: 1 GHz

Clock output: 500 MHz

Input I channel: 373 MHz

Q channel: 173 MHz

Power Supply: Remote power supplies (set at 2.0V at board level)

## **C. Heavy Ion Testing**

### **C1. Sample Preparation**

ADC08D1520WGFQV die were assembled into 128 pin LQFP plastic packages. The packages were de-capped to expose the die surface to the ion beam. The de-capped units were soldered to the ADC081000 Eval Boards V1.1 or ADC08D1000DEV Boards.

The sample size was 3 units for each test.

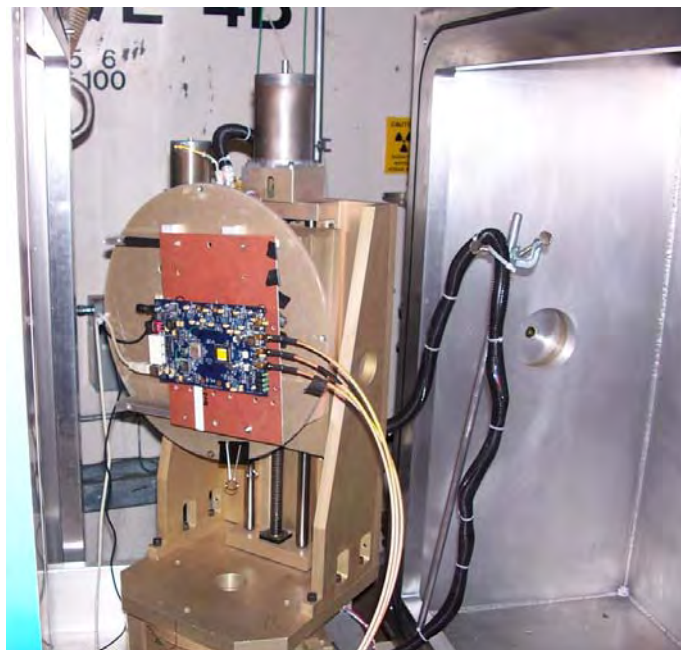
### **C2. Test Facility and Date**

The test facility for heavy ion testing was the 88" Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) located in Berkeley, California [7]. The 4.5 MeV/nucleon beam was used (see Appendices A and B for ion energies and penetration depths).

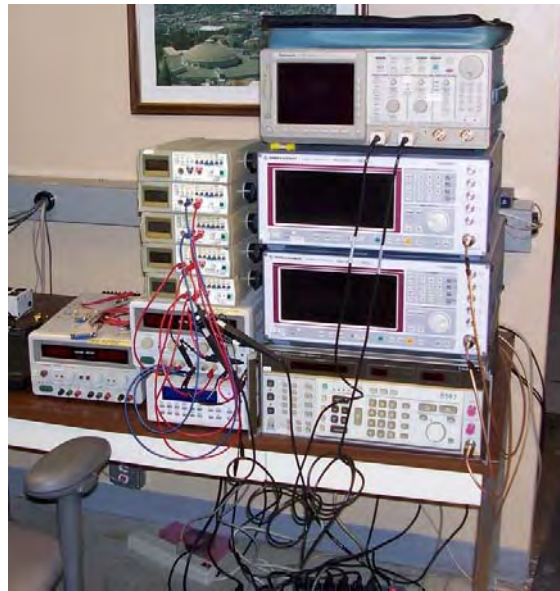
The testing was performed on May 16, 17 and 18 of 2007.

### **C3. Setup**

The test boards were mounted inside the vacuum chamber (Fig. 9). All of the test equipment, except the probe amplifier, was located outside the vacuum chamber, upstairs in the control room (Fig. 10). Special feed-throughs were developed to connect the equipment to the test boards through the vacuum chamber.



**Figure 9: Inside the vacuum chamber (picture from previous experiments with ADC08D1000).**



**Fig. 10: Measurement setup in the control room.**

## **D. Proton Testing**

### **D1. Sample Preparation**

ADC08D1520WGFQV die were assembled into 128 lead WG hermetic packages using the MIL-STD-38535 class V process flow. The packages were soldered on to ADC08D1520DEV boards.

The sample size was 3 units.

### **D2. Test Facility and Date**

The test facility for the proton testing was the Indiana University Cyclotron Facility in Bloomington, Indiana [8]. The 200 MeV proton beam (actual energy: 198MeV) was used with flux range between  $1.0 \times 10^7$  to  $1.7 \times 10^7$  p/s  $\text{cm}^2$ . The 1 inch copper collimator was used to focus the ion beam on the DUT and prevent other components on the board from getting proton irradiation.

Testing was performed on December 11, 2008 between.

### **D3. Test Setup**

The ADC08D1000DEV board was attached to a holding plate, which was held in front of the beam by a vise (Fig. 11). Shielding was placed around the beam path to the board to prevent the proton beam from impacting other components on the board (Fig. 12 and 13). To protect the components on the board, especially the FPGA, from secondary neutrons, shredded pieces of borated polyethylene were put between the test board and

holding plate (Fig.11) and a slab of borated polyethylene was taped to the front side of the test board, covering the FPGA (Fig. 14).

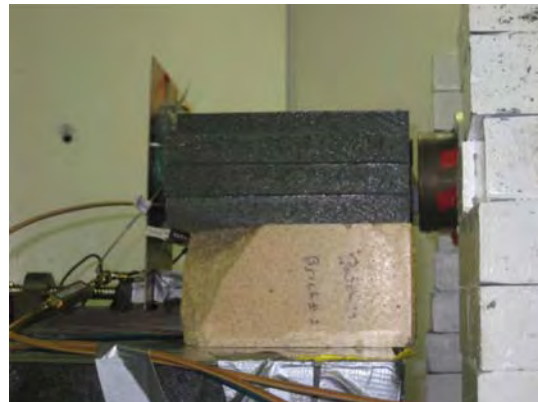
The signal generators and laptop computer were placed behind a brick wall. The laptop computer was networked and controlled by a second laptop computer in the control room.



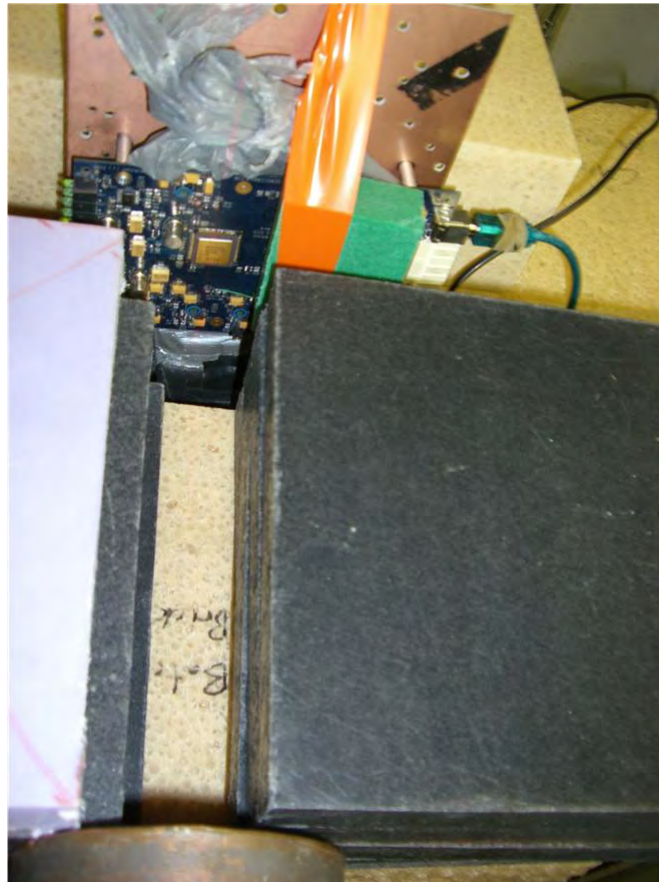
**Fig. 11: Test board attached to holding plate, with bag of shredded borated polyethylene between the board and plate to shield from secondary neutrons.**



**Fig. 12: Backside of board with beam line shielding.**



**Fig. 13: Side view of board and beam line shielding.**



**Fig. 14: Topside view of beam line. Borated polyethylene slab was taped over the FPGA to protect it from secondary neutrons.**

## IV. Results

### A. ADC Data Output Test Results – Proton Testing

Proton testing was done on three units at an energy of 198 MeV, with the flux ranging from  $1.0 \times 10^7$  to  $1.7 \times 10^7$  p/s  $\text{cm}^2$ . The irradiation was not always continuous as the proton beam was occasionally diverted for medical treatments at the Indiana University facility. Each unit received a total fluence of  $1.0 \times 10^{10}$  p/ $\text{cm}^2$ . No upsets to the entire test system were seen during this testing. There was one upset to the FPGA, where it locked up for less than 1  $\mu\text{s}$ , during an experimental run with the clock set at 400 MHz.

No ADC data output errors were recorded during the proton testing.

### B. ADC Data Output Test Results – Heavy Ion Testing

Heavy ion testing of the ADC data output was done on three units using different ions with LET ranging from 5.76 to 99.85 MeV/mg/ $\text{cm}^2$  (see Appendices A and B for ion LET and penetration depths).

Errors were seen at each ion LET tested.

#### B1. Code Error Rate vs. Bit Error Rate

For digital products, it is common to report errors in terms of bit error rate. For an ADC, the whole output code is important and each bit will have a different impact on the output code. For this reason, it is of more value to report errors in terms of code errors instead of bit errors.

The output of the CER program is binary and was converted to decimal. All errors are reported in terms of the complete output word or code (0 to 255) and not in terms of bit errors. This does result in the error cross sections being calculated 8 times higher than if the errors were reported in bits.

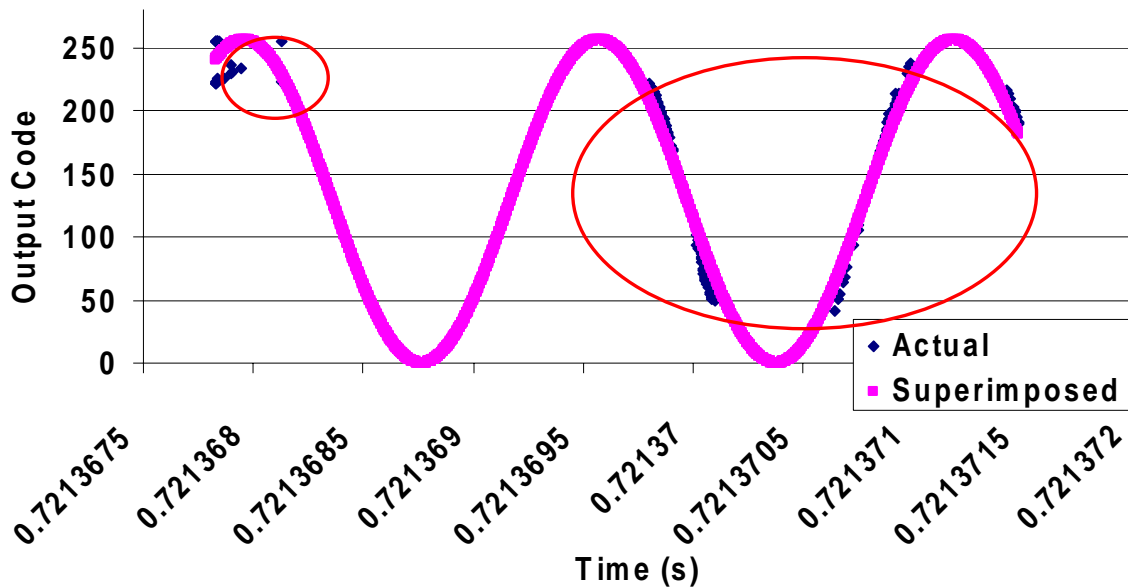
The magnitude of the errors were independent of the LET.

#### B2. Event Length

Since the CER program compares successive output readings, two errors would be registered for a single event lasting one clock cycle, one for when there was an erroneous output code and one for when the output code returned back to the expected reading. Events that lasted for less than 2ns in duration were considered to be emanating from a strike to the digital circuitry of the ADC such as registers, flip-flops, logic-gates etc. and defined as DSET's (Digital Single Event Transients).

There were cases where errors were recorded for many consecutive clock cycles. These cases were considered to be one event, lasting longer than 1 ns. In some cases there would be a set of consecutive errors, followed by a gap of no errors less than 1  $\mu\text{s}$

long, followed by another set of consecutive errors (Fig. 15). These cases would also be considered one long event, since at the fluxes used, the average time between ion strikes was greater than 3  $\mu$ s. The gap where errors were not seen was added into the total time of the event. These longer events were considered to be generated from strikes to the analog components due to the slower recovery time and were defined as ASET's (Analog Single Event Transients).



**Fig. 15: Example of an ASET. The time stamp, converted to seconds, is listed on the x-axis. The actual ADC data output reading, converted from binary to decimal is shown in blue. The expected output (at a frequency of 620 KHz) is “Superimposed” over the data and shown in red.**

DSET's and ASET's were seen at each ion tested. The maximum ASET length seen for each ion was dependent upon the LET up to an LET of 77 MeV/mg/cm<sup>2</sup> (Fig. 16). Above that level, the maximum ASET, did not significantly increase with LET. The longest ASET seen during the testing was 2460 ns. The average event length seen at each ion energy was somewhat dependent upon on LET. Fig. 17 shows the average event length (including both DSET's and ASET's) for the 3 units tested.

### B3. Error Magnitude

The magnitude of the errors ranged from 7 LSB, the threshold limit for detection, to 250, nearly the full output range (Fig. 18 and 19). The magnitude of the errors was independent of the LET (Fig. 19).

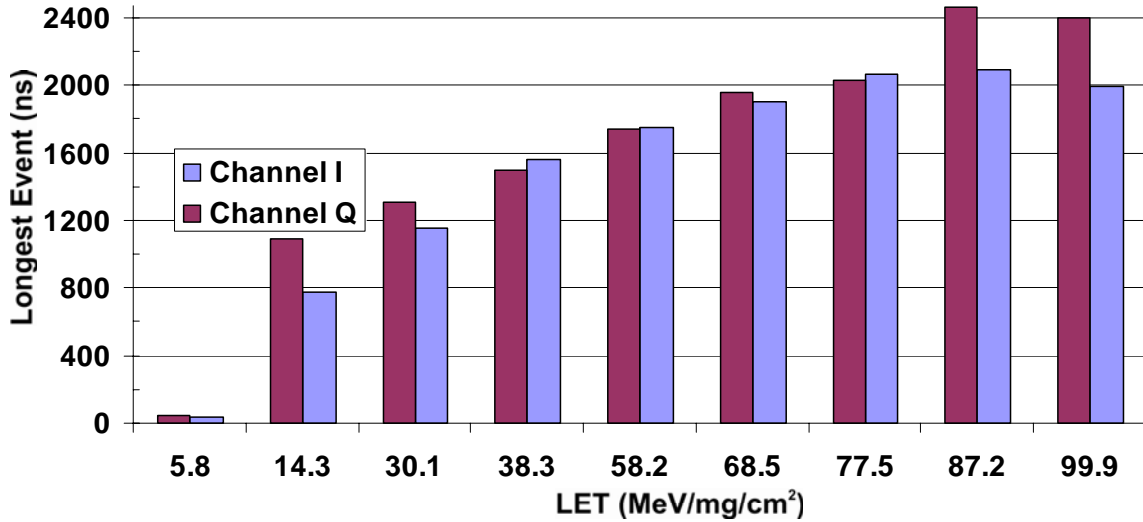


Fig. 16: Longest ADC output data ASET seen at each LET for the 3 samples tested.

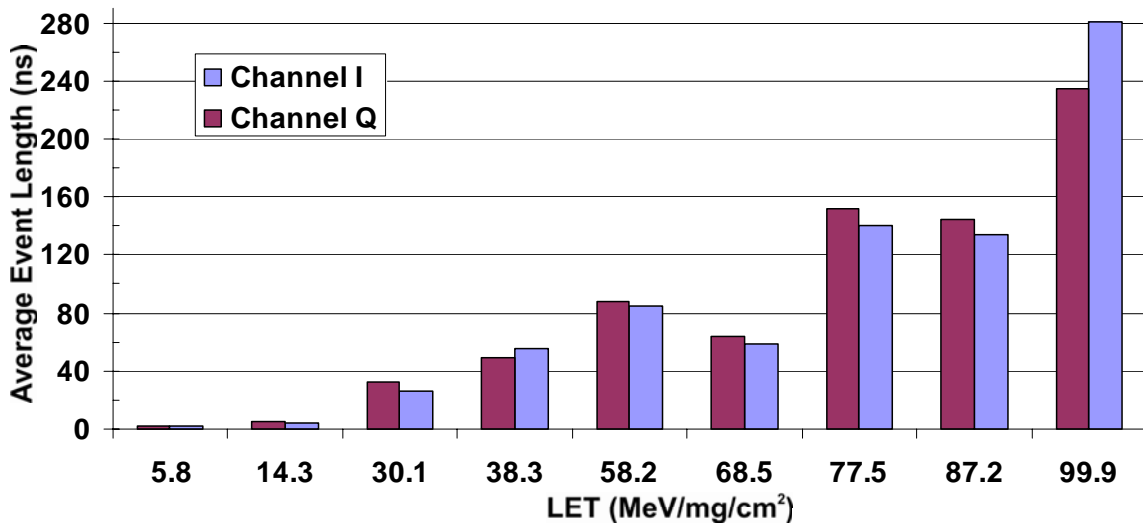


Fig. 17: Average length of ADC data output upset event per LET for each channel.

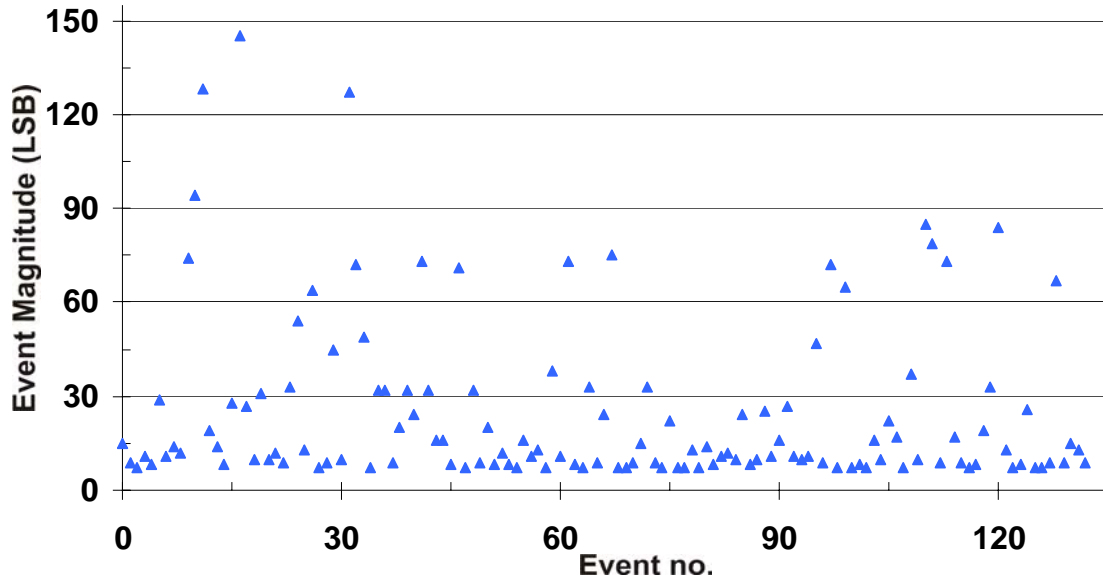


Fig. 18: Magnitude of error for threshold over 6LSB due to an Argon ion strike on Channel I

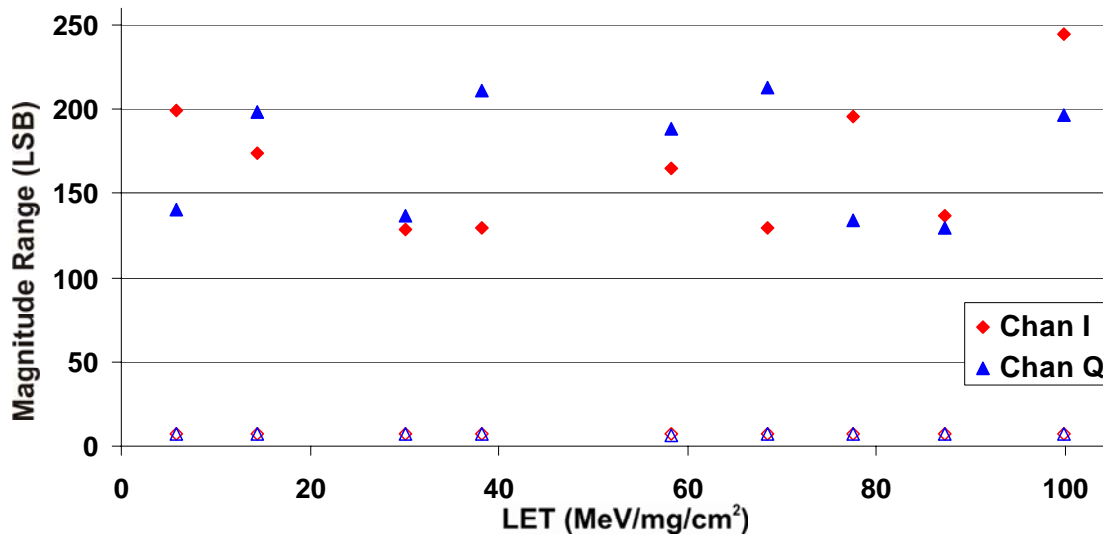


Fig. 19: Maximum (solid triangle and diamond) and minimum event error (open triangle and diamond magnitude) seen per LET for all 3 units tested.

## C. Output Clock Results – Heavy Ion Testing

Heavy ion testing of the output clock was done on three units using different ions with LET ranging from 5.76 to 99.85 MeV/mg/cm<sup>2</sup> (see Appendices A and B for ion LET and penetration depths).

No clock errors were seen at 5.76 MeV/mg/cm<sup>2</sup>, but were seen at the next LET tested, 14.33 MeV/mg/cm<sup>2</sup>.

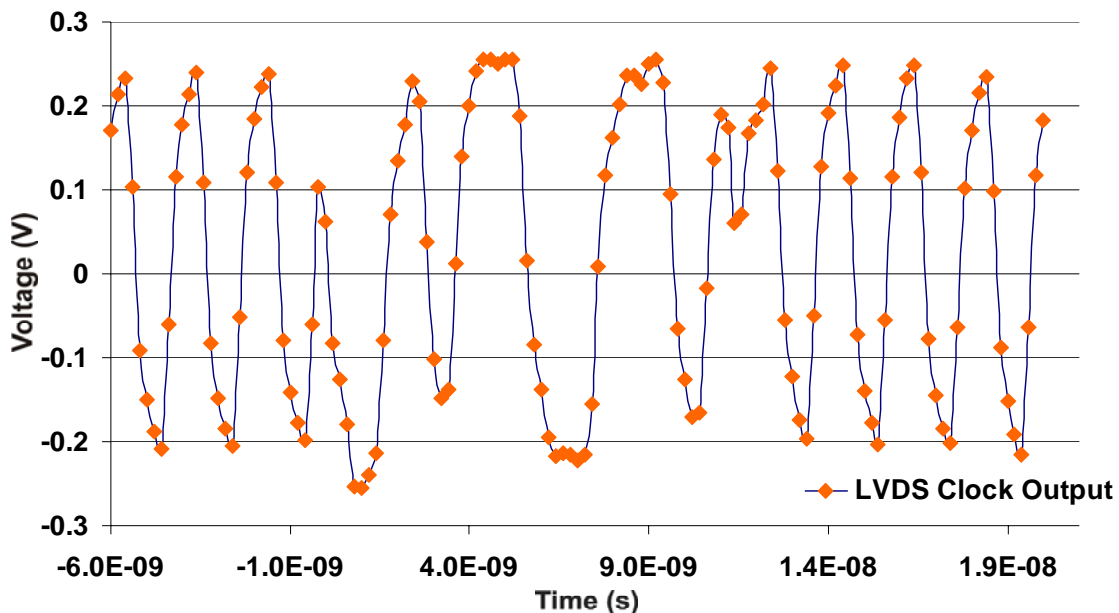
Since an LET threshold for the output clock was found, the output clock was not monitored during proton testing.

### C1. Output Clock Error Signatures

The output clock single event upsets recorded by the oscilloscope were divided into three categories: disrupted output, phase shift and attenuation.

### C2. Output Clock Disrupted

Fig. 20 is an example of the output being disrupted for several clock cycles after an ion strike. During this disruption, the output is no longer a clean sine wave. Sometimes, the signal could be stuck high or low for one clock cycle, but the output would eventually recover and still be in phase.



**Fig. 20: Example of the output clock being disrupted for several clock cycles. This one was caused by a Bi ion strike.**

### C3. Output Clock Phase Shift

In some cases, an ion strike could cause the output clock to be stuck high or low for one or more clock cycles. When the output clock would recover, it would be 180° out of phase (Fig. 21 and 22). The output clock runs at half the frequency of the input clock. On power up, the output clock locks on the “first” input clock cycle. After the ion strike, the output clock would relock on the “second” input clock cycle.

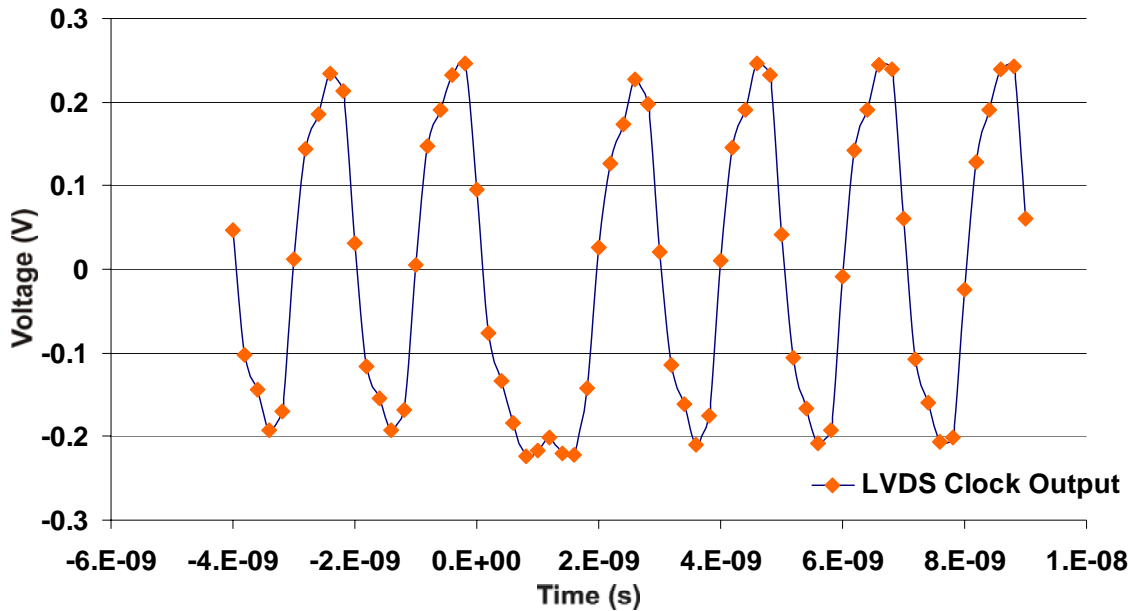


Fig. 21: Output clock stuck low for one clock cycle and then relocking 180° out of phase from the original output signal. From Bi ion strike.

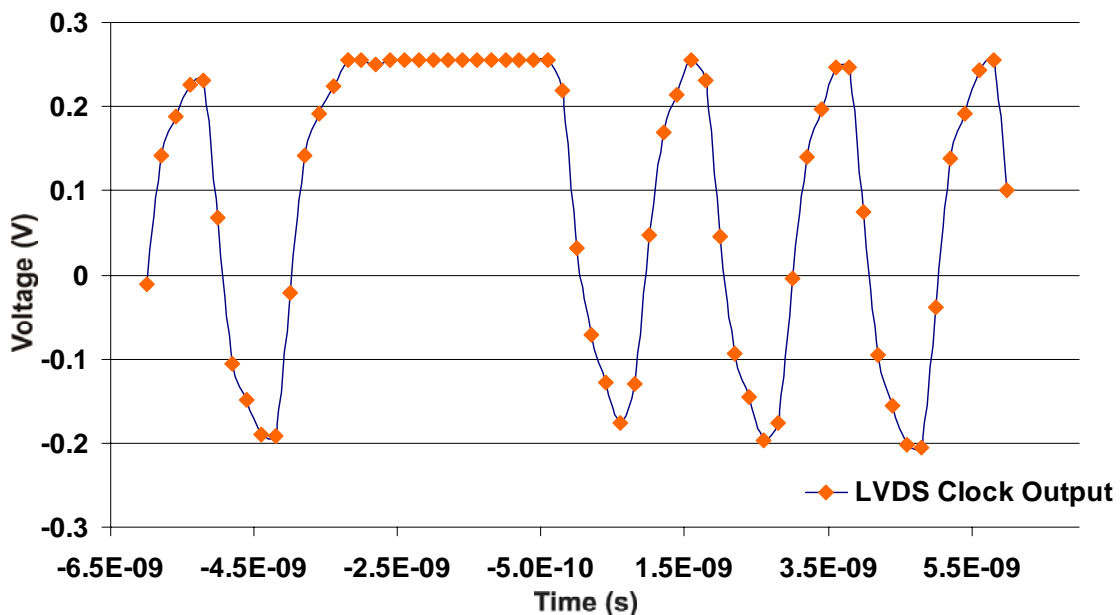


Fig. 22: Output clock stuck high for several cycles and relocking 180° out of phase from the original output signal. From Bi ion strike.

#### C4. Output Clock Attenuation

The most common cause for a scope trigger was due to attenuation of the output clock signal (Fig. 23). Although the differential output signal was attenuated, there were no other disruptions to the signal and there was no phase shift (Fig. 24).

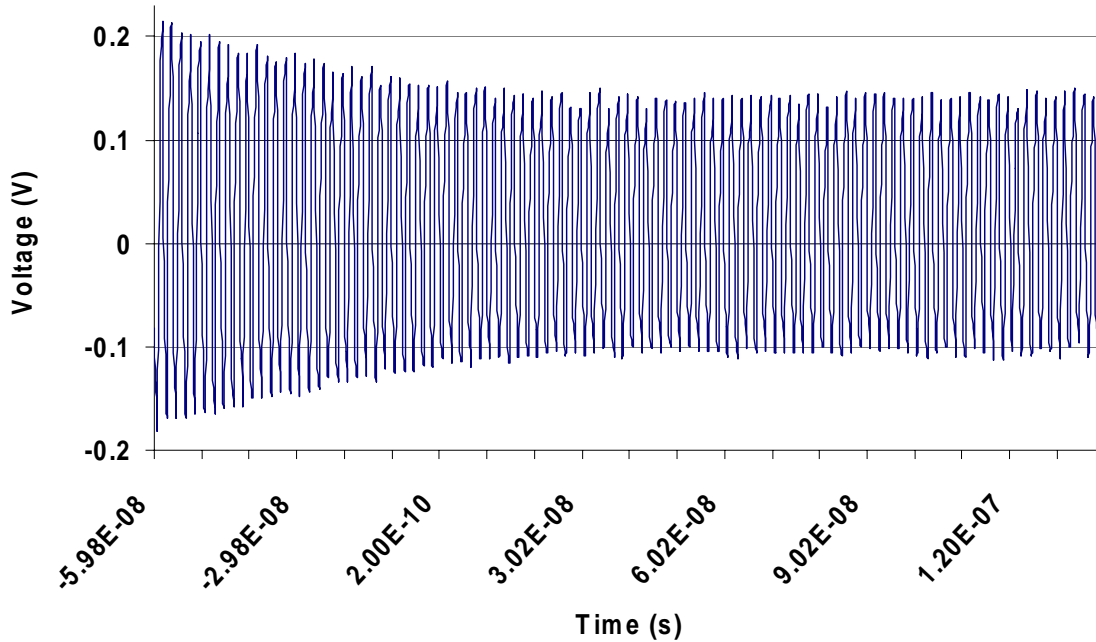


Fig. 23: Clock output signal attenuation caused by Bi ion strike.

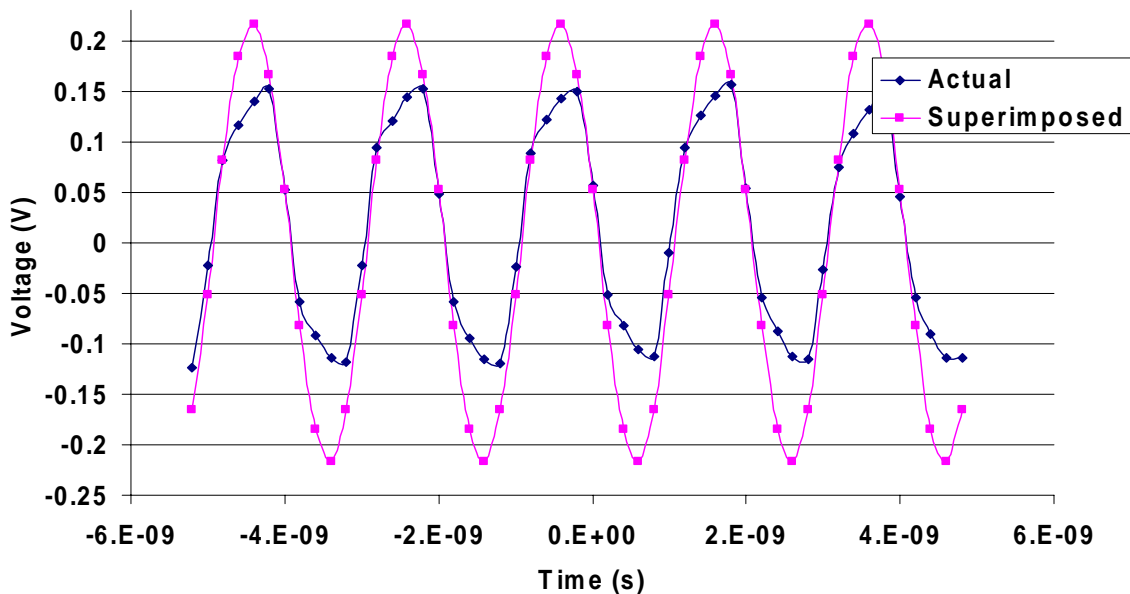
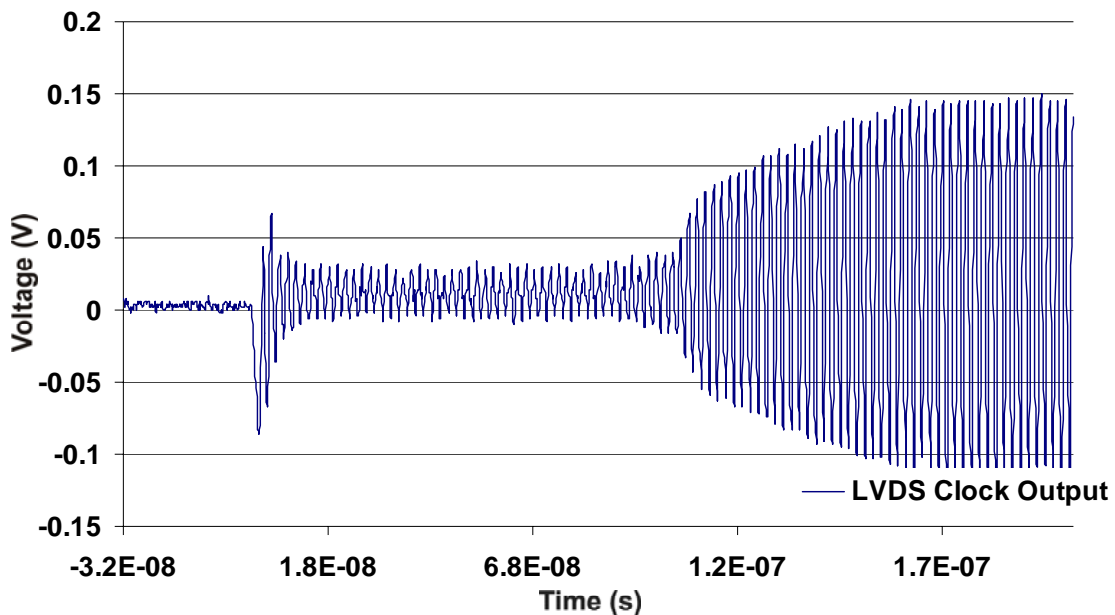


Fig. 24: Zoom in on the attenuated clock output signal from Fig. 23. The actual output captured by the oscilloscope is in blue. The expected output, seen before the ion strike is “superimposed” in red.

In most cases, the output clock signal attenuation was not significant enough to cause a problem in the downstream circuitry (i.e. the differential voltage remained larger than the datasheet spec limit [1]). For a few events, the attenuation was severe (Fig. 25).

Since the differential probe monitoring the output clock was connected to the oscilloscope through a probe amplifier and then 30 feet of cable, the output seen at the scope was centered on 0 V and scaled down. To evaluate this data, the differential output limit listed in the datasheet was similarly scaled down to  $\pm 80$  mV. A routine was written into PERL to evaluate the frames captured by the scope. Any scope captures where the attenuation was not great enough to drop the differential output below the limit, were not included in the event count.



**Fig. 25: Output clock signal attenuated by an ion strike. This was counted as an event.**

### C5. Output Clock Event Length

Most of the upsets seen on the output clock were relatively short in length, lasting one to ten clock cycles (2 to 20 ns). Some of the attention upsets had long times, lasting over 100 ns. The longest event seen was 198 ns. The average length of the events and the longest event for each LET are shown in Fig. 26.

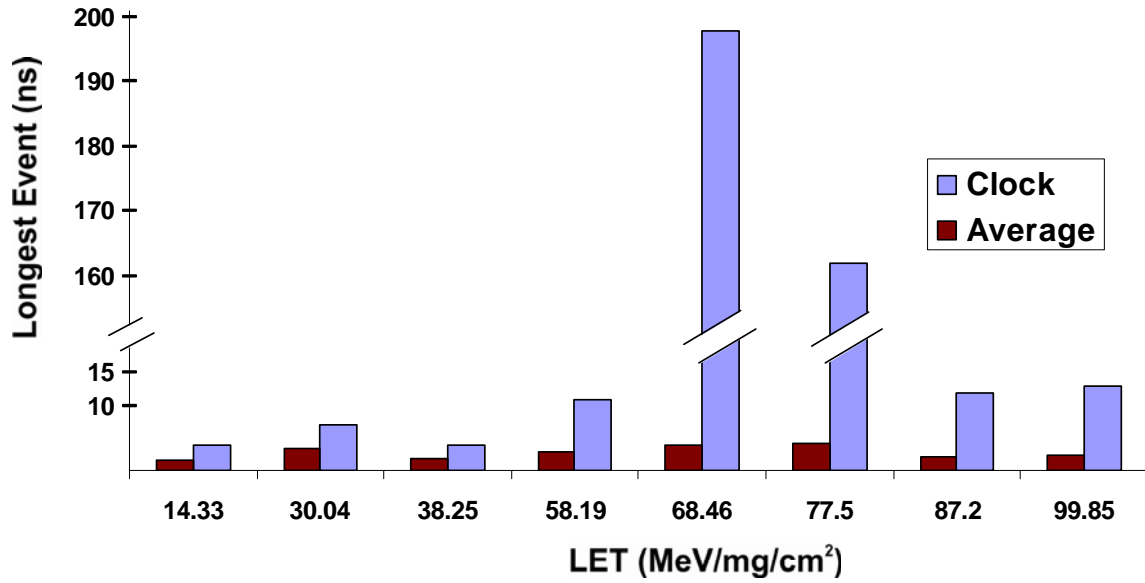


Fig. 26: Average length of a clock output upset in red and the longest clock output upset recorded for each LET in blue.

## V. Analysis of the Results

### A. Analytic Tools

The probability of an event occurring for a certain ion energy is graphically represented by plotting the event cross section vs. the ion LET. The cross section is calculated by dividing the number of events recorded during an ion run by the fluence for a particular LET. A Weibull distribution [9] is used to statistically characterize the failure behavior of the device. Furthermore, a figure of merit (FOM) equation [10] is used to predict the monthly upset rate of the ADC. In all cases, event cross sections and FOM results are expressed in total output code errors and not errors per bit. Reporting in errors per bit would lower the cross section by a factor of 8.

#### A1. Weibull Distribution

The integral form of the distribution that describes the event cross-sections as a function of LET is:

$$F(L) = A \left( 1 - \exp \left\{ - \left[ \frac{L - L_0}{W} \right]^s \right\} \right); L > L_0$$

$$F(L) = 0; L < L_0$$

where, **F(L)** is the event cross-section for a particular LET

**A** is the limiting cross-section

**W** is the width of the distribution

**L<sub>0</sub>** is the threshold LET

**s** is the shape parameter

For the ease of calculation,  $L_0$  was set to 0 and  $W$  was set to 100. For the ADC output data, the threshold LET was not found, and 0 was an appropriate value to use. For the output clock, the threshold LET was between 6 and 14 MeV/mg/cm<sup>2</sup>. Changing  $L_0$  had little impact on the curve fitting and the impact on the FOM calculations was less than  $\pm 20\%$ . Keeping  $L_0$  at 0 simplified the calculations and resulted in worst case FOM. The values of  $A$  and  $s$  were adjusted to fit the actual data.

#### A2. Monthly Events

The following figure of merit [10] was used to characterize the monthly number events per channel for the data path and number of events per month for the LVDS clock output.

$$FOM = 30 \times 200 \times \frac{\sigma_{limit}}{L_{0.25}^2}$$

where,  $\sigma_{limit}$  is the limiting cross-section

$L_{0.25}^2$  is the LET at 25% of the limiting cross-section

The multiplication by 30 in the FOM was used to get the monthly number of events. The variables are taken from the Weibull plot.

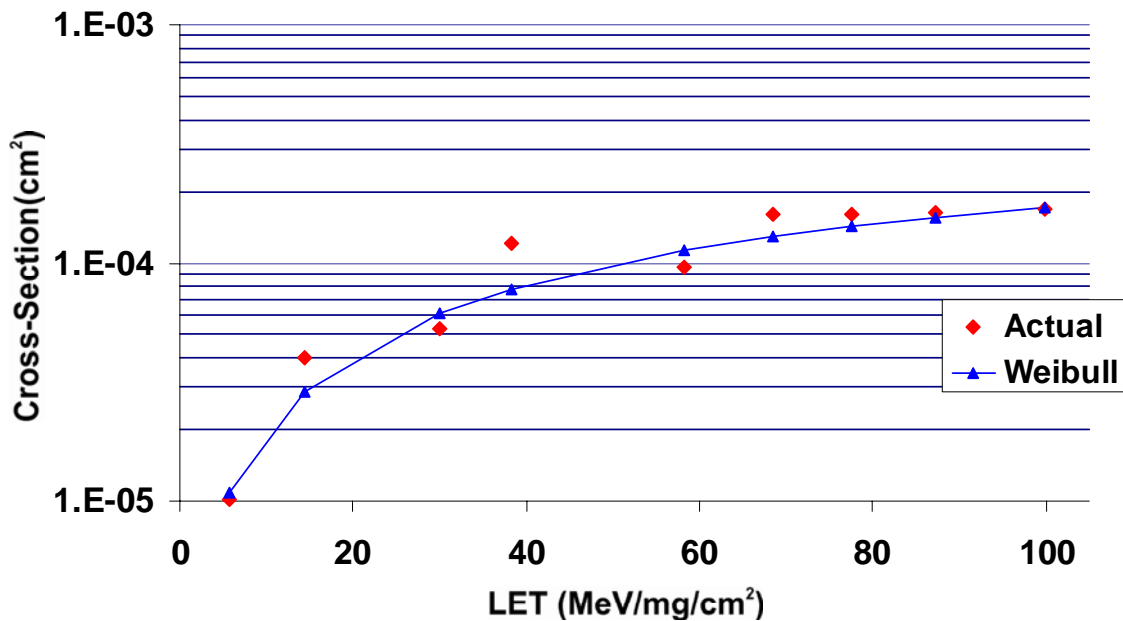
### A3. Total Monthly Accumulated Event Time

The total monthly accumulated event time, i.e. monthly outage time, was calculated by multiplying the FOM with the average of the longest upset lengths for all the ion strikes.

## B. ADC Data Output

### B1. Cross Section vs. LET

Figs. 27, and 28 show the cross section vs. LET and Weibull plots for the average ASET and DSET of the ADC data output per channel. DSET and ASET events for both channels were calculated separately for each of the 3 units tested, and then averaged to determine the event cross-section per channel. Fig. 29 shows the combined event cross section per channel with error bars that show the maximum and minimum event cross section for both channels and all 3 units. Cross sections are expressed in total code errors and not errors per bit. Expressing the events in errors per bit would lower the cross sections by a factor of 8.



**Fig. 27: ADC data output DSET cross section vs. LET per channel. The cross section is an average of both channels for all 3 units tested. For the Weibull plot parameters,  $A=0.00027$  and  $s=1.12$ .**

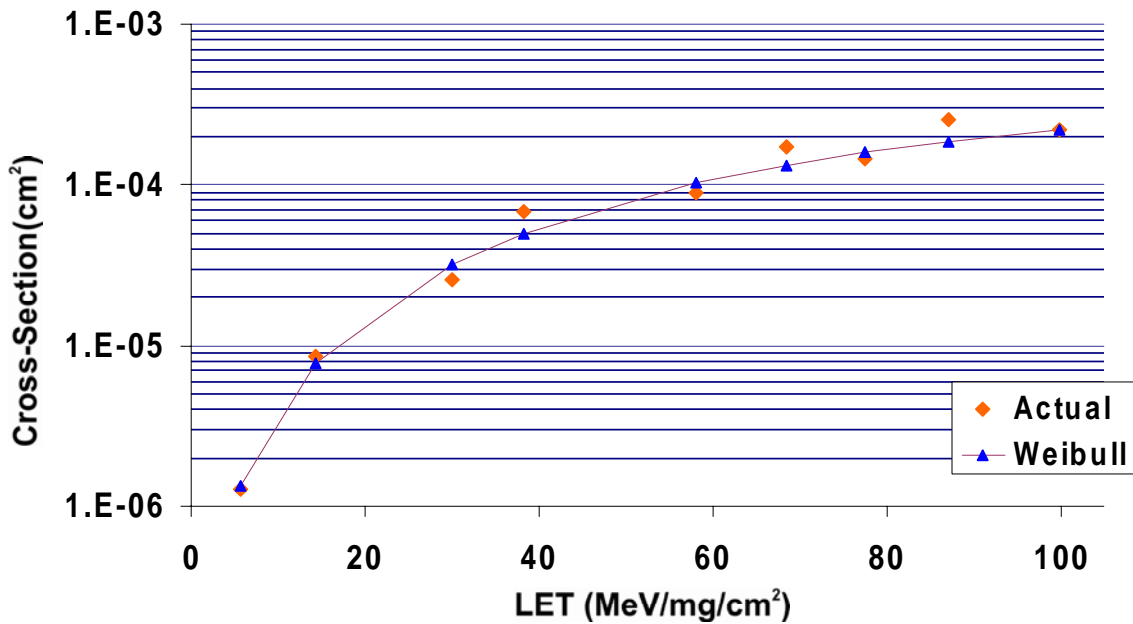


Fig. 28: ADC data output ASET cross section vs. LET per channel. The cross section is an average of both channels for all 3 units tested. For the Weibull plot parameters,  $A=0.00035$  and  $s=1.95$ .

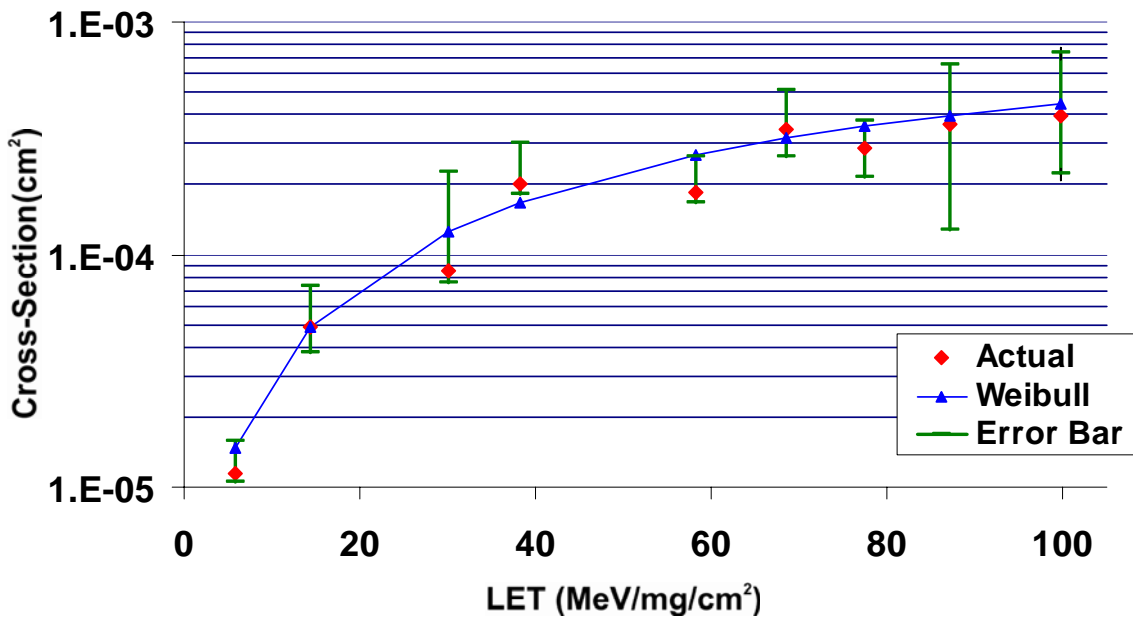


Fig. 29: Total ADC data output SEU cross section vs. LET per channel. ASET and DSET were combined and averaged from the 3 boards and two outputs. The green error bars are the minimum and maximum range seen on the 3 units and 2 channels per unit. For the Weibull plot parameters,  $A=0.0007$  and  $s=1.35$ .

## B2. Monthly Events and Outage Time

The average events per channel per month were calculated for both ASETs and DSETs using the FOM as discussed in section V-A. The values were calculated based on the data from the Weibull curve. The average ASET **events/channel/month** was  $8 \times 10^{-4}$ . The average DSET events/channel/month was  $2 \times 10^{-3}$ . The total events/channel/month for the ASET and DSET combined was  $4 \times 10^{-3}$ .

The reliability of a semiconductor device performance is indicated in terms of its “**outage time**”, i.e. a lower outage time typically indicates a robust and reliable device. The longest event duration times were averaged over all the ion strikes and multiplied by the FOM to calculate the *Total Monthly Accumulated Event Time* (outage time). The average of the longest event duration time was 1627ns. Therefore, the calculated outage time was **6 ns/month**.

## C. Output Clock

### C1. Cross Section vs. LET

Fig. 30 shows average output clock SEU cross section vs. LET and Weibull plots. The cross sections are averaged from the 3 units tested.

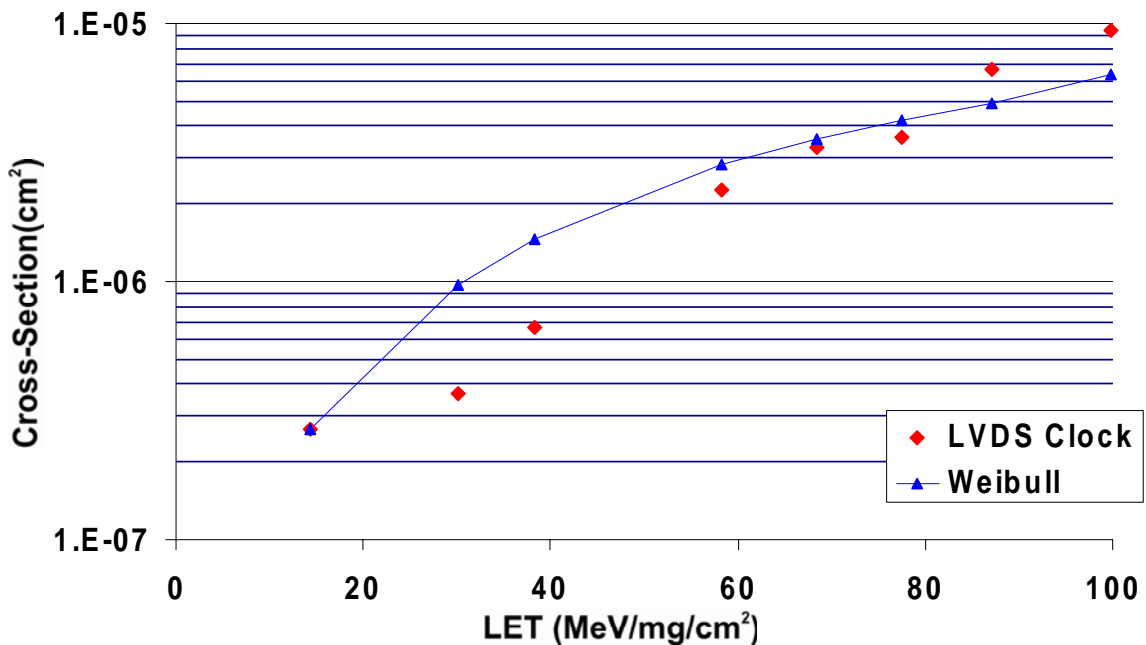


Fig. 30: Output clock SEU cross section vs. LET averaged from the 3 units tested. For the Weibull plot parameters,  $A=0.00001$  and  $s=1.8$ .

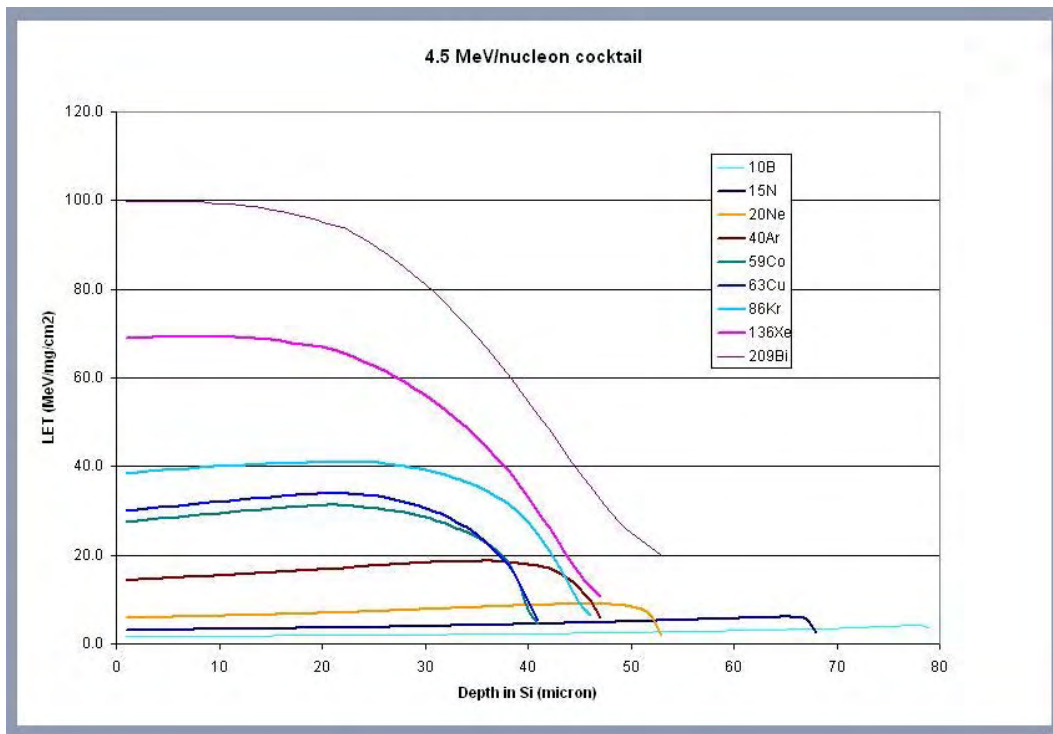
## **B. LVDS Clock Test**

The figure of merit (average events per month) for the clock output was  $4 \times 10^{-5}$ . In order to calculate the *total monthly accumulated event time*, the average of the longest upset for each ion strike, **51ns** was used. The *monthly outage time* was **2 ps**.

## Appendix A

### Heavy-Ion Cocktail Bragg Curves

Fig. A1 is a Bragg curve plot from the Lawrence Berkeley National Laboratory [7] that shows the depth of penetration and energy for each ion used in the experiment. The ADC08D1000WGFQV had a thickness of 11  $\mu\text{m}$  from the top of the passivation to the bottom of the epi layer. From Fig. A1, one can see that at 11  $\mu\text{m}$ , none of the ions start to lose energy and some have a slight increase in energy. Thus, the LET value of the ion is almost constant as it passes through the sensitive charge collection region of the transistor. As a result, the need to correct LET magnitudes used in the report (for penetration depth) was eliminated.



**Fig. A1. LET vs. penetration profile for various ion species used in the heavy-ion experiments**

## Appendix B

### 4.5 MeV/nucleon cocktail (HeH<sup>+1</sup> to Bi)

This cocktail, based on a tune-up of the ion source and Cyclotron using <sup>40</sup>Ar<sup>+8</sup>, has an A/q ratio of 5 and energy of 4.5 MeV/nucleon. To achieve lower LET, boron can be added by special request. For even lower LET, HeH<sup>+1</sup> ions can be accelerated; this requires a special tune-up. For an LET of about 100 MeV/mg/cm<sup>2</sup>, <sup>209</sup>Bi<sup>+41</sup> can be run at this energy, but requires advance notice and the AECR-U ion source. All of the above information was obtained from LBNL.

Table B1. Heavy-ion cocktail used in the SEE experiments.

Cocktail	Ion	Ion Energy	Mass	Charge State	LET	Range in Si
~MeV/u		MeV	amu		(MeV/(mg/cm <sup>2</sup> ))	microns
4.5	B*	45	10	+2	1.64	79
4.5	N	67	15	+3	3.08	67
4.5	Ne	90	20	+4	5.73	53
4.5	Ar	180	40	+8	14.33	48
4.5	Cu	293	65	+13	29.91	44
4.5	Kr*	325	78	+15	39.54	41
4.5	Kr	378	86	+17	39.25	47
4.5	Ag	464	107	+21	58.19	46
4.5	Xe	603	136	+27	68.46	48
4.5	Tb	724	159	+32	77.50	52
4.5	Ta	805	181	+36	87.20	53
4.5	Bi*	940	209	+41	99.70	54

\* = by special request

## References

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<http://www.national.com/ds/DC/ADC08D1520QML.pdf>
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<http://www.jedec.org/download/search/jesd57.pdf>
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