Single Event Upset Characterization of GHz Analog to Digital Converters with Dynamic Inputs Using a Beat Frequency Test Method

Kirby Kruckmeyer, *Member, IEEE*, Robert L. Rennie, *Member, IEEE,* Dawn H. Ostenberg,
Vishwanath Ramachandran, and Tareq Hossain

Abstract—**Typically, single event upset (SEU) testing of analog to digital converters (ADC) has been done with static inputs. A test method, using a beat frequency and code error detection software, is presented. This test method allows for SEU characterization of ultra high speed ADC's, using dynamic inputs that more closely reflect the operating conditions in a space application. The test method is demonstrated on National Semiconductor's ADC08D1000WG-QV at 1 gigasample per second (GSPS) and an input frequency close to 1 GHz. A discussion of the SEU signatures and error rates are also presented.**

I. Introduction

TESTING the single event upset (SEU) performance of an ultra high speed analog to digital converter (ADC) under typical operating conditions presents a challenge. Newer communications applications will involve data rates of one gigasample per second (GSPS) or higher, with high frequency inputs that can be into the second or third Nyquist zones. At these high data rates, just monitoring and capturing the output data can be complex. Others have presented novel and elegant solutions for monitoring ADC outputs, but these usually involve testing with a static input [1]-[3]. It may be more appropriate to characterize the SEU performance with dynamic inputs as they are used in the applications. Dynamic signals put more stress on the input structures and there is the possibility that the large front end analog blocks could create long internal transients.

A test method was developed using a beat frequency and code error detection software so that an ADC could be tested with the input frequency close to 2 times Nyquist. With the input frequency set very close to the clock frequency, the output code of the ADC is a slow moving sine wave, changing at a rate of less than 1 LSB per clock cycle. Code error rate software is used to detect when the output shifts from the expected value.

This test method was demonstrated on National Semiconductor's ADC08D1000WG-QV, a dual channel, 8 bit, low power ADC [4]. The testing was done with a 1GHz clock and 998.76MHz input, resulting in a 1.24 MHz output.

II. Device Description

National Semiconductor's ADC08D1000WG-QV is a dual channel 8 bit ADC that can run up to data rates of 1.2 gigasamples per second (GSPS) and supports input bandwidths to 1.7 GHz. It is built on a folding architecture for low power consumption (800mW per channel) and uses a calibration circuit for improved performance with an effective number of bits (ENOB) of 7.2 at Nyquist [5]. It is immune to single event latch ups at 120 MeV/mg/cm^2.

The two independently operating 8 bit ADC's, called I and Q, convert the inputs synchronously using a single input clock. Each of these converters has a 1:2 demultiplexer that feeds two LVDS output buses, called DI and DId and DQ and DQd for I and Q channels respectively. The DId and DQd outputs are delayed by one clock cycle with respect to DI and DQ outputs. Thus, the digital outputs from the two ADCs on the chip are available on 4 separate differential LVDS 8-bit buses. Current and previous samples for each channel are clocked out at one half the sampling rate under normal operating conditions (Fig. 1 and 4).

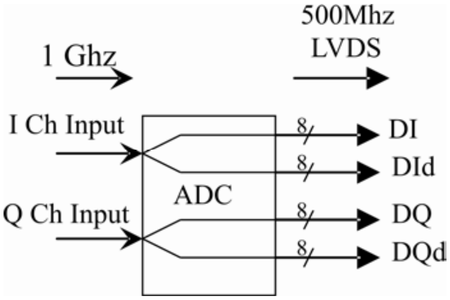

Fig. 1 ADC08D1000WG-QV inputs and outputs. Each channel has a 1:2 demultiplexer that feeds two LVDS output buses.

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Kirby Kruckmeyer is with National Semiconductor, Santa Clara, CA 95052 (telephone: 408-721-3548, email: kirby.krcuckmeyer@nsc.com).

Robert L. Rennie is with National Semiconductor, Santa Clara, CA 95052 (telephone: 408-721-5119, email: rob.rennie@nsc.com).

Dawn H. Ostenberg is with National Semiconductor, Santa Clara, CA 95052 (telephone: 408-721-7064, email: dawn.ostenberg.nsc.com)

Vishwanath Ramachandran and Tareq Hossain are with Vanderbilt University, Nashville, TN 37235 (email: vishwa.ramachandran@vanderbilt.edu and tareq.hossain@vanderbilt.edu).

III. TEST METHOD

A. Test Setup

ADC08D1000WG-QV die, assembled in plastic packages for this study, were decapped and soldered to ADC08D1000DEV boards [6]. Three separate units and boards were used for the testing.

The ADC08D1000DEV board uses a single power supply that powers the entire board, including the ADC. On the board, the ADC connects to a Xilinx Virtex4 FPGA for storing and processing the ADC output data.

The ADC08D1000DEV board was connected to a laptop computer through a USB interface and was driven with WaveVision4 software. This setup enabled data output acquisition, Fast Fourier Transform analysis (FFT) and calculation of critical parameters [6].

For this study, the clock input, and the I and Q channels were supplied by separate signal generators (Fig. 2). Due to the configuration of the test facility, the signal generators were connected to the test board by 30 feet of SMA cables.

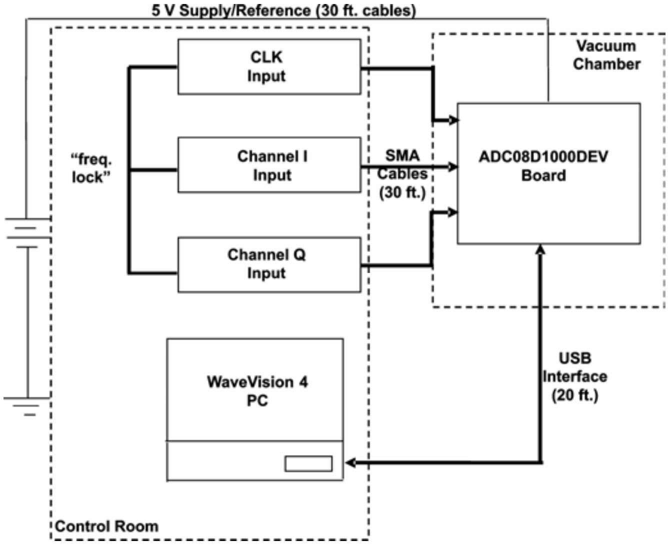


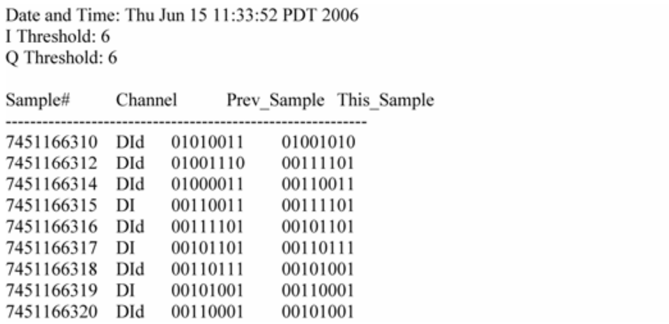
Fig. 2 SEU test setup, using ADC08D1000DEV board.

B. Code Error Detection Software

For the SEU testing, the Virtex4 was programmed with code error detection software. For each channel (I or Q), the output was compared to the previous output. For instance, on the I channel, the DI output was compared to the previous DId output. If the output codes differed by more than a preset LSB value, an error would be registered. The clock cycle, DI output code and previous DId code output would be recorded for the error (Fig. 3). For an event that lasted for one clock cycle, two errors were recorded, one for the actual error, and one for when the output returned back to the expected value. For events that lasted longer than one clock cycle, errors were continuously recorded until the output returned to the expected value.

It was chosen to monitor the complete code rather than the individual bits. Although the outputs of the ADC are digital, the SEU errors are most likely not bit flips as seen on digital products, but code errors generated from the analog portion of the device.

The threshold for an error to be registered was set at ±6 LSB. Earlier tests showed a background noise of ±4 LSB for this setup. The performance of the setup was degraded due to the units being decapped and the long cables from the signal generators and pass-throughs to the vacuum chamber required by the configuration of the test facility.



```
Date and Time: Thu Jun 15 11:33:52 PDT 2006
I Threshold: 6
Q Threshold: 6

Sample#      Channel      Prev_Sample  This_Sample
--------------------------------------------------------
7451166310  DId    01010011     01001010
7451166312  DId    01001110     00111101
7451166314  DId    01000011     00110011
7451166315  DI     00110011     00111101
7451166316  DId    00111101     00101101
7451166317  DI     00101101     00110111
7451166318  DId    00110111     00101001
7451166319  DI     00101001     00110001
7451166320  DId    00110001     00101001
```

Fig. 3 Partial code error report for unit 2 for a Bi ion run.

C. Beat Frequency

The beat frequency (and resultant output of the ADC) is the difference between the clock and input frequencies (Fig.4). This allows the input of the ADC to be run at high frequencies, while the outputs are at a much lower frequency. This is necessary to keep the expected output change to less than 1 LSB per clock cycle, so that the code error detection program does not record normal expected output changes, which would mask changes due to SEU's (Fig. 5).

For this study, the maximum nominal conversion rate of 1 GSPS was chosen and the clock was set at 1 GHz. The input frequency (f_{in}) required to get 1 LSB change per clock cycle can be calculated by the following equation:

$$f_{in} = \frac{f_s}{2^N \pi} \tag{1}$$

where f_s is the sampling frequency and N is the resolution of the ADC in bits [7]. In this case with the sampling frequency set at 1 GHz, the input frequency was set at 998.76 MHz, for a beat frequency and output of 1.24 MHz.

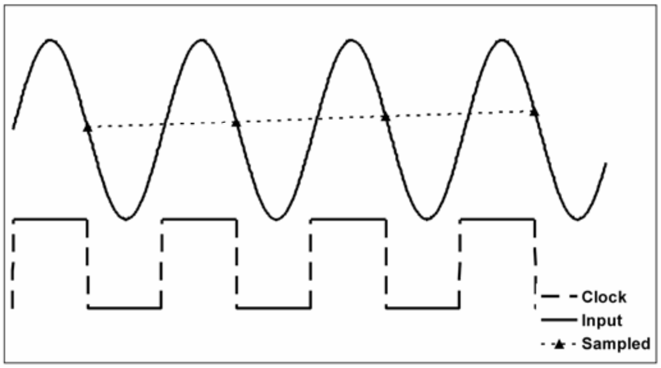


Fig. 4 Beat frequency. With the clock frequency set at 1 GHz, and the input frequency, slightly lower at 998.76 MHz, the sampled points on the input curve will result in an output of 1.24 MHz.

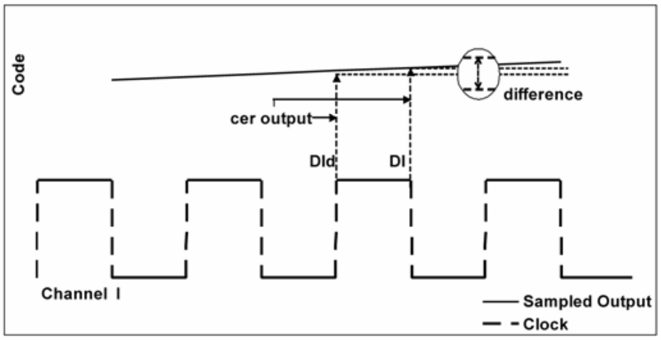


Fig 5. ADC output with the beat frequency. The output clock of the ADC08D1000WG-QV, with the 2:1 demultiplexed LVDS output buses, runs at half of the speed of the input clock. The outputs alternate between the DI and DId buses. With a 1 GHz input clock and a 1.24MHz output, the maximum rate change between the output buses at the steepest part of the curve will be 1 LSB.

D. *Test Procedure*

Testing was done using the 88" cyclotron at the Berkeley Accelerated Space Effect facility at the Lawrence Berkeley National Laboratory. The 4.5MeV/nucleon beam was used. Ions used, linear energy transfers (LET) and penetration range into silicon are shown in Table I.

At the beginning of the testing of each board, and after each ion run, an FFT was run and the critical parameters were analyzed as a cursory check to ensure that the part did not experience any hard errors that would have damaged the part or require it to be reset. A more in depth single event latch up study had been completed earlier, using a different setup. That testing showed the part to be immune to single event latch up, up to the 120 MeV/mg/cm^2 tested [8].

The code error detection program was started just prior to the start of an ion run. The ion beam was shut off when the fluence reached 1x10^7 ions/cm^2 or after one hundred errors were recorded on one channel, whichever came first, in accordance with test method JESD57 [9]. The code error detection program would then be stopped and the error data for the ion run would be uploaded to the computer.

IV. TEST RESULTS

No evidence of hard errors, requiring the units to be reset, were observed during this testing.

The code error detection software detected errors at all ions tested, starting at nitrogen with an LET of 3.08 MeV/mg/cm^2. Nitrogen was run to a fluence of 1x10^7 ions/cm^2. For all other ions, 100 errors were registered before the 1x10^7 ions/cm^2 fluence was reached (Table I). It was never possible to stop the beam exactly on 100 errors. In the case of the heavier ions, the errors occurred so quickly that several hundred to a thousand errors were recorded before the beam could be stopped.

The magnitude of the errors ranged from 7 to 145 LSB. Very few errors had a magnitude that exactly matched a bit size (8, 16, 32, 64 or 128). The magnitude of the errors was independent of LET. Fig. 6 shows the magnitude of the errors for one unit for an argon ion run.

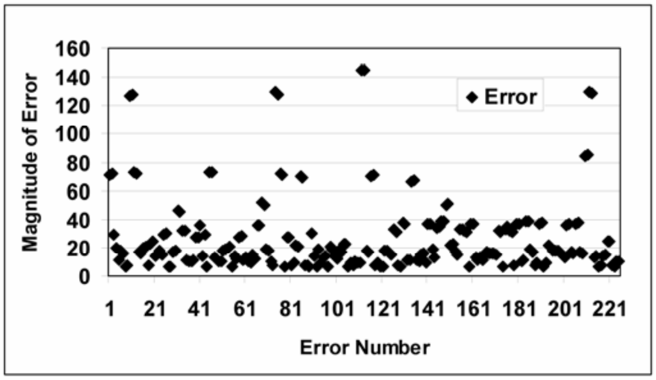


Fig 6. Magnitude of the errors for the I channel of unit N2 during an Ar ion run.

V. DATA ANALYSIS

A. *Event duration*

Two types of events were differentiated based on the error data. The first type was isolated events that lasted one clock cycle (1 ns). These were indicated by an error recording when the event occurred and another error on the next clock cycle when the output returned to the expected value. These were defined as Digital Single Event Transients (DSET).

The second type of event was defined as an Analog Single Event Transient (ASET). These were identified by a long string of errors that lasted several to hundreds of consecutive clock cycles. Because a single event can consist of many errors, the decision to stop on 100 errors for an ion run turned out to be inappropriate to gather enough data for a statistically significant cross section on a mixed-signal part, such as an ADC.

In some cases, a long string of errors would be closely followed by another long string. It is believed that these strings all comprised the same event, and that there were gaps in registering the errors. The time gap between the errors was very short compared to the flux of the ion beam, making it very unlikely that these would be two separate events caused by two separate ion strikes. The gaps in error strings would typically be under 100 ns, while the average time between ion strikes was 5 ms at the maximum flux of 2x10^5 ions/cm^2/s used in this testing (Fig. 7).

The gaps in the event are due to the limitations of the code error detection software. Only a difference between the demultiplexed outputs is detected. If both outputs have the same magnitude of error, the error will only be registered at the beginning and when the output returns to the expected value. In many cases, it is believed that both outputs became stuck at the same value for a period of time during the event. One way around this limitation would be to record the output at several clock cycles before and after every error recording.

B. *ASET signature*

Whenever there was an ASET on the I channel, the Q channel would also exhibit an ASET at roughly the same time and duration. (A similar correlation between the channels was not detected for the DSET's.) The Q channel ASET would be delayed from the I channel ASET by approximately

TABLE I
LIST OF IONS USED, RAW ERROR COUNT AND NUMBER OF UPSET EVENTS FOR UNIT 2

Ion	Energy(MeV)	LET (MeV/mg/cm^2)	Range in Si (µm)	Fluence (ions/ cm^2)	I errors	Q errors	I events	Q events
^{15}N^{+3}	67	3.09	67	1.01E+7	51	48	25	27
^{20}Ne^{+4}	90	5.77	53	9.72E+6	113	120	57	63
^{40}Ar^{+8}	180	14.3	48	1.40E+6	108	117	51	59
^{65}Cu^{+13}	293	29.89	44	2.15E+5	359	143	27	28
^{86}Kr^{+17}	378	39.24	47	1.34E+5	252	242	18	15
^{136}Xe^{+27}	603	68.83	48	3.34E+4	721	679	4	7
^{209}Bi^{+41}	940	99.64	54	5.03E+3	528	476	2	3

4000 ns. The delay is believed to be an artifact of how the Virtex4 stores and logs the data.

During an ASET, neither of the demultiplexed outputs would match the expected value. Fig. 7 shows the DI and DId outputs for the I channel, along with a curve showing the expected output. In many cases, the error of the two outputs would be in opposite directions.

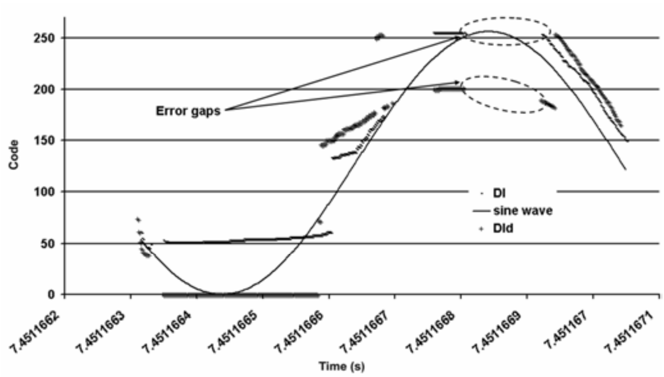


Fig. 7 Output codes for the 2:1 demultiplexed outputs of the I channel during an ASET for unit N2 during a Bi ion run. The expected output sine wave is superimposed over the output codes. The phase was estimated based on the signature of the errors. There are two gaps during the ASET where no errors were recorded. The dashed ovals indicate the longest gap.

A few of the observed ASET's lasted more than 1 µs, comprising more than one output cycle. In these cases, the error signature from the first cycle would partially be repeated during the second cycle (Fig. 8).

The duration of an ASET was dependent on LET at low LET values (Fig. 9). Above an LET of 68 MeV/mg/cm^2, there appeared to be less of a dependence.

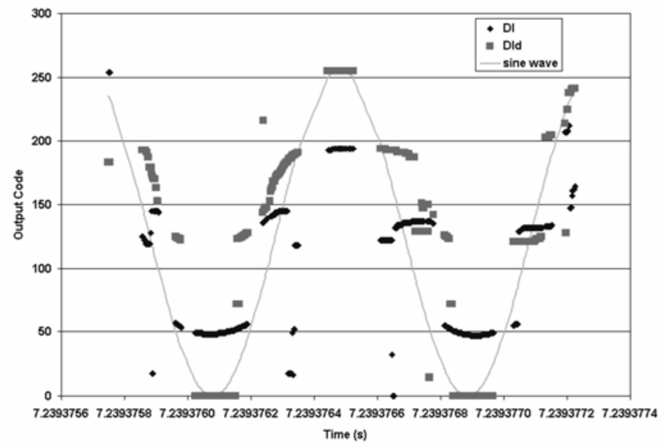


Fig. 8 Output codes for the 2:1 demultiplexed outputs of the I channel during ASET for unit 1 during a Bi ion run. The expected output sine wave is superimposed over the output codes. The phase was estimated based on the signature of the errors. The error signature during the first cycle of the event is partially repeated during the second cycle.

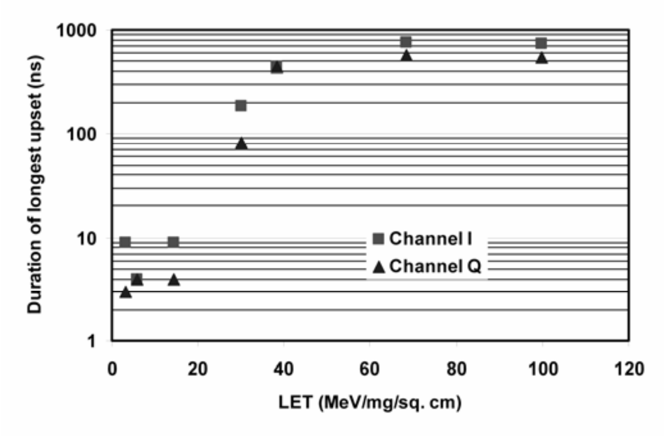


Fig. 9 Longest duration event vs. LET for unit 2.

These ASET signatures provide clues to what areas of the device are being impacted by the ion strikes. For instance, because the magnitude of the errors do not match a bit size (8, 16, 32, 64 or 128), it is unlikely that the digital output structures are being impacted. Since both channels show errors at the same time, it is likely that the common front end analog cells were involved. An in-depth study using these data to isolate the sensitive cells is beyond the scope of this paper, but will be covered at a later date.

C. *Cross section vs. LET curve*

The errors were grouped into events for each of the units (Table I). The data for the three units was combined, a cross section per channel vs. LET plot was generated and a Weibull curve was fitted to the data (Table II and Fig. 10).

TABLE II
WEIBULL PARAMETERS

W (MeV/mg/cm^2)	L_{TH} (MeV/mg/cm^2)	s	Limiting X-section (cm^2)
100	3	1.6	$5.05\text{x}10^{-4}$

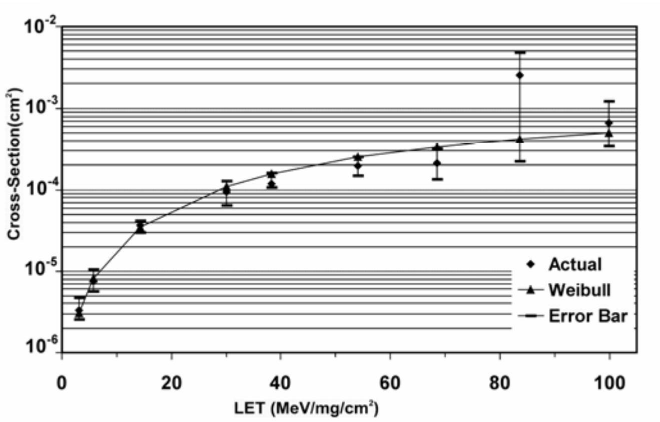


Fig. 10 Cross section vs. LET curve of single event upsets per channel for the ADC08D1000WG-QV. Data is for the 3 units tested.

VI. CONCLUSIONS

A test setup using code error detection and a properly chosen beat frequency makes it possible to characterize the SEU performance of an ADC using dynamic inputs close to the sample rate. This can be preferable to testing the part with static inputs. Not only do the dynamic inputs used in this study more closely match space application conditions, the resulting error signatures can provide clues to what part of the circuit is susceptible to an ion strike.

A code error detection program that logs errors instead of the whole data output stream makes handling and analyzing the data manageable. On a mixed-signal product, such as an ADC, it can be more appropriate to monitor the entire code instead of the individual bit errors. Collection of just 100 errors for each ion run may not be sufficient for a mixed-signal product. It may require analyzing the data in real time at the test site to determine how errors comprise an event and adjusting the length of the ion runs accordingly.

This method could be enhanced by recording the data for several clock cycles before and after an error is registered. This would overcome the limitation of only one error being recorded when both outputs exhibit the same magnitude of error, give greater visibility into the output status during any gaps in the error recordings in a long event and facilitate the analysis of the DSET signatures.

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