

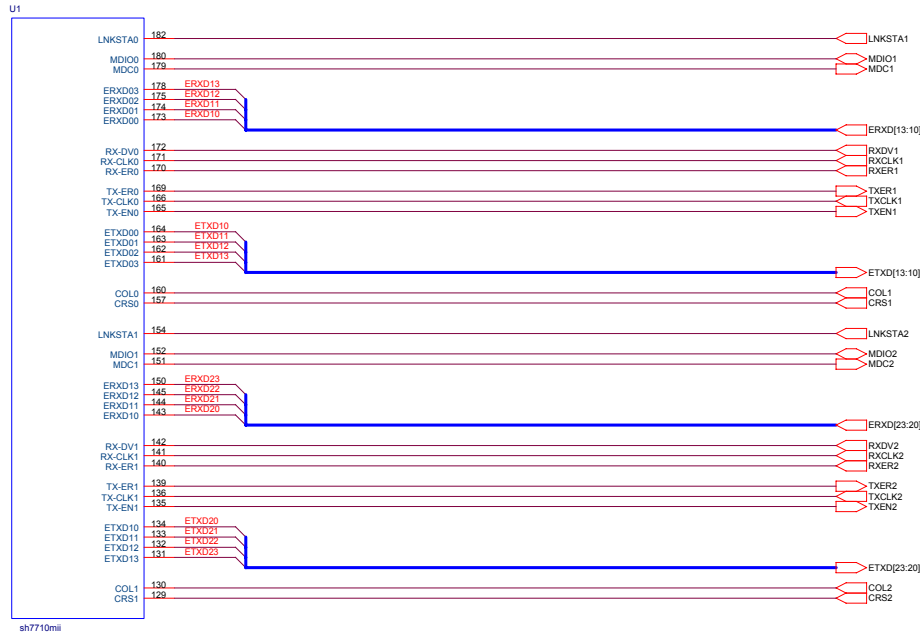
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Note: For Reference Only

RENESAS

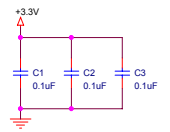
# SH7710 RISC Microprocessor

NOTE: For dual MII devices.

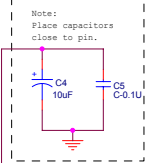


MII Connections

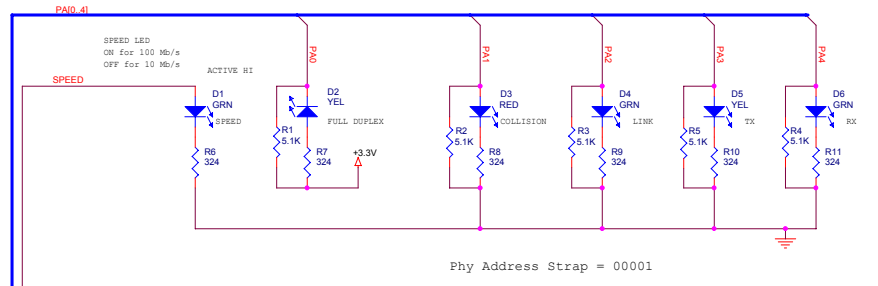
Note: For Reference Only  
**MI I ETHERNET PHY 1**



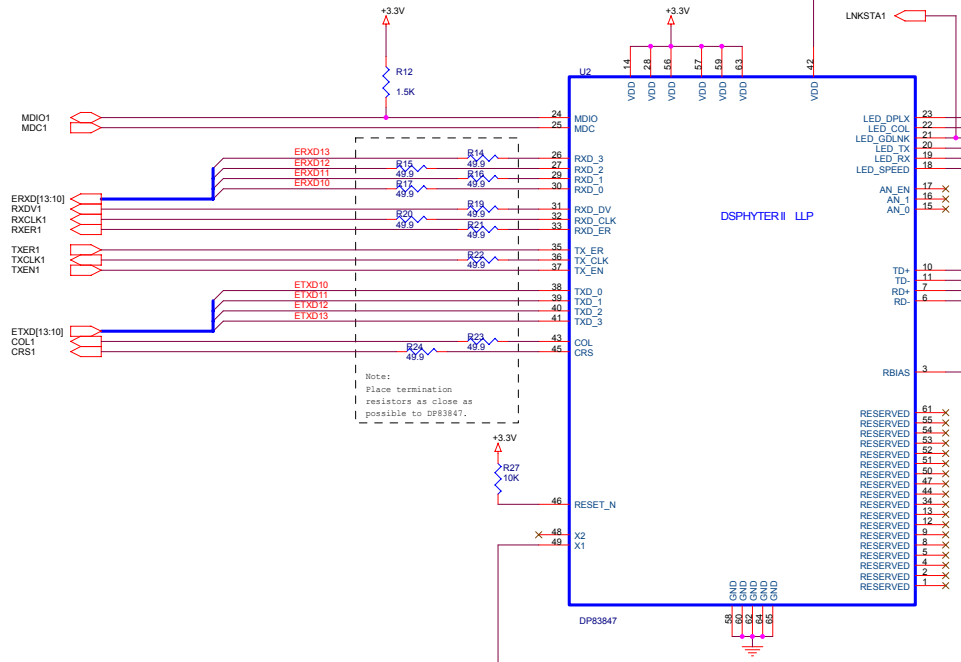
NOTE: place 0.1uF capacitors close to each power pin (14, 28, 56) on U2. See layout of reference design board for proper connections to VDD bars (57, 59, 63).



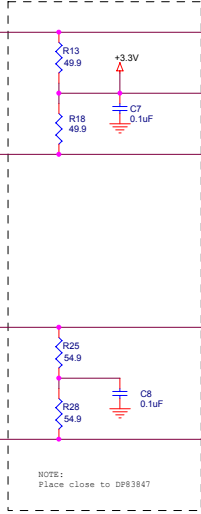
Note: Place capacitors close to pin.



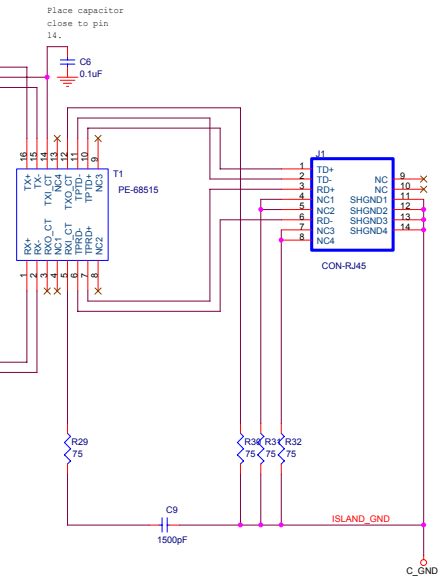
Phy Address Strap = 00001



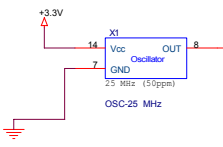
Note: Place termination resistors as close as possible to DP83847.



NOTE: Place close to DP83847

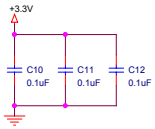


NOTE: All GND are system ground plane  
 C\_GND is chassis ground plane

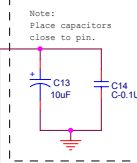


OSC=25 MHz

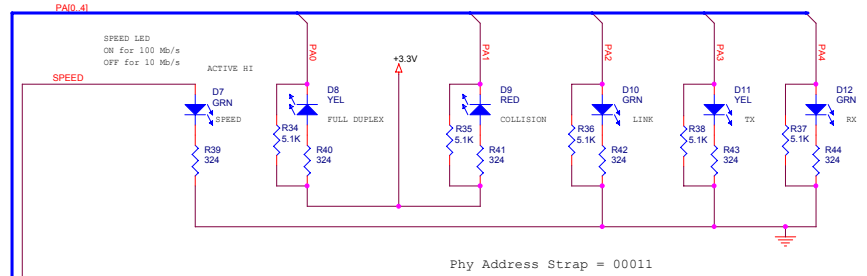
Title		Renesas SH7710/NSC DP83847 App. Note	
Size	Document Number	Rev	
C	CID Working Draft: MI I Ethernet PHY 1	A	
Date:	Friday, July 09, 2004	Sheet	2 of 3



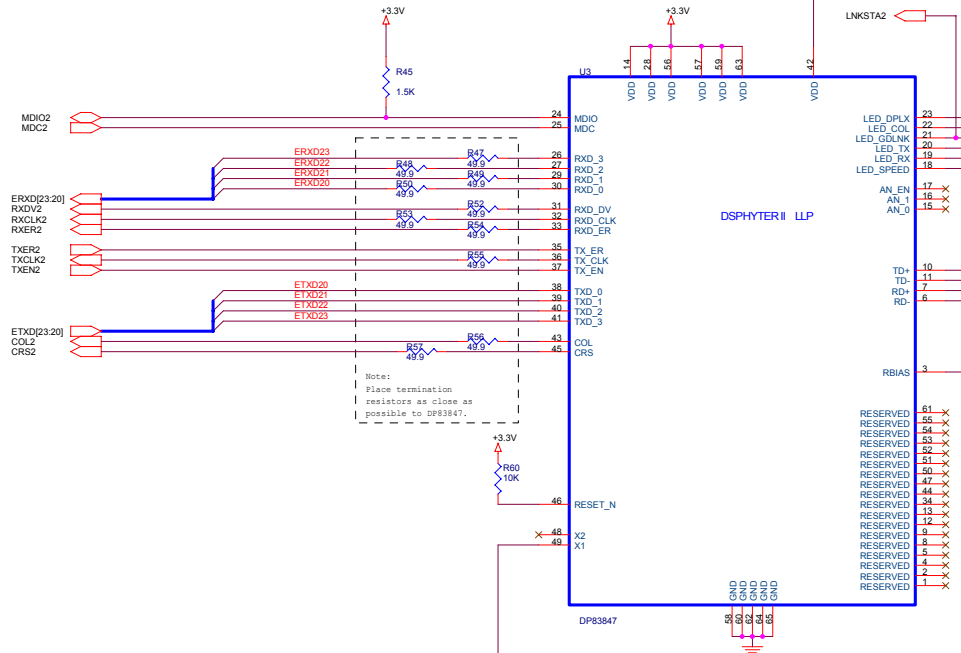
NOTE: place 0.1uF capacitors close to each power pin (14, 28, 56) on U2. See layout of reference design board for proper connections to VDD bars (57, 59, 63).



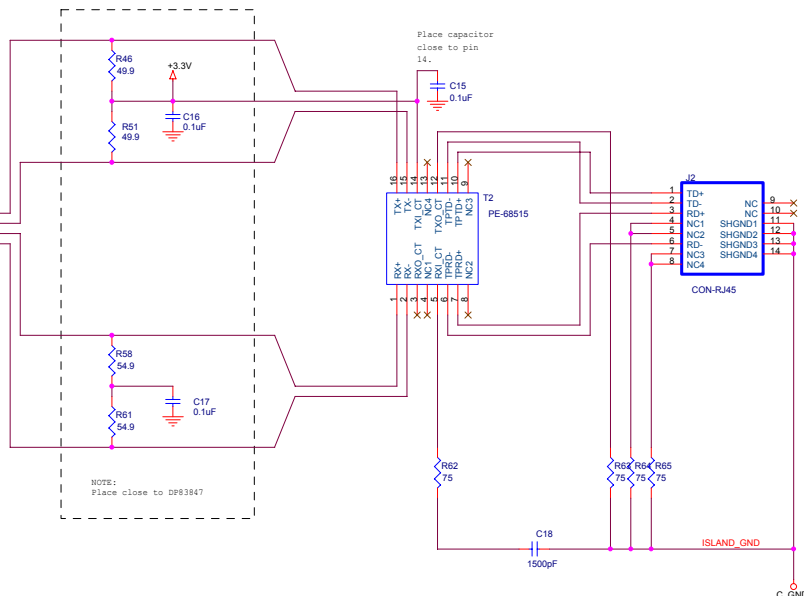
Note: Place capacitors close to pin.



Phy Address Strap = 00011

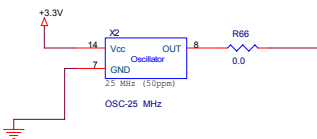


Note: Place termination resistors as close as possible to DP83847.



NOTE: Place close to DP83847

NOTE: All GND are system ground plane  
 C\_GND is chassis ground plane



Title		Renesas SH7710/NSC DP83847 App. Note	
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