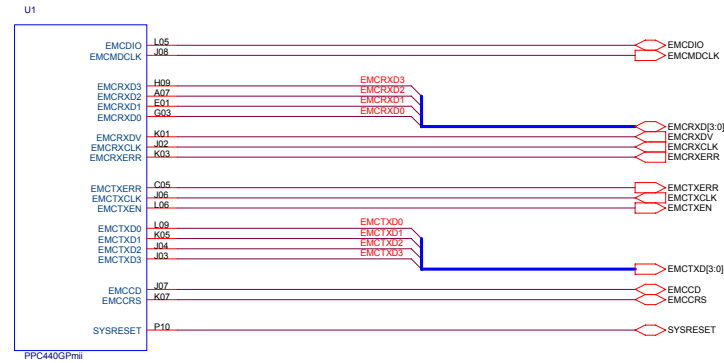


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Note: For Reference Only

IBM Power PC 440GP Embedded Processor

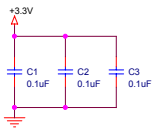
NOTE: For use with a single MII device.



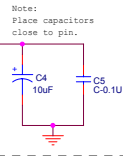
MII Connections

Title		IBM PPC440GP/NSC DP83847 App. Note	
Size	Document Number	Rev	
C	CID Working Draft: CPU MII Connections	A	
Date:	Thursday, October 28, 2004	Sheet	1 of 2

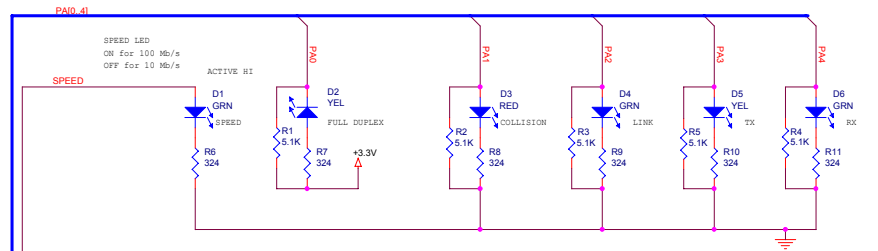
MII ETHERNET PHY



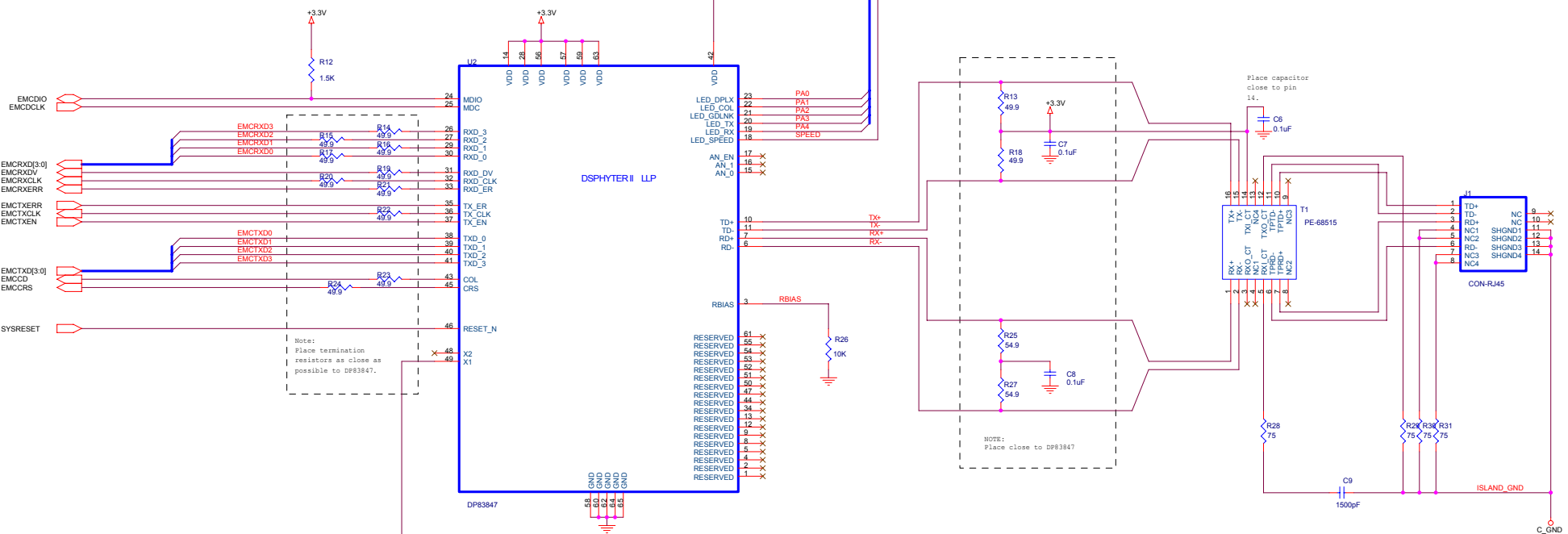
NOTE: place 0.1uF capacitors close to each power pin (14, 28, 56) on U2. See layout of reference design board for proper connections to VDD bars (57, 59, 63).



Notes:
Place capacitors close to pin.



Phy Address Strap = 1



Note:
Place termination resistors as close as possible to DP83847.

NOTE:
Place close to DP83847

Place capacitor close to pin 14.

NOTE:
All GND are system ground plane
C_GND is chassis ground plane

Title		
IBM PPC440G/NSC DP83847 App. Note		
Size	Document Number	Rev
C	CID Working Draft: MII Ethernet	A
Date	Friday, July 09, 2004	Sheet 2 of 2