

# LX16EVK01

## Channel Link III Ser/Des

### Evaluation Kit

Rev 1.0  
Oct, 2010

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## General Description

The LX16EVK01 is designed to allow for easy evaluation of the DS92LX1621 and DS92LX1622 Channel Link III Ser/Des. This kit allows for 2 basic methods of evaluation:

- 1) Users may apply parallel clock, data and I2C commands, and evaluate the power, jitter and cable performance of the Ser/Des. Or,
- 2) Apply only a parallel clock and enable BIST mode. This allows the user to easily evaluate the serial link and check device feature functionality such as receive equalization, SSCG, etc.

The LX16EVK01 boards uses USB connectors as the serial Channel Link III inputs/outputs. SMA connectors can also be attached and configured for serial input/output if other types of the cable are desired.

## Features

- 20 – 50 MHz support for up to 800 Mbps (default configuration)
- LVCMOS parallel interface: 16-bit data (default) + clock + 2 upstream GPIO
- High speed forward channel + bi-directional control channel + back channel GPIO serialized to 1 pair
- AC Coupled STP Interconnect up to 10 meters in length
- Selectable receive equalization, SSCG, and deserializer output slew rate
- Integrated serial terminations
- @ Speed link BIST Mode and reporting pin
- I2C compatible Serial Control Bus
- Power down mode minimizes power dissipation
- Randomized, DC-balanced and Scrambled data stream with CRC
- >8 kV HBM

## Applications

- Industrial Displays
- Machine Vision
- Medical Imaging

## Ordering Information

**PART:** LX16EVK01

**Demo boards:**

**Tx:** DS92LX1621-EVK

**Rx:** DS92LX1622-EVK

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## Quick Start Guide:

### DS92LX1621 Tx Board:

1. Connect 3.3V DC power and ground of the board to JP1 from the power supply (3.3V on left pin, ground on right pin). Connect 1.8V DC power and ground of the board to the J3 and J4 from the power supply respectively.
2. Attach the USB cable to the TX board (DS92LX1621) output and to an RX board (DS92LX1622) input.
3. Attach parallel data and clock to the TX board at connector J1. This is typically done with a flat ribbon cable (not supplied).

### DS92LX1622 Rx Board

4. Connect 3.3V DC power and ground of the board to JP1 from the power supply (3.3V on left pin, ground on right pin). Connect 1.8V DC power and ground of the board to the J4 and J5 from the power supply respectively.
5. Attach the USB cable to the RX board (DS92LX1622) input from a TX board (DS92LX1621) output.
6. Attach parallel data and clock output to the RX board at connector J1. This is typically done with a flat ribbon cable (not supplied).

Jumpers and switches on both the TX and RX boards have been configured at the factory; they should not require any changes for immediate operation. See the datasheet for more details.

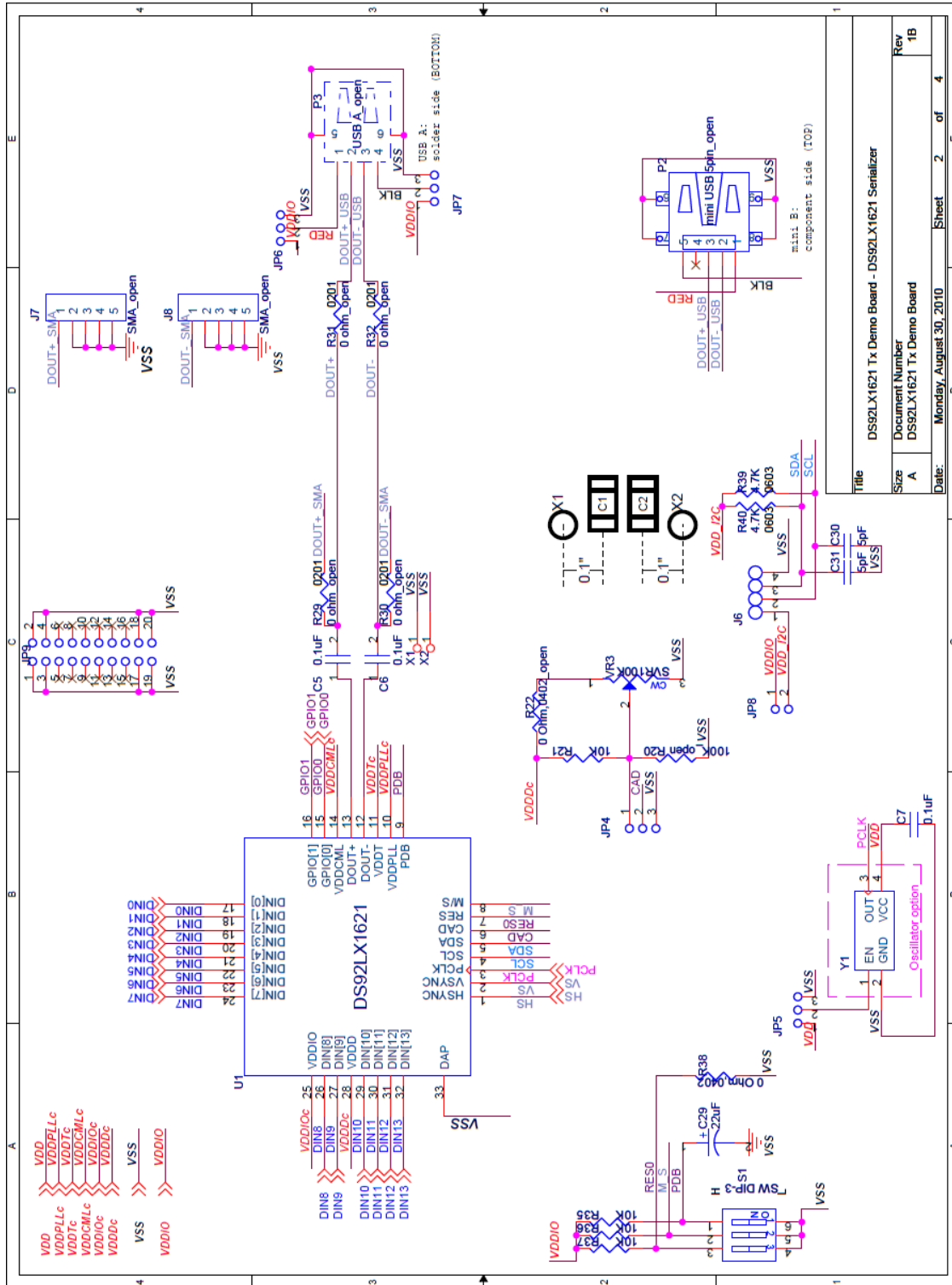
## Tx Board Configuration Settings

Component	Name	Function
<b>Power Connections</b>		
J2	5V DC	Optional 5V DC Power Jack. Note: unpopulated by default
J3	1.8V DC	1.8V VDD Power.
J4	VSS	Ground.
JP1	3.3V DC	3.3V VDD Power (left header pin), Ground (right header pin)
JP2	VDDIO	Input voltage select. Jumper set to 3.3V by default.
<b>Input and Output Connections</b>		
J1	38 position wall header	Connect to data input.
P3	USB Connector (Type-A Female)	Connect to Channel Link II output (default).
J7 and J8	SMA Connectors	Connect to Channel Link II output. Note: unpopulated by default
<b>Control Connections</b>		
S1:1	PDB	Power down mode input. PDB = H, Serializer is enabled (default) PDB = L, Serializer is in power-down mode
S1:2	M_S	I2C Mode Select. M_S = H, Slave Mode – device receives clock and data from local master M_S = L, Master Mode – device generates and drives the clock line
S1:3	RESO	Reserved. Keep set to LOW (default)
JP4 and VR3	ID[x]	Connect CAD pin to VSS to have the default device PHY address (default setting). Connect CAD pin to VR1 pin; then adjust VR4 value to select desired device PHY address. See datasheet for detailed information.
JP8 and J6	I2C Interface	Leave JP8 unconnected if I2C VDD is provided by an external source. (default).
<b>Others</b>		
JP5, JP6, JP7	Other options	Do not connect

## Tx Board Bill of Materials

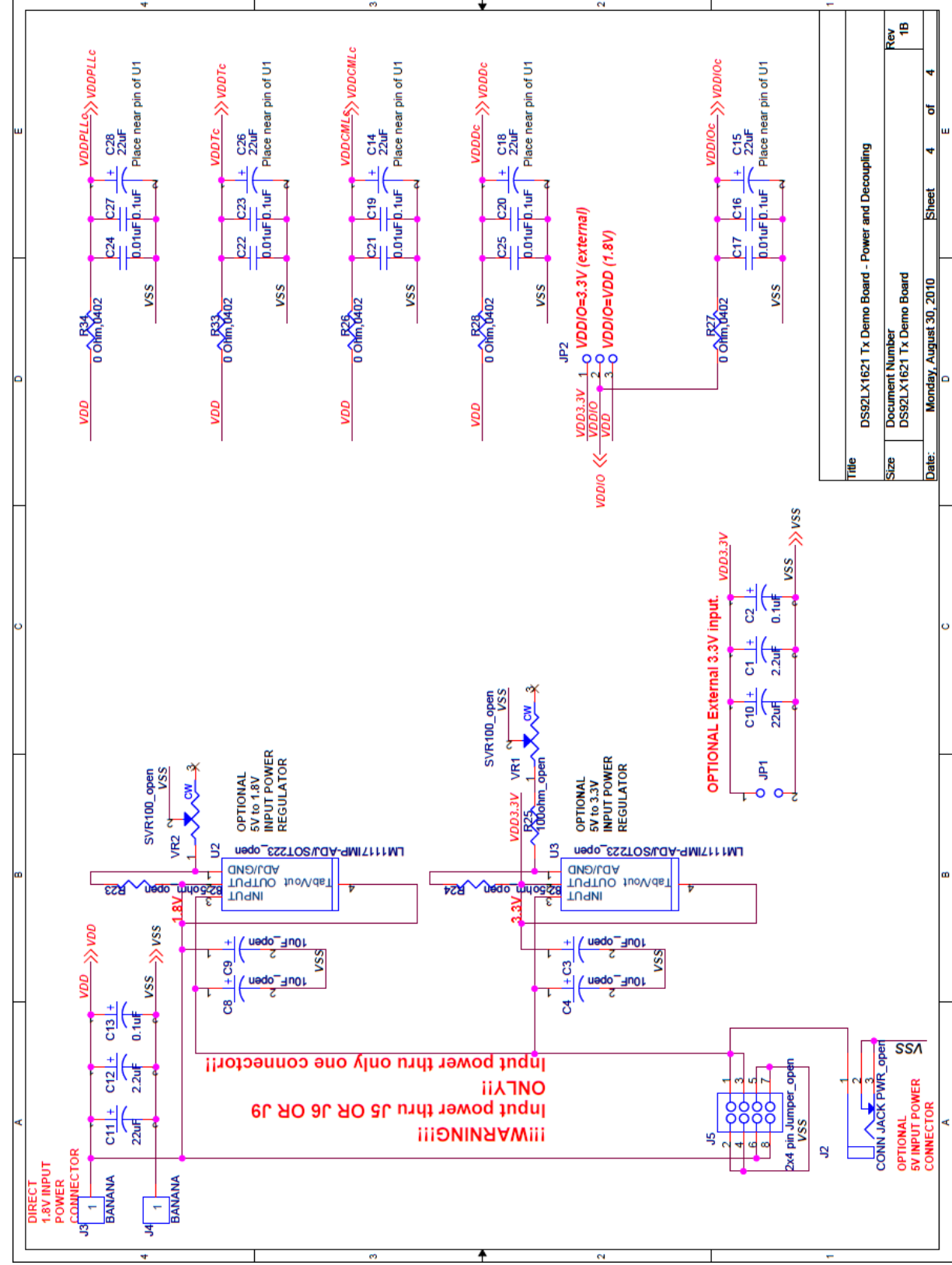
Item	Quantity	Reference	Part	Comments	MFR Part#
1	2	C1,C12	2.2uF	KEMET	399-3714-1-ND
2	2	C13,C2	0.1uF	KEMET	399-1249-1-ND
3	4	C3,C4,C8,C9	10uF_open	nichicon	493-2365-1-ND
4	2	C5,C6	0.1uF	Panasonic	PCC2398CT-ND
5	6	C7,C16,C19,C20,C23,C27	0.1uF	Panasonic	PCC2277CT-ND
6	2	C10,C11	22uF	nichicon	493-2391-1-ND
7	6	C14,C15,C18,C26,C28,C29	22uF	Kemet	399-3835-1-ND
8	5	C17,C21,C22,C24,C25	0.01uF	KEMET	399-3189-1-ND
9	2	C30,C31	100pF	TDK Corporation	445-1786-1-ND
10	3	JP1,JP3,JP8	2-Pin Header	AMP/Tyco	A26542-ND
11	5	JP2,JP4,JP5,JP6,JP7	3-Pin Header	AMP/Tyco	A26545-ND
12	1	JP9	2X10-Pin Header, open	AMP/TYCO	A26580-ND
13	1	J1	HEADER 19x2	AMP/TYCO	A26588-ND
14	1	J2	CONN JACK PWR_open	CPU Inc	CP-002A-ND_open
15	2	J3,J4	BANANA	Johnson	J147-ND
16	1	J5	2x4 pin Jumper_open	Molex	WM26808-ND
17	1	J6	IDC1X4	Molex/Waldom Electronics Corp	WM2702-ND
18	2	J8,J7	SMA_open	Johnson Components	J658-ND_open
19	1	P1	HSD_2X2_open	Rosenberger	
20	1	P2	mini USB 5pin_open	Hirose	H2959CT-ND
21	1	P3	USB A	AMP/Tyco	A31726-ND
22	18	R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R15,R16,R17,R18	49.9ohm_open	Venkel	
23	1	R19	49.9ohm_open	Panasonic	P49.9CCT-ND
24	1	R20	100K_open	Panasonic	P100KHCT-ND_open
25	4	R21,R35,R36,R37	10K	Panasonic	P10.0KHCT-ND
26	1	R22	0 Ohm,0402_open	Panasonic	P0.0JTR-ND_open
27	2	R24,R23	82.5ohm_open	Panasonic	P82.5HCT-ND
28	1	R25	100ohm_open	Panasonic	P100HCT-ND
29	5	R26,R27,R28,R33,R34	Ferrite Bead	Murata	490-5442-1-ND
30	2	R29,R30	0 ohm_open		
30a	3	R31,R32,R38	0 ohm		
31	2	R40,R39	1.0K	Panasonic	P1.0KGCT-ND
32	1	S1	SW DIP-3	Grayhill	GH7182-ND
33	1	U1	DS92LX1621	National	
34	2	U2,U3	LM1117IMP- ADJ/SOT223_open	National	LM1117IMP-ADJ/NOPB
35	2	VR1,VR2	SVR100_open	Bourns	3214W-101ETR-ND
36	1	VR3	SVR100K	Bourns	3224W-1-104ECT-ND
37	2	X2,X1	TP_0402		
38	1	Y1	OSC4/SM		535-10059-5-ND_open

# Tx Board Schematics



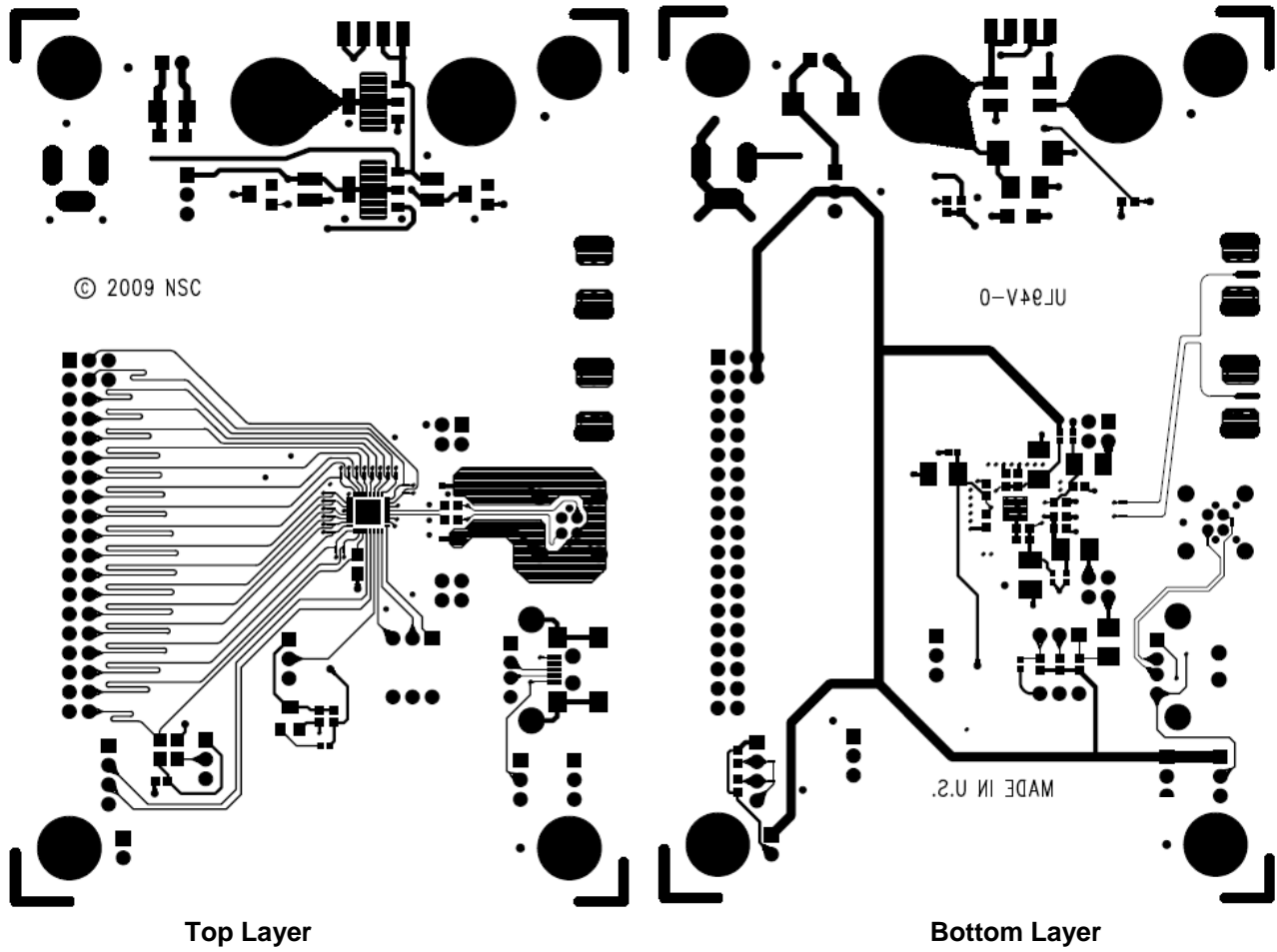
Title	DS92LX1621 Tx Demo Board - DS92LX1621 Serializer
Size	Document Number DS92LX1621 Tx Demo Board
Date:	Monday, August 30, 2010
Sheet	2 of 4
Rev	1B





Title	DSS92LX1621 Tx Demo Board - Power and Decoupling
Size	Document Number DSS92LX1621 Tx Demo Board
Date:	Monday, August 30, 2010
Sheet	4 of 4
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# Tx Board Reference Layout



## Rx Board Configuration Settings

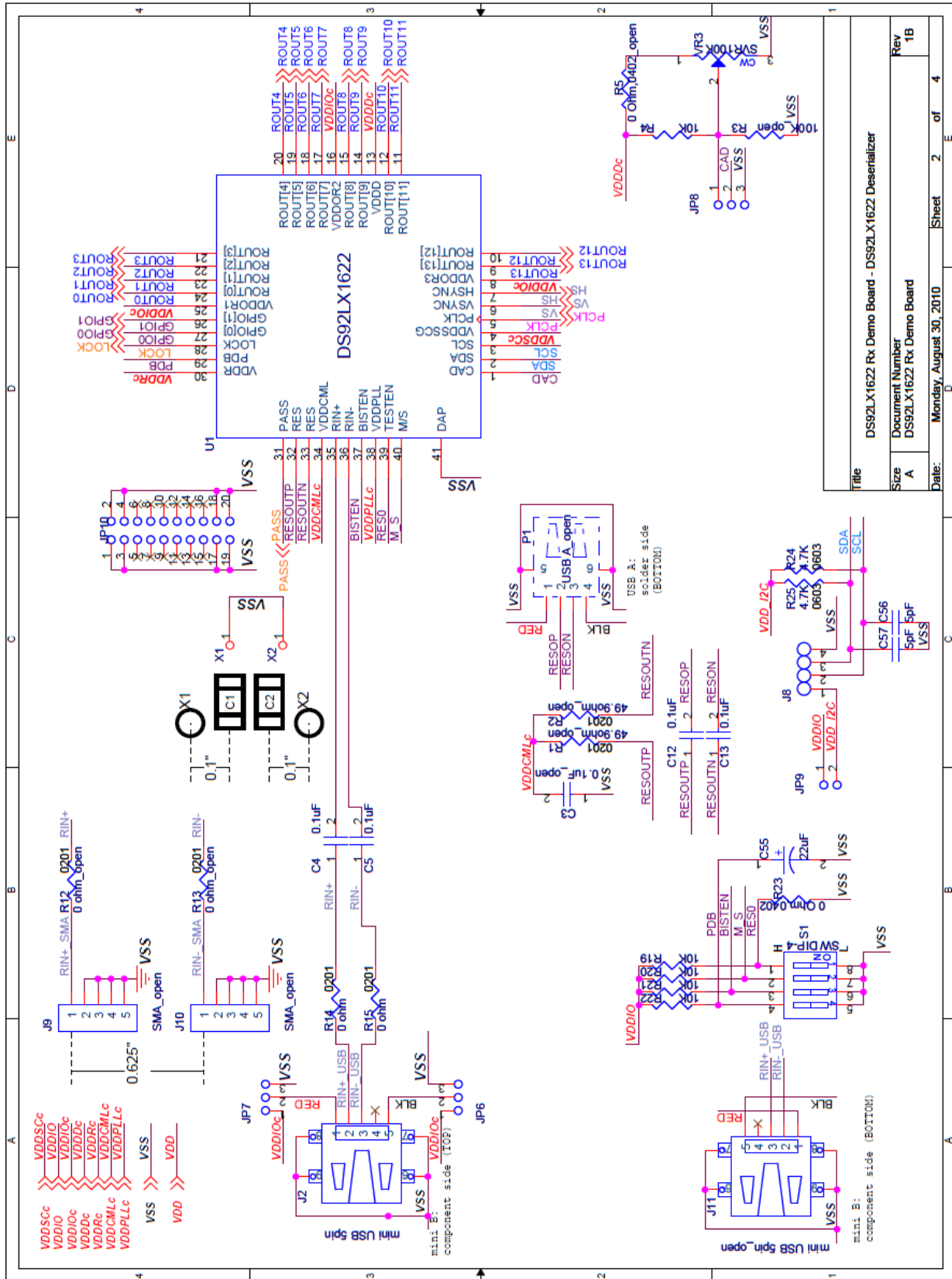
Component	Name	Function
<b>Power Connections</b>		
J3	5V DC	Optional 5V DC Power Jack. Note: implemented by default
J4	1.8V DC	1.8V VDD Power.
JP1	3.3V DC	3.3V VDD Power (left header pin), ground (right header pin)
J5	VSS	Ground.
JP2	VDDIO	Output voltage select. Jumper set to 3.3V by default.
<b>Input and Output Connections</b>		
J7	38 position wall header	Connect to data output.
J9 and J10	SMA Connector	Connect to Channel Link II input. Note: unpopulated by default.
J2	USB Connector (micro-B, female)	Connect to Channel Link II input.
<b>Control Connections</b>		
S1:1	RESO	Reserved. Keep set to LOW.
S1:2	M_S	I2C Mode Select. M_S = H, Slave mode – device will accept a clock from a local master M_S = L, Master mode – device will generate a clock and drive a slave device
S1:3	BISTEN	BIST Enable BISTEN = H, BIST mode enabled BISTEN = L, BIST mode disabled (default)
S1:4	PDB	Power down mode input. PDB = H, Deserializer is enabled (default) PDB = L, Deserializer is in power-down mode
JP8 and VR3	ID[x]	Connect CAD pin to VSS to have the default device PHY address (default setting). Connect CAD pin to VR1 pin; then adjust VR4 value to select desired device PHY address. See datasheet for detailed information.
J8 and JP9	I2C Interface	Leave JP9 unconnected if I2C VDD is provided by an external source. (default).
<b>Others</b>		
LED1	PASS	PASS output. "ON" when PASS is "H"
LED2	LOCK	LOCK output. "ON" when LOCK is "H"
JP6, JP7	Other options	Do not connect

## Rx Board Bill of Materials

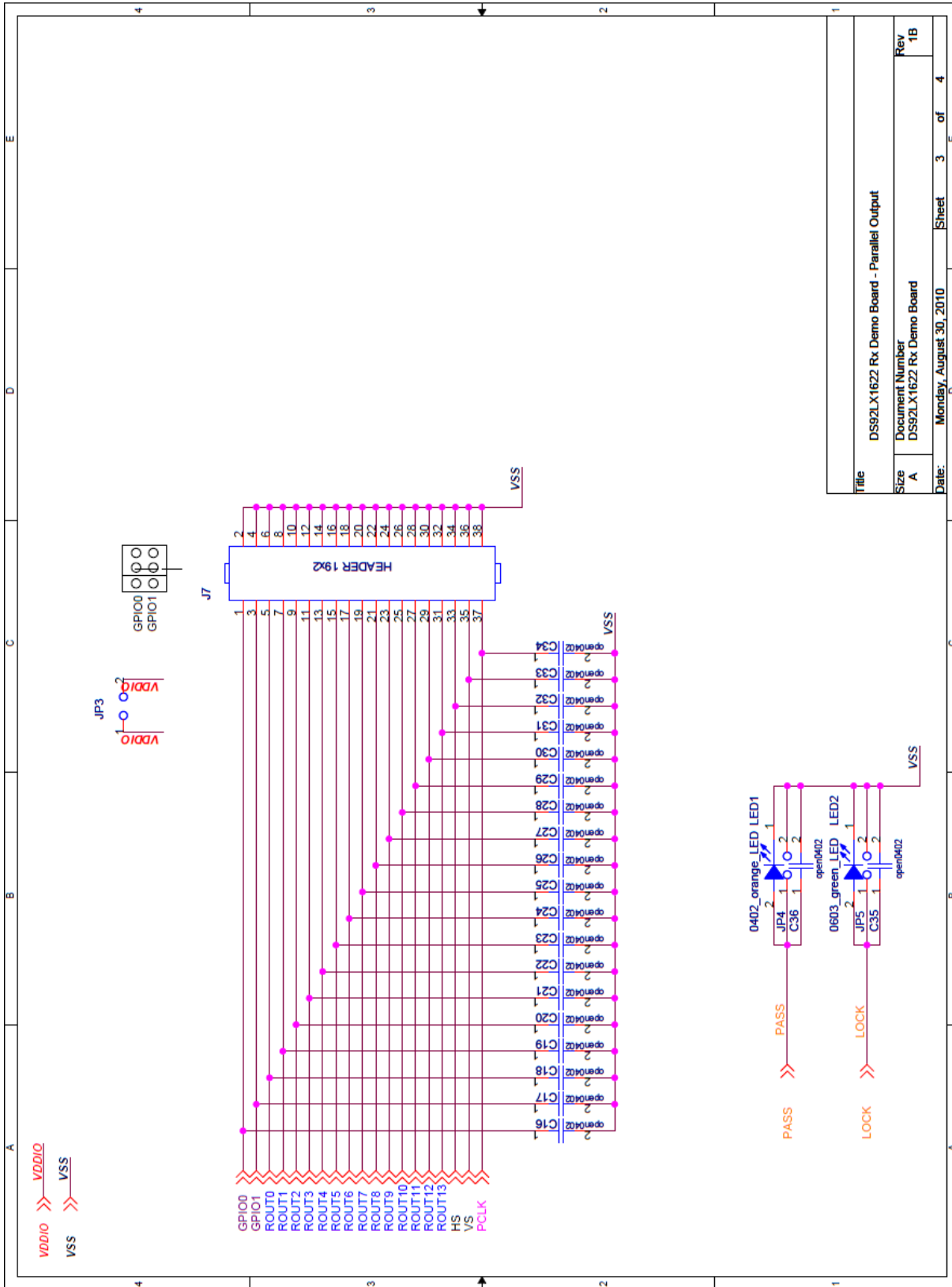
Item	Quantity	Reference	Part	Comments	MFR Part#
1	4	C1,C2,C6,C7	10uF_open	nichicon	493-2365-1-ND_open
2	1	C3	0.1uF_open	Panasonic	PCC1731CT-ND_open
3	4	C4,C5,C12,C13	0.1uF	Panasonic	PCC2398CT-ND
4	2	C8,C11	22uF	nichicon	493-2391-1-ND
5	2	C9,C14	2.2uF	KEMET	399-3714-1-ND
6	2	C15,C10	0.1uF	KEMET	399-1249-1-ND
7	21	C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36	open0402		
8	7	C37,C38,C41,C50,C51,C54, C55	22uF	Kemet	399-3835-1-ND
9	6	C39,C42,C45,C46,C49,C53	0.1uF	Panasonic	PCC2277CT-ND
10	6	C40,C43,C44,C47,C48,C52	0.01uF	KEMET	399-3189-1-ND
11	2	C56,C57	100pF	TDK Corporation	445-1786-1-ND
12	3	JP1,JP3,JP9	2-Pin Header	AMP/Tyco	A26542-ND
13	4	JP2,JP6,JP7,JP8	3-Pin Header	AMP/Tyco	A26545-ND
14	2	JP5,JP4	2-Pin Header_open 2X10-Pin Header, open	AMP/Tyco	A26542-ND
15	1	JP10	HSD_2X2_open	AMP/TYCO	A26580-ND
16	1	J1	mini USB 5pin	Rosenberger	
17	1	J2	CONN JACK	Hirose	H2959CT-ND
18	1	J3	PWR_open	CPU Inc	CP-002A-ND_open
19	2	J4,J5	BANANA 2x4 pin	Johnson	J147-ND
20	1	J6	Jumper_open	Molex	WM26808-ND
21	1	J7	HEADER 19x2	AMP/TYCO	A26588-ND
22	1	J8	IDC1X4	Molex/Waldom Electronics Corp	WM2702-ND
23	2	J10,J9	SMA_open	Johnson Components	J658-ND_open
24	1	J11	mini USB 5pin_open	Hirose Lumex	H2959CT-ND_open
25	1	LED1	0402_orange_LED	Opto/Components Inc	67-1879-1-ND
26	1	LED2	0603_green_LED	LITE-ON INC	160-1446-1-ND
27	1	P1	USB A_open	AMP/Tyco	A31726-ND_open
28	2	R1,R2	49.9ohm_open	Venkel	
29	1	R3	100K_open	Panasonic	P100KHCT-ND_open
30	5	R4,R19,R20,R21,R22	10K	Panasonic	P10.0KHCT-ND

Item	Quantity	Reference	Part	Comments	MFR Part#
31	1	R5	0 Ohm,0402_open	Panasonic	P0.0JTR-ND_open
32	2	R6,R7	82.5ohm	Panasonic	P82.5HCT-ND
33	1	R8	100ohm_open	Panasonic	P100HCT-ND_open
34	6	R9,R10,R11,R16,R17,	Ferrite Bead	Murata	490-5442-1-ND
34a	1	R23	0 Ohm,0402	Panasonic	P0.0JTR-ND
35	2	R12,R13	0 ohm_open		
36	2	R14,R15	0 ohm	any	
37	2	R25,R24	1.0K	Panasonic	P1.0KGCT-ND
38	1	S1	SW DIP-4	Grayhill	GH7184-ND
39	1	U1	DS92LX1622	National	

# Rx Board Schematics



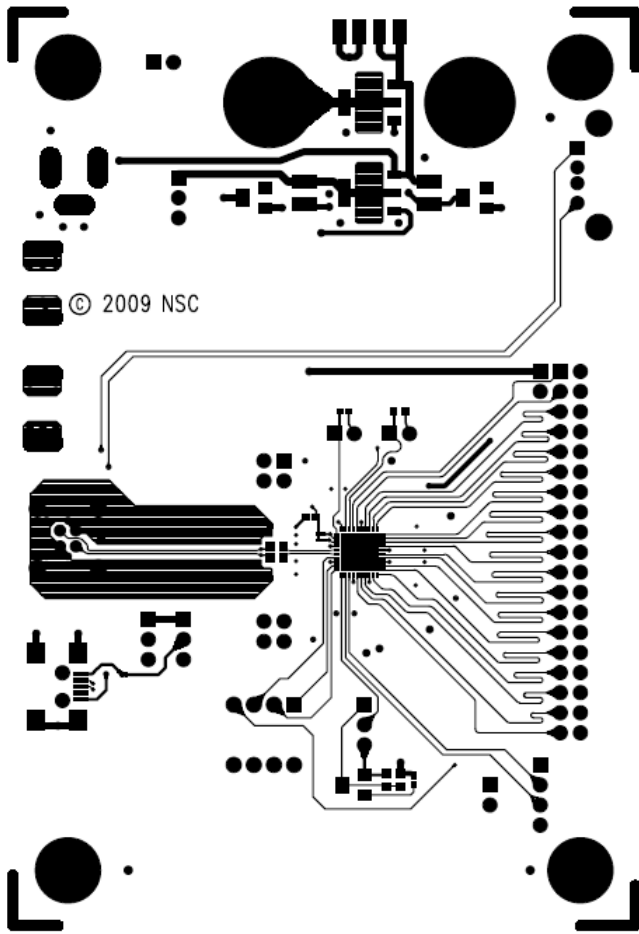
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DS92LX1622 Rx Demo Board - DS92LX1622 Deserializer			
Size	Document Number	Rev	
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Date:	Monday, August 30, 2010	Sheet	2 of 4



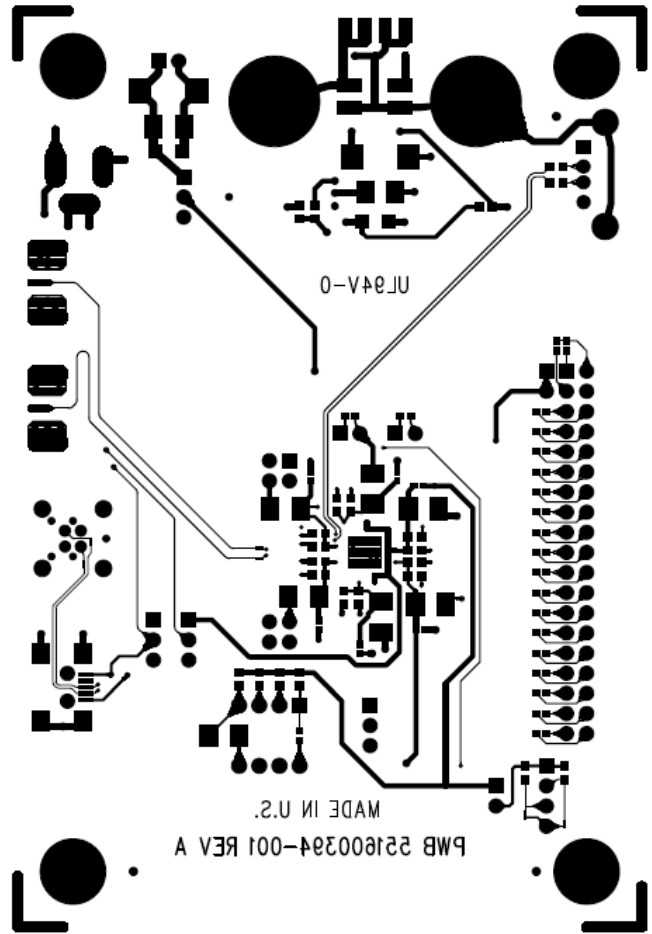
Title	DS92LX1622 Rx Demo Board - Parallel Output
Size	Document Number
A	DS92LX1622 Rx Demo Board
Date:	Monday, August 30, 2010
Sheet	3 of 4
Rev	1B



# Rx Board Reference Layout



Top Layer



Bottom Layer