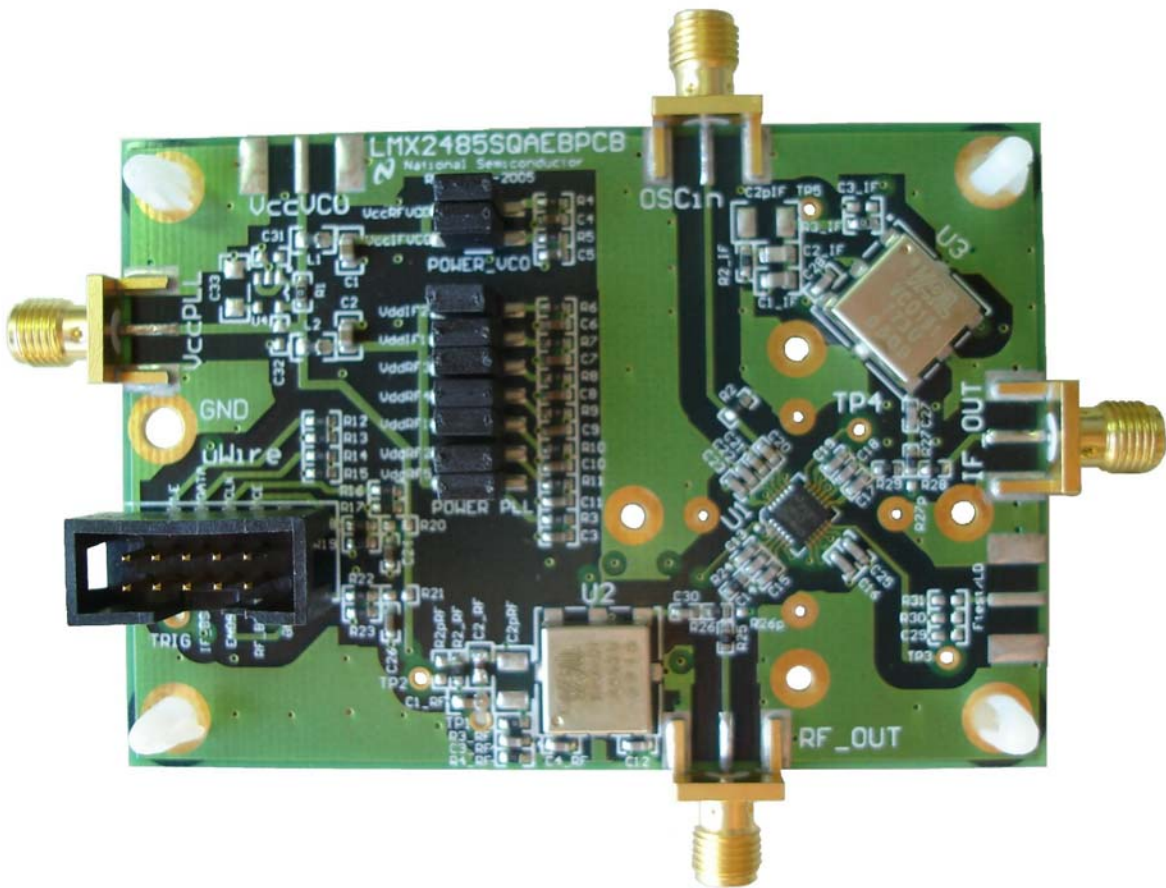




LMX2485 Evaluation Board Instructions



National Semiconductor Corporation
Wireless Communications, RF Products Group

2900 Semiconductor Dr.
M/S A2-600
Santa Clara, CA, 95052-8090

LMX2485SQFPEBI Rev 1.24.2006



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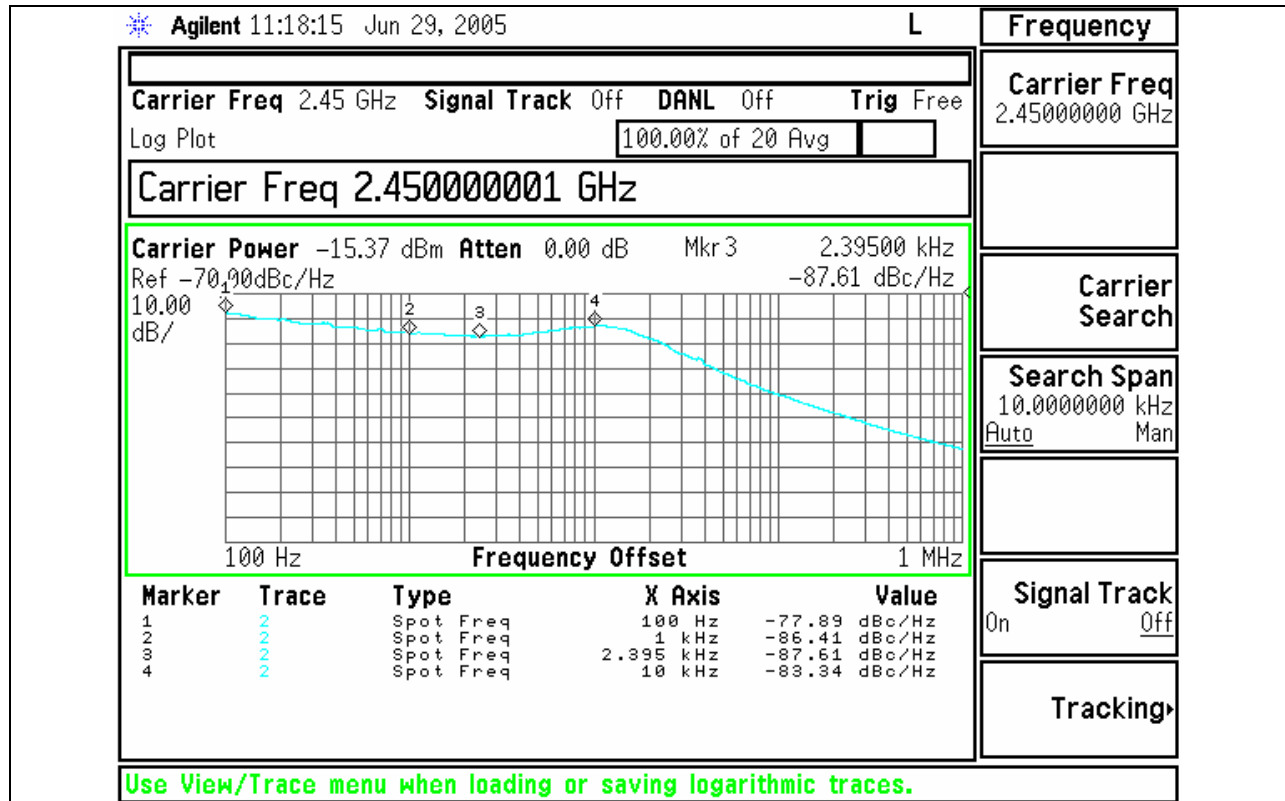
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General Description

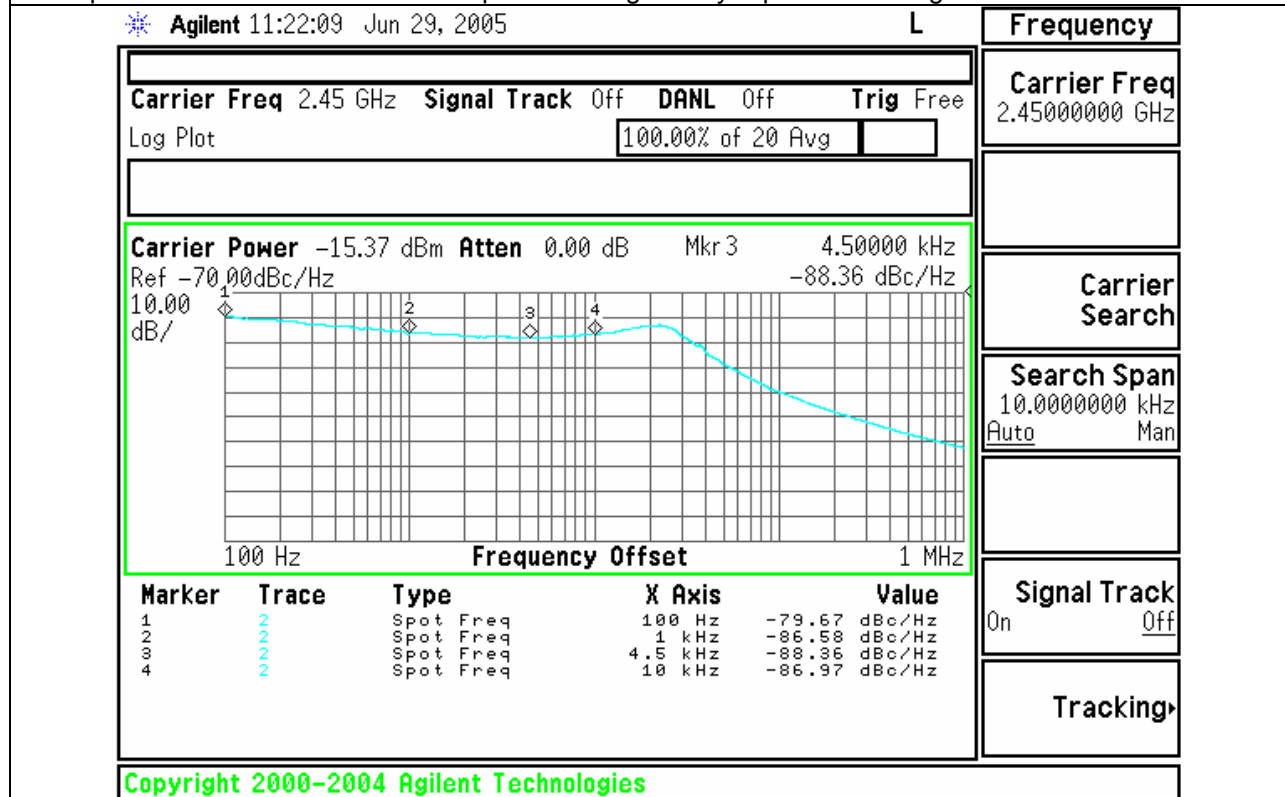
The LMX2485 Evaluation Board simplifies evaluation of the LMX2485 2.6 GHz/0.8 GHz PLLatinum™ dual frequency synthesizer. The board enables all performance measurements with no additional support circuitry. The evaluation board consists of a LMX2485 device, a RF VCO module and IF VCO & RF/IF loop filters built by discrete components. The SMA flange mount connectors are provided for external reference input, RF and IF VCO outputs, and the power and grounding connection. A cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of MICROWIRE™ serial port emulation, the CodeLoader software included can be run on a PC to facilitate the LMX2485 internal register programming for the evaluation and measurement.

RF Loop Filter			
Phase Margin	39.4 deg	Pole Ratio T3 /T1	51.2 %
Loop Bandwidth	11.3 KHz	Pole Ratio T4/T3	31.1 %
Theoretical Lock Time (Assuming no cycle slipping)	508 uS for 2400 – 2480 MHz to 1 kHz tolerance	Roll-Off @ 200 KHz	-51.1 dB
		Settings for Operation	
		$K\phi$	8X (760 uA)
		Comparison Frequency	20 MHz
		Output Frequency	2400 – 2500 MHz
		PLL Supply	3.3 Volts
		Other Information	
		VCO Used	VARIL191-2450U
VCO Gain	55 MHz/Volt		
VCO Input Capacitance	22 pF		
IF Loop Filter			
Phase Margin	46.4 deg	Theoretical Lock Time	508 uS for 760 - 780 MHz to 1 KHz tolerance
Loop Bandwidth	4.7 KHz	Spur Gain @ 50 KHz	50.5 dB
		Settings for Operation	
		$K\phi$	3.5 mA
		Comparison Frequency	50 kHz
		Output Frequency	760 - 780 MHz
		PLL Supply	3.3 Volts
		Other Information	
		VCO Used	VARIL191-773U
VCO Gain	18 MHz/Volt		
VCO Input Capacitance	100 pF		

RF PLL Phase Noise



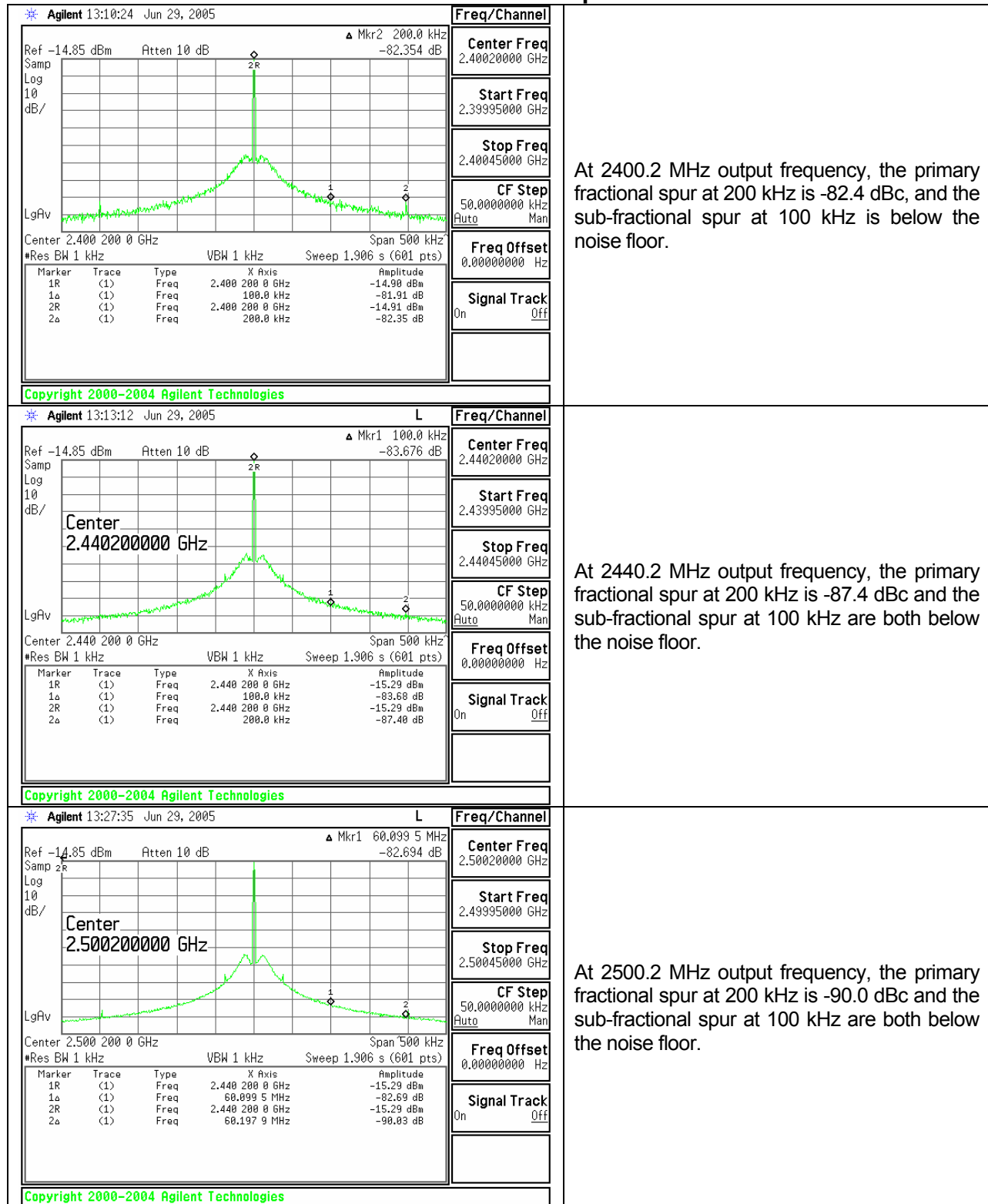
Loop Bandwidth is about 10 kHz. The phase noise gradually improves as one goes farther from the carrier.



For this plot, the charge pump was increased to 16X.



RF PLL Fractional Spurs





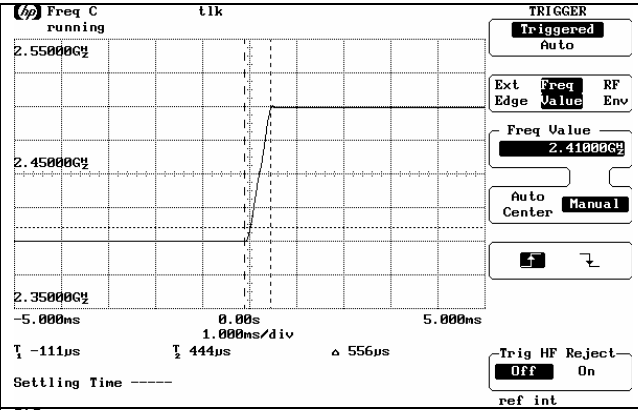
RF PLL Lock Time

No CSRC. RF_TOC=0	<p>VERTICAL Center/Top/Bottom Center 2.450000GHz Span 200.00MHz 25.00MHz/div Find Center Find Center and Span ref int</p>	Peak time without cycle slip reduction is 1733 μ S.
	<p>Time Markers Off On T1 [---] -111us T2 [----] 1.356ms Freq Markers Off F/ΔF TRACK Analyze All Between Markers ref int</p>	Peak time without cycle slip reduction is 1467 μ S.
	<p>Time Markers Off On T1 [---] Trigger Point T2 [----] Settling Time Freq Markers Off F/ΔF TRACK F 2.500000000GHz ΔF +/- 1.000kHz Analyze All Between Markers ref int</p>	Positive lock time is 1793 μ S
	<p>Time Markers Off On T1 [---] Trigger Point T2 [----] Settling Time Freq Markers Off F/ΔF TRACK F 2.400000000GHz ΔF +/- 1.000kHz Analyze All Between Markers ref int</p>	Negative Lock time is 1661 μ S

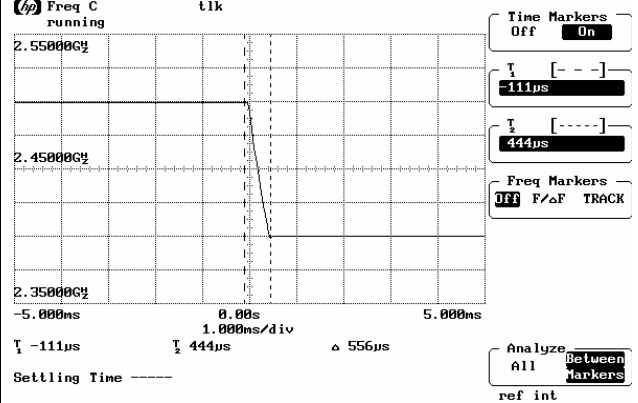


RF PLL Lock Time

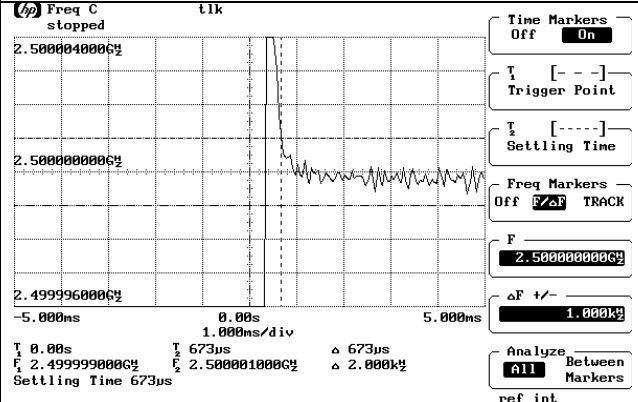
Cycle Slip Reduction Enabled. RF_TOC=2500



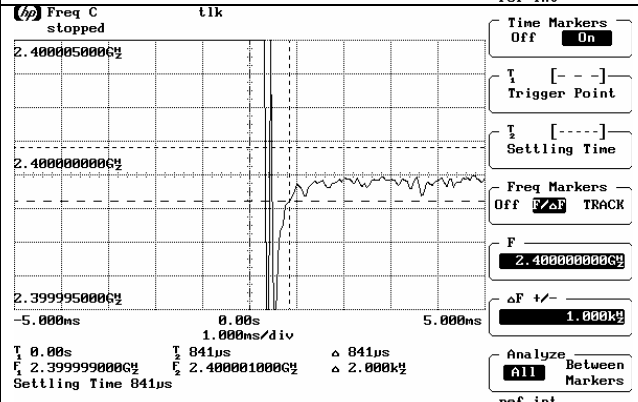
Peak time with cycle slip reduction is 556 µs.



Peak time with cycle slip reduction is 556 µs.



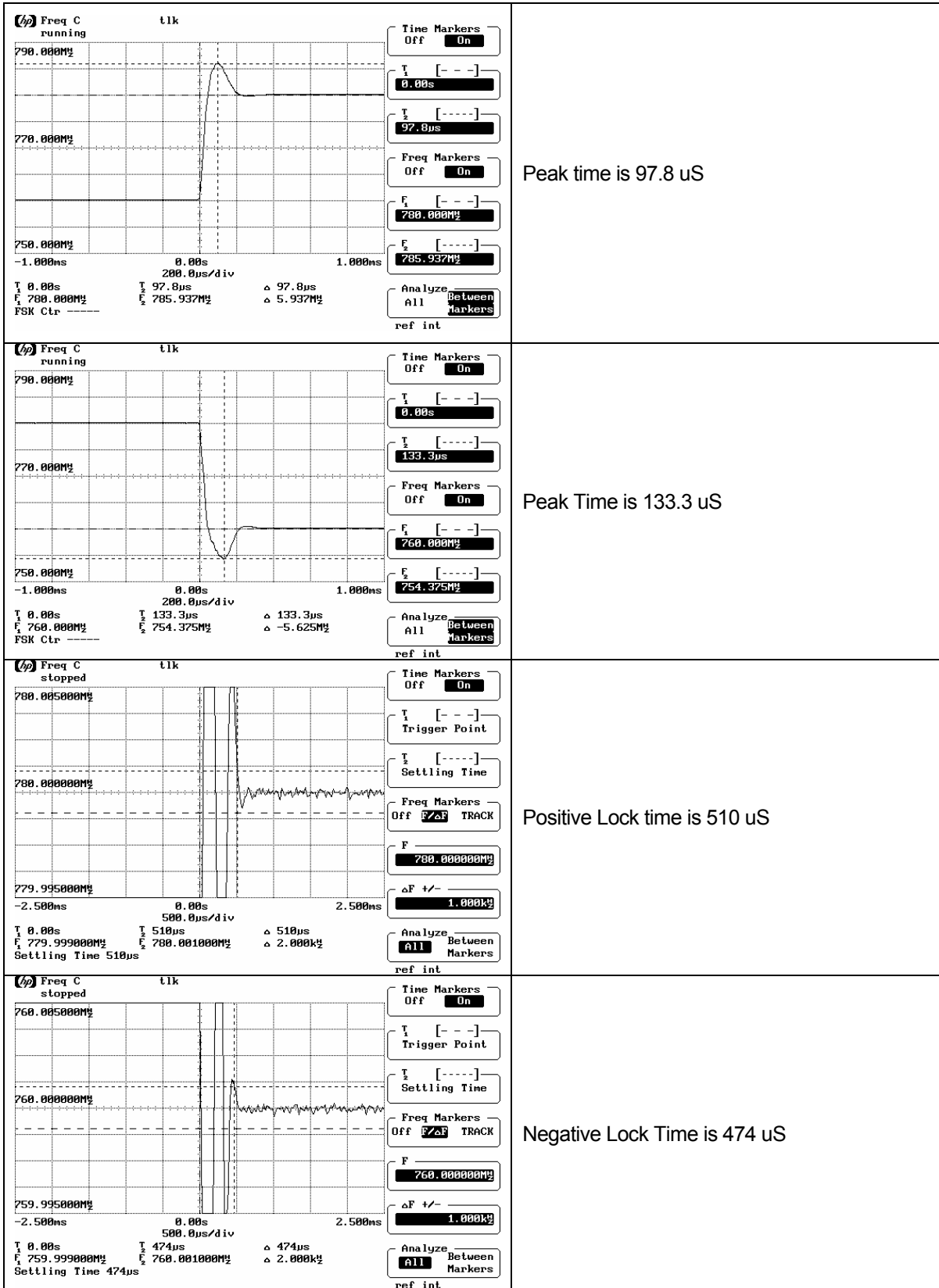
Positive lock time is 673 µs



Negative Lock time is 841 µs



IF PLL Lock Time



IF PLL Phase Noise

Agilent 11:09:34 Oct 1, 2004 T

Carrier Freq 770 MHz Signal Track Off DANL Off Trig Free

Log Plot 100.00% of 50 Avg

Carrier Freq 770.0000003 MHz

Carrier Power -8.30 dBm Atten 0.00 dB Mkr 4 100.000 kHz
 Ref -60.00dBc/Hz -119.38 dBc/Hz

Marker	Trace	Type	X Axis	Value
1	2	Spot Freq	100 Hz	-78.97 dBc/Hz
2	2	Spot Freq	1 kHz	-77.53 dBc/Hz
3	2	Spot Freq	10 kHz	-80.31 dBc/Hz
4	2	Spot Freq	100 kHz	-119.38 dBc/Hz

Frequency

Carrier Freq 770.000000 MHz

Carrier Search

Search Span 10.0000000 kHz
 Auto Man

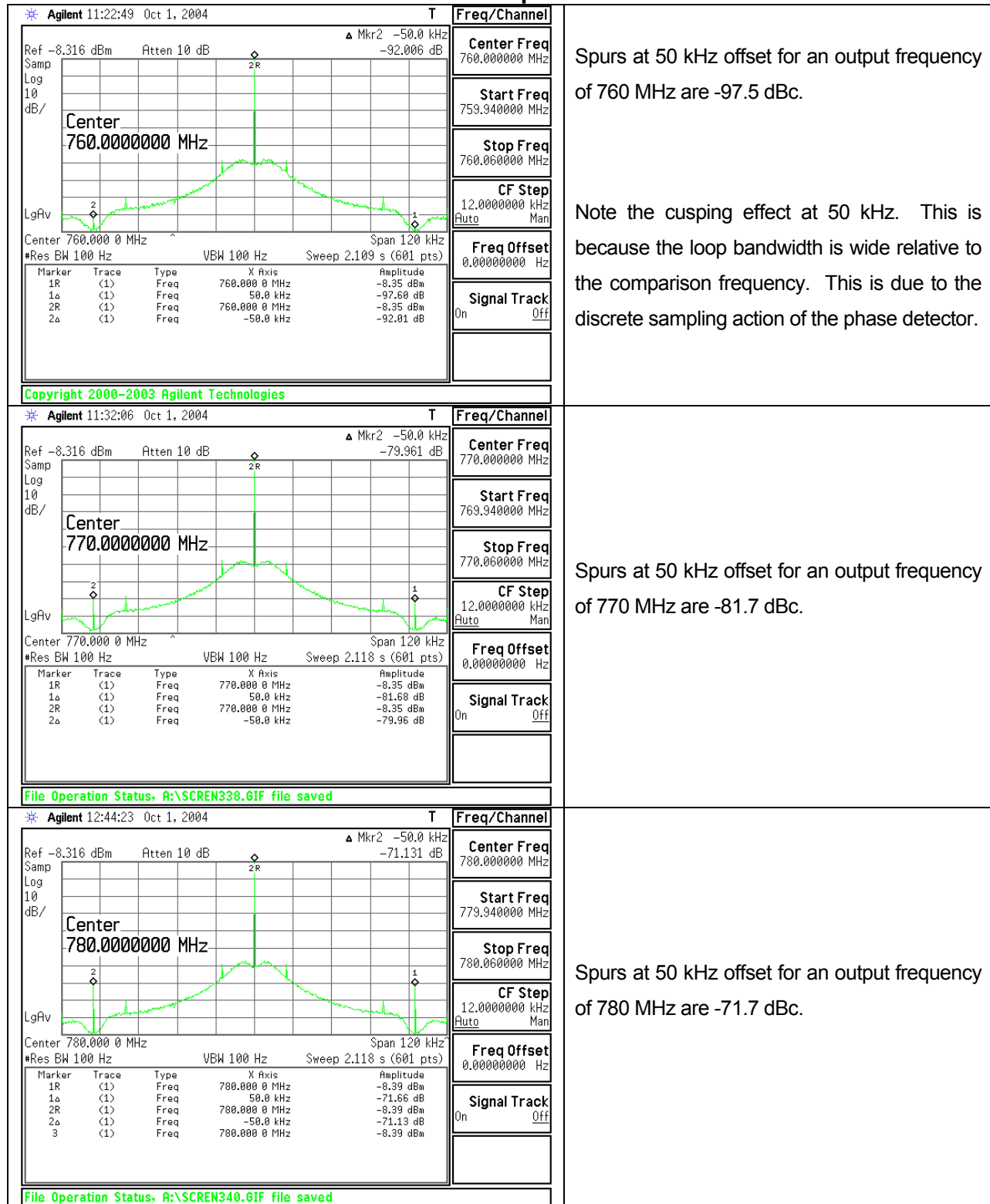
Signal Track
 On Off

Tracking

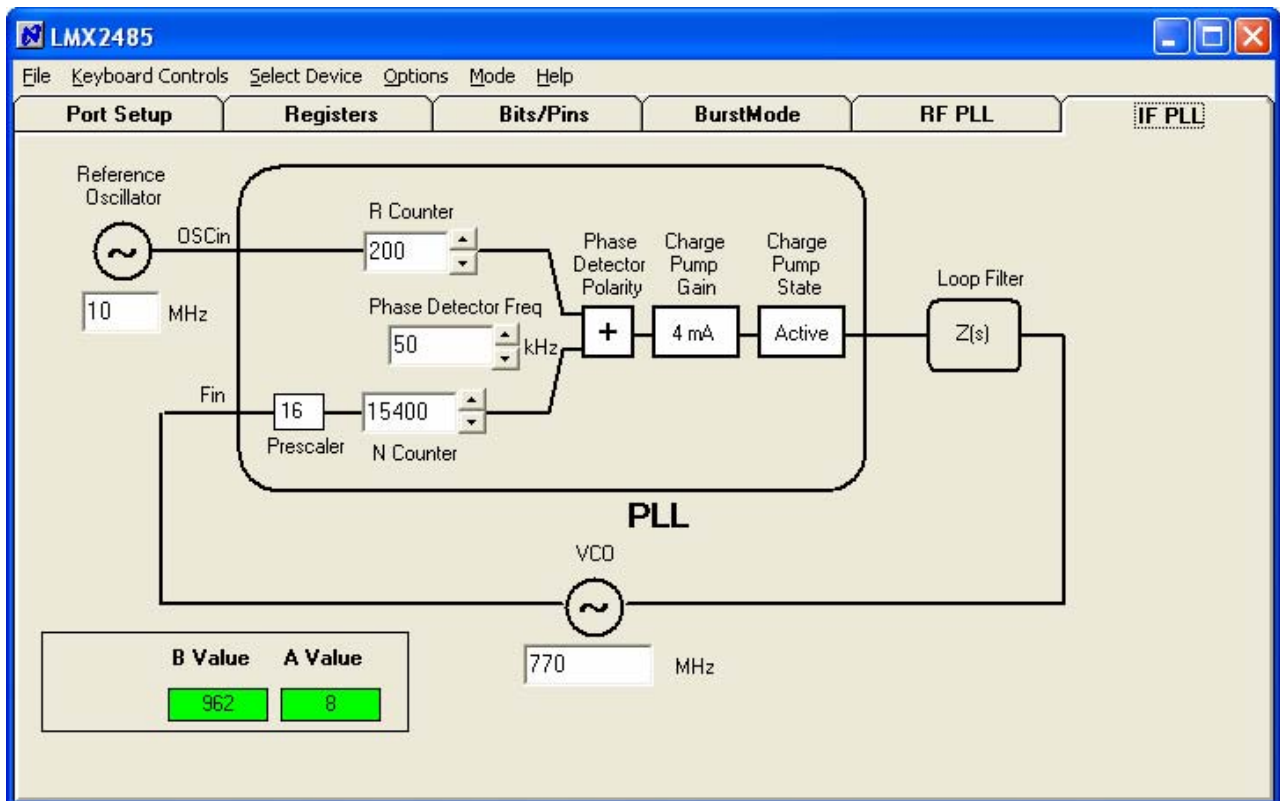
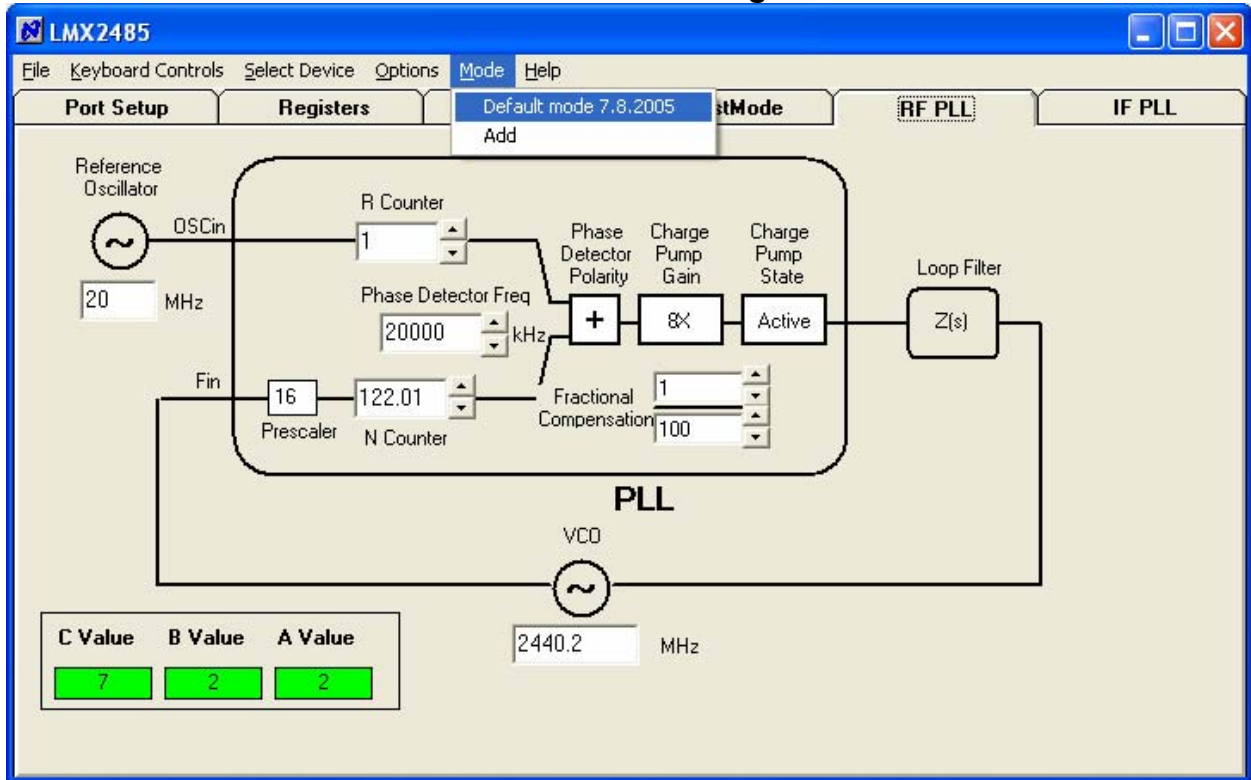
Use View/Trace menu when loading or saving logarithmic traces.

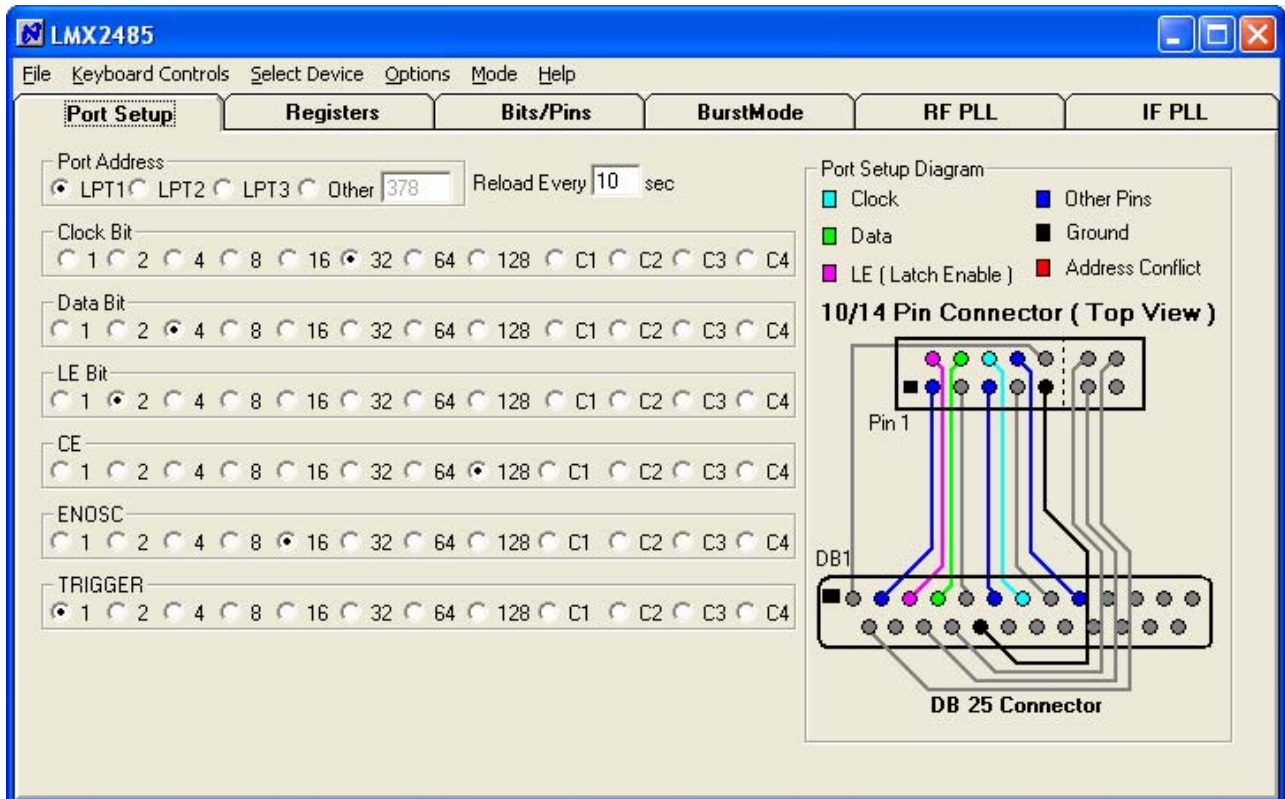
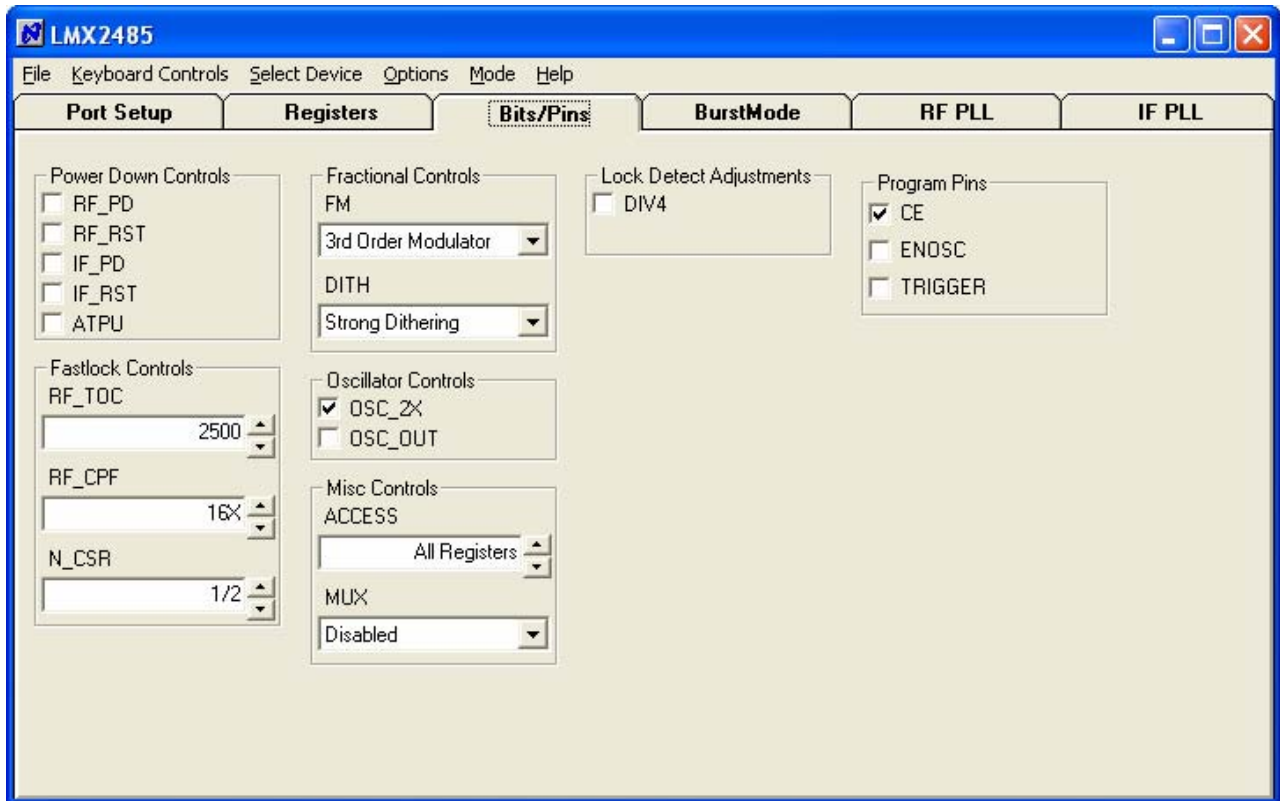


IF PLL Spurs



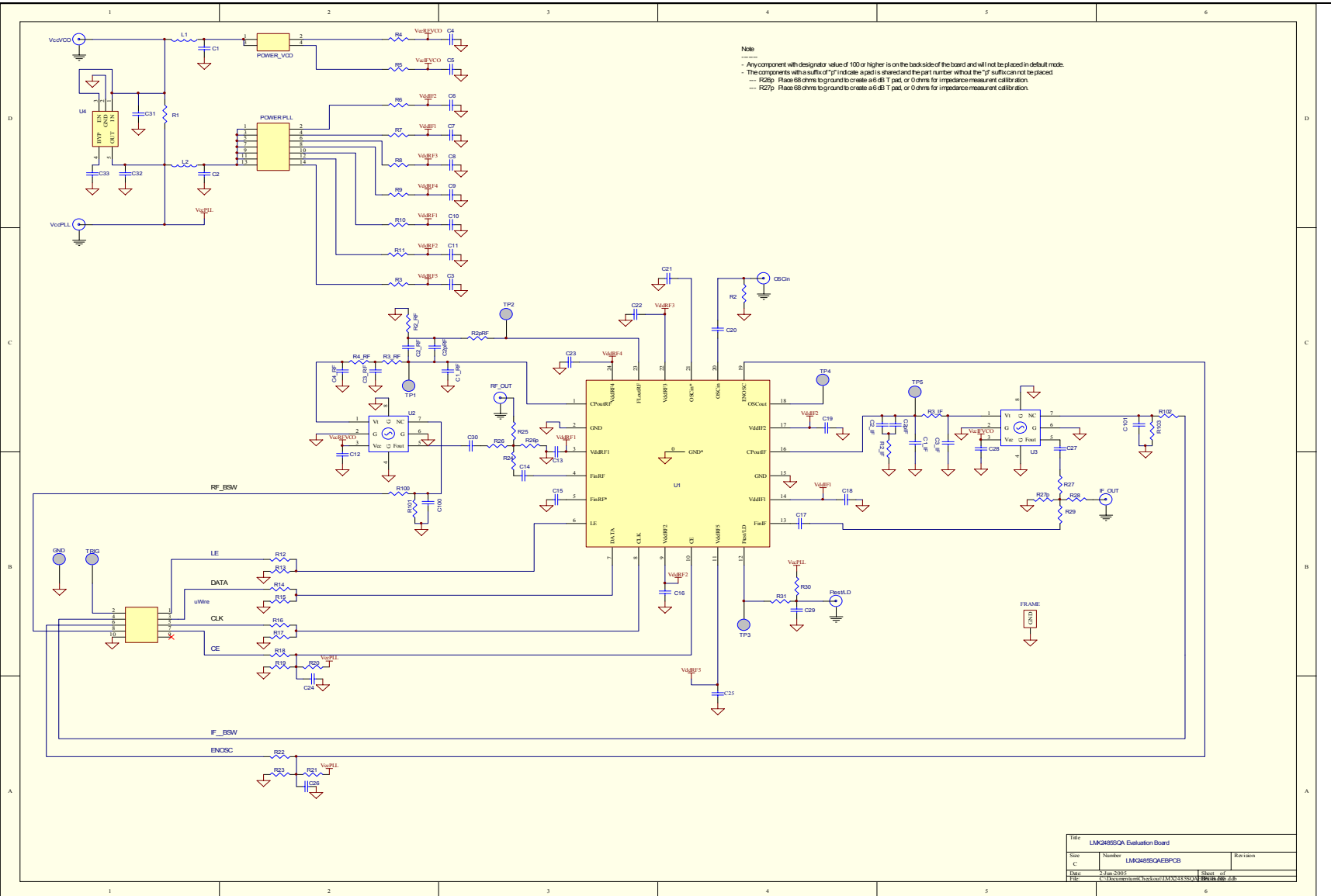
CodeLoader Settings







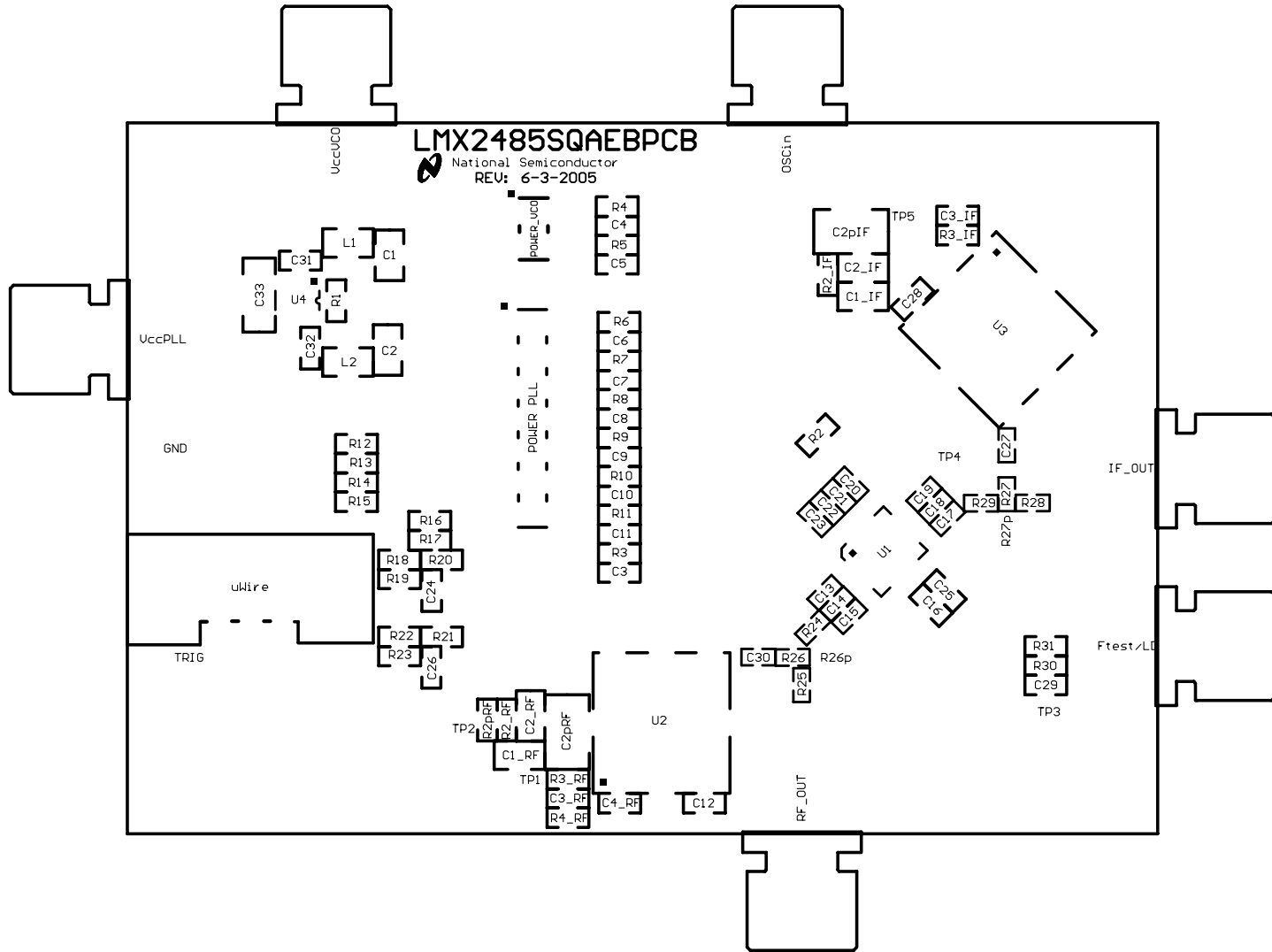
Schematic



Title	LMX2485QA Evaluation Board		
Size	Number	Rev	Issued
C	LMX2485QAEBPCB		
Date	2-Jan-2003	Sheet	of
File	C:\Users\johnd\Documents\LMX2485QA\PCB\LMX2485QAEBPCB.dwg		

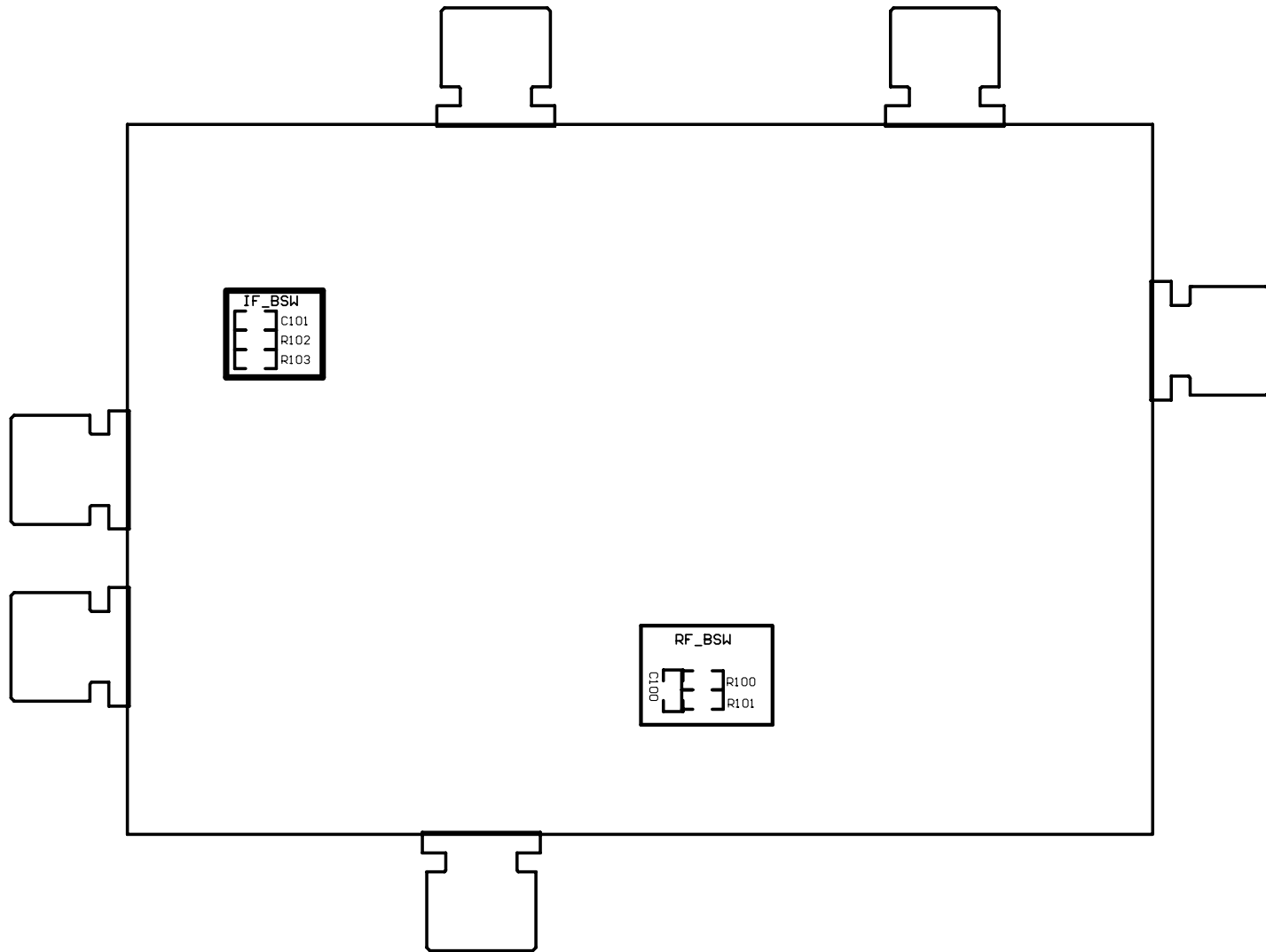


Top Build Diagram





Bottom Build Diagram





Bill of Materials

Revision		6/24/2005								
Item	Qty	Manufacturer	Part Number	Value	Unit	Size	Voltage	Tolerance	Material	Designator
0	23	Open, No Component								C2pRF, C2pIF, C3_IF, C29, C31, C32, C33 R2pRF, R20, R21, R26p, R27p, R30, R31 R100, R101, R102, R103, C100, C101, VccVCO, Ftest/LD, U4
1	1	National Semiconductor	LMX2485SQAEBPCB	er = 4, First GND 10 mils down		4 layer board. 62 mils total thickness			FR4	n/a
2	4	SPC Technology	SPCS-8	Stand-Offs					Nylon	Place in 4 holes in edge of board
3	9	Com Con Connectors	CCIJ255G	2-Pin	Shunt				Plastic	Place across POWER_PLL (1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14) and POWER_VCO (1-2, 3-4)
4	1	Com Con Connectors	HTSM3203-4G2	4-Pin	Header				Plastic	POWER_VCO
5	1	Com Con Connectors	HTSM3203-14G2	14-Pin	Header				Plastic	POWER_PLL
6	1	FCI Electronics	52601-S10-8	10-Pin	Header				Plastic	uWire
7	4	Johnson Components	142-0701-851	Edge SMA					Metal	IF_OUT, OSCin, RF_OUT, VccPLL
8	14	Kemet	C0603C470J5GAC	47	pF	603	50 V	5%	C0G	C12, C13, C14, C15, C16, C17, C18, C19, C22, C23, C25, C27, C28, C30
9	1	Kemet	C0603C561J5GAC	560	pF	603	50 V	5%	C0G	C4_RF
10	1	Kemet	C0603C821J5GAC	820	pF	603	50 V	5%	C0G	C3_RF
11	1	Kemet	C0805C182J3GAC	1.8	nF	805	25 V	5%	C0G	C1_IF
12	1	Panasonic	ECHU1C103JX5	10	nF	805	16 V	5%	Film	C2_IF
13	1	Kemet	C0805C153J3RAC	15	nF	603	25 V	5%	X7R	C1_RF
14	2	Kemet	C0603C104K3RAC	100	nF	603	25 V	10%	X7R	C20, C21
15	1	Kemet	C0603C154K4RACTU	150	nF	603	16	10%	X7R	C2_RF
16	11	Kemet	C0603C105K4PAC	1	uF	603	16 V	10%	X5R	C3, C4, C5, C6, C7, C8, C9, C10, C11, C24, C26
17	2	Kemet	C0805C106K8PAC	10	uF	805	10 V	10%	X5R	C1, C2
18	2	Vishay	CRCW0603000ZRT1	0	Ω	0603	10 V	5%	Ceramic	R1, R3_IF
19	9	Vishay	CRCW0603100JRT1	10	Ω	0603	10 V	5%	Ceramic	R3, R4, R5, R6, R7, R8, R9, R10, R11
20	6	Vishay	CRCW0603180JRT1	18	Ω	0603	10 V	5%	Ceramic	R24, R25, R26, R27, R28, R29
21	1	Vishay	CRCW0603510FRT1	51	Ω	0603	10 V	1%	Ceramic	R2
22	1	VISHAY	CRCW0603221JRT1	220	Ω	0603	10 V	5%	Ceramic	R2_RF
23	1	VISHAY	CRCW0603152JRT1	1.5	KΩ	0603	10 V	5%	Ceramic	R3_RF
24	1	VISHAY	CRCW0603272JRT1	2.7	KΩ	0603	10 V	5%	Ceramic	R4_RF
25	1	Vishay	CRCW0603822JRT1	8.2	KΩ	0603	10 V	5%	Ceramic	R2_IF
26	5	Vishay	CRCW0603103JRT1	10	KΩ	0603	10 V	5%	Ceramic	R12, R14, R16, R18, R22
27	5	Vishay	CRCW0603123JRT1	12	KΩ	0603	10 V	5%	Ceramic	R13, R15, R17, R19, R23
28	2	Steward	LI0603D301R-00	Inductor	nH	603			Ferrite	L1, L2
29	1	National Semiconductor	LMX2485SQ	PLL	n/a	24P	3.6	n/a	Silicon	U1
30	1	VARIL	VCO191-2450U	2400 - 2480	MHz	U	3 V		Can	U2
31	1	VARIL	VCO191-773U	760-780	MHz	U	3 V		Can	U3

Additional Features of the LMX2485 Evaluation Board

HYBRID VCO FOOTPRINT

Although the evaluation board is created to support a particular VCO, the footprint is flexible and designed such that other VCOs are easy to put on the board. To mount a smaller VCO on the board, scratch off the solder mask with the flat edge of a screwdriver and then put solder on the pads such that it covers the exposed copper.

TEST POINTS

Test Point	Function
TP1	RF Charge Pump voltage
TP2	RF Fastlock output
TP3	Ftest/LD output
TP4	OSCoout pin
TP5	IF Charge Pump Output
TRIG	Microwire trigger

BANDSWITCH VCO SUPPORT

The board is also configured so that CodeLoader can control a bandswitch VCO for either the RF or IF PLL. In order to do this, one can use the trigger pin. Don't forget to stuff the components on the bottom layer from this.

COMPONENT OPTIONS

Some components have a 'p' suffix to denote it as an option. These usually have shared footprints and can not both be stuffed. Below is a list of these options.

Component	Option
C2_RF & C2pRF	These components both add in parallel. There are 2 footprints here to allow for different sizes of capacitors
C2_IF & C2pIF	These components both add in parallel. There are 2 footprints here to allow for different sizes of capacitors
R2_RF & R2pRF	During Fastlock, the chip switches R2pRF in parallel with R2_RF
R26 & R26p	For normal operation, R26p should be open. However, for sensitivity measurements, 68 Ω may be placed in R26p and R26 can be removed in order to form a 6 dB T-Pad.
R27 & R27p	For normal operation, R27p should be open. However, for sensitivity measurements, 68 Ω may be placed in R27p and R27 can be removed in order to form a 6 dB T-Pad.