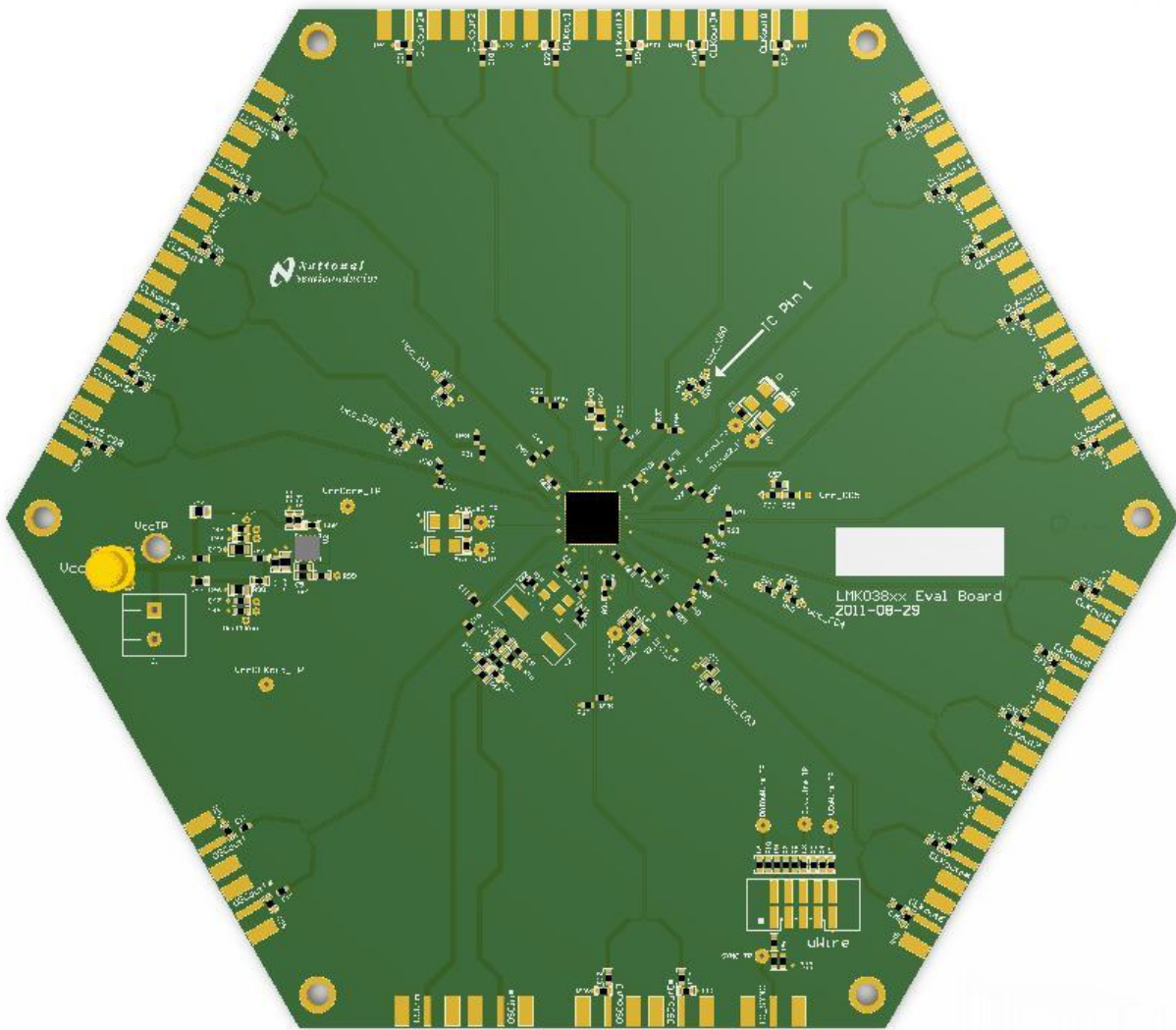




LMK03806
Ultra Low Jitter Clock Generator



LMK03806 Evaluation Board Operating Instructions

Texas Instruments
October 2011

Table of Contents

TABLE OF CONTENTS	2
GENERAL DESCRIPTION	4
EVALUATION BOARD KIT CONTENTS	4
QUICK START	5
DEFAULT CODELOADER MODES FOR EVALUATION BOARDS.....	6
EXAMPLE: USING CODELOADER TO PROGRAM THE LMK03806B	7
1. START CODELOADER 4 APPLICATION.....	7
2. SELECT DEVICE	7
3. PROGRAM/LOAD DEVICE.....	8
4. RESTORING A DEFAULT MODE.....	8
5. VISUAL CONFIRMATION OF FREQUENCY LOCK.....	9
6. ENABLE CLOCK OUTPUTS.....	9
PLL LOOP FILTERS AND LOOP PARAMETERS	10
PLL LOOP FILTER	10
<i>Integrated VCO PLL</i>	10
EVALUATION BOARD INPUTS AND OUTPUTS	11
RECOMMENDED TEST EQUIPMENT	15
APPENDIX A: CODELOADER USAGE	16
PORT SETUP TAB	16
CLOCK OUTPUTS TAB	17
PLL TAB.....	18
BITS/PINS TAB	19
REGISTERS TAB.....	21
APPENDIX B: TYPICAL PHASE NOISE PERFORMANCE PLOTS	22
PLL.....	22
<i>VCO Clock Output Phase Noise</i>	22
CLOCK OUTPUTS (CLKOUT)	23
<i>CLKout Phase Noise (div12 and div24)</i>	23
APPENDIX C: SCHEMATICS	25
POWER SUPPLIES.....	25
LMK03806B DEVICE WITH LOOP FILTER AND CRYSTAL CIRCUITS	26
OUTPUTS, (OSCOU0/1, CLKOUT0/1/2/3)	27
CLOCK OUTPUTS (CLKOUT 4/5/6/7).....	28
CLOCK OUTPUTS (CLKOUT8/9/10/11)	29
APPENDIX D: BILL OF MATERIALS	30
APPENDIX E: PCB LAYERS STACKUP	34
APPENDIX F: PCB LAYOUT	35
LAYER #1 – TOP	35
LAYER #2 – RF GROUND PLANES.....	36
LAYER #3 – VCC PLANES	37

LAYER #4 – BOTTOM.....	38
LAYERS #1 AND 6 – TOP AND BOTTOM (COMPOSITE).....	39
APPENDIX G: PROPERLY CONFIGURING LPT PORT	40
LPT DRIVER LOADING.....	40
CORRECT LPT PORT/ADDRESS	40
CORRECT LPT MODE.....	41
APPENDIX H: TROUBLESHOOTING INFORMATION	42
1) CONFIRM COMMUNICATIONS	42

General Description

The LMK03806 Evaluation Board simplifies evaluation of the LMK03806B high performance, ultra low-jitter, multirate clock generator. Texas Instruments *CodeLoader* software can be used to program the internal registers of the LMK03806B device through the MICROWIRE™ interface. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC and can be downloaded from <http://www.national.com/timing/software/>.

Evaluation Board Kit Contents

The evaluation board kit includes:

- (1) LMK03806 Evaluation Board
- (1) LMK03806 Family Quick Start Guide
 - Evaluation board instructions can be downloaded from www.national.com.
- (1) CodeLoader uWire cable (LPT → uWire)

Quick Start

1. Connect a voltage of **5.0 volts** to the Vcc SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO.
2. Connect the uWire header to a computer parallel port with the CodeLoader cable. A USB communication option is also available, search at www.national.com for: USB2UWIRE-IFACE.
3. Program the device with CodeLoader. CodeLoader is available for download at: www.national.com/timing/software/
 - a. Select correct LMK03806B from “Select Device → Clock Conditioners” Menu.
 - b. Select a default mode from the “Mode” Menu. For the quick start use, “**20 MHz Crystal**”
 - c. **Ctrl-L** must be pressed at least once to load all registers. Alternatively click menu Keyboard Controls → Load Device.
4. Measurements may be made at an active CLKout port via its SMA connector.

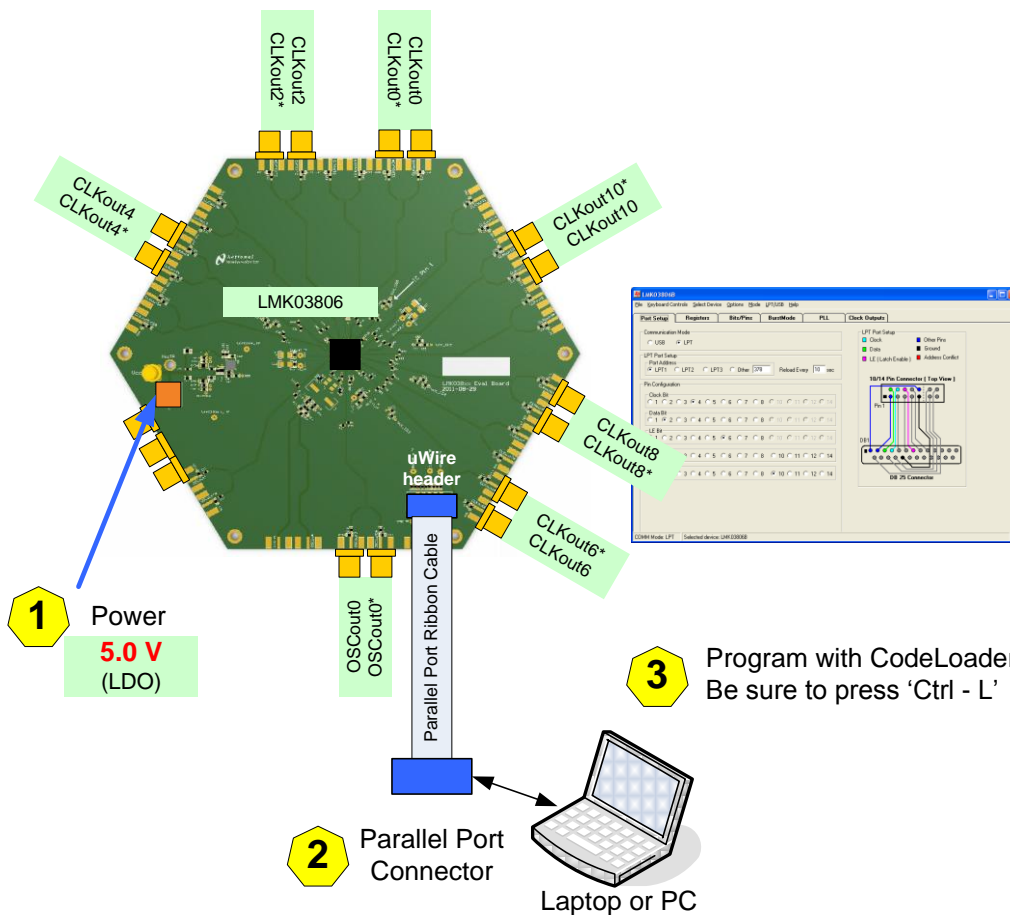


Figure 1: Quick Start Diagram

Default CodeLoader Modes for Evaluation Boards

CodeLoader saves the state of the selected LMK03806B device when exiting the software. To ensure a common starting point, the following modes listed in Table 1 **Error! Reference source not found.** may be restored by clicking “Mode” and selecting the appropriate device configuration, as shown in Figure 2 in the case of the LMK03806B device. Similar default modes are available for each LMK03806B device in CodeLoader.

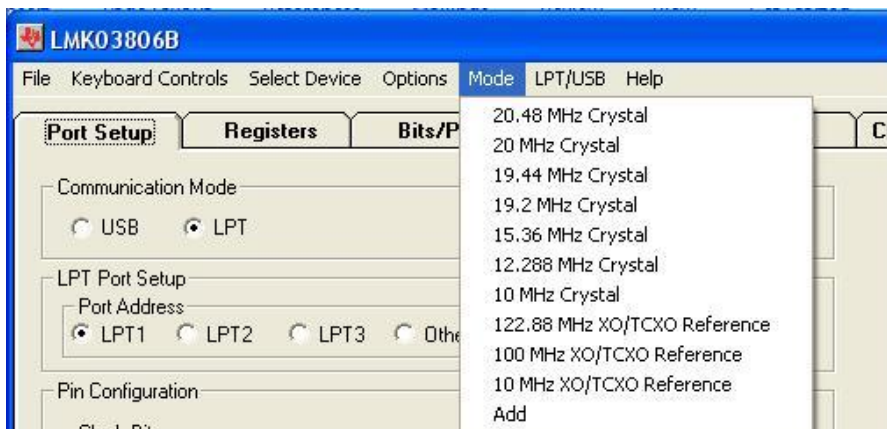


Figure 2: Selecting a Default Mode for the LMK03806B Device

After restoring a default mode, press Ctrl+L to program the device. The default modes also disable certain outputs, so make sure to enable the output under test to make measurements.

Table 1 - Default CodeLoader Modes for LMK03806

Default CodeLoader Mode	XTAL Frequency
LMK03806B, 20 MHz	20 MHz

The next section outlines step-by-step procedures for using the evaluation board with the LMK03806B.

Example: Using CodeLoader to Program the LMK03806B

The purpose of this section is to walk the user through using CodeLoader 4 to make some measurements with the LMK03806B device as an example. For more information on CodeLoader refer to Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at <http://www.national.com/timing/software/>.

Before proceeding, be sure to follow the Quick Start section above to ensure proper connections.

1. Start CodeLoader 4 Application

Click “Start” → “Programs” → “CodeLoader 4” → “CodeLoader 4”

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

2. Select Device

Click “Select Device” → “Clock Conditioners” → “LMK03806B”

Once started CodeLoader 4 will load the last used device.

To load a new device click “Select Device” from the menu bar, then select the subgroup and finally device to load. For this example, the LMK03806B is chosen.

Selecting the device does cause the device to be programmed.

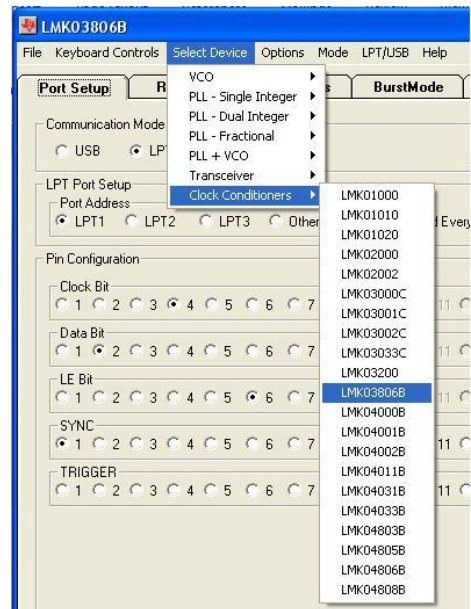


Figure 3 - Selecting the LMK03806B Device

3. Program/Load Device

Assuming the Port Setup settings are correct, press the “Ctrl+L” shortcut or click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK03806 file.



Figure 4 – Loading the Device

Once the device has been initially loaded, CodeLoader will automatically program changed registers so it is not necessary to re-load the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoReload with Changes.”

Because a default mode will be restored in the next step, this step isn’t really needed but included to emphasize the importance of pressing “Ctrl+L” to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at <http://www.national.com/timing/software/> for more information on Port Setup. Appendix H: Troubleshooting Information contains information on troubleshooting communications.

4. Restoring a Default Mode

Click “Mode” → “LMK03806B, 20 MHz Crystal”; then press Ctrl+L.



Figure 5: Setting the Default mode for LMK03806

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.

PLL Loop Filters and Loop Parameters

The default loop filter for the PLL has been configured for a 60 kHz bandwidth. The following table contains the parameters for the PLL.

TI's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: <http://www.national.com/timing/software/>.

PLL Loop Filter

Table 2: PLL Loop Filter Parameters for LMK03806B

Integrated VCO PLL		
	LMK03806B	
C1_LF	0.022	nF
C2_LF	1.8	nF
C3 (internal)	0.01	nF
C4 (internal)	0.01	nF
R2_A2	0.82	k Ω
R3 (internal)	0.2	k Ω
R4 (internal)	0.2	k Ω
Charge Pump Current, $K\phi$	3.2	mA
Phase Detector Frequency	20	MHz
Frequency	2500	MHz
K_{vco}	19	MHz/V
N	25	
P	5	
Phase Margin	75	degrees
Loop Bandwidth	63	kHz

Note: PLL Loop Bandwidth is a function of $K\phi$, K_{vco} , N as well as loop components. Changing $K\phi$ and N will change the loop bandwidth.

Evaluation Board Inputs and Outputs

The following table contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable CodeLoader programming controls are noted for convenience. Refer to the [LMK03806B Datasheet](#) for complete register programming information.

Table 3: Evaluation Board Inputs and Outputs

Connector Name	Signal Type, Input/Output	Description																										
<p><u>SMA's Populated:</u> CLKout0, CLKout0*, CLKout2, CLKout2*, CLKout4, CLKout4*, CLKout6, CLKout6*, CLKout8, CLKout8*, CLKout10, CLKout10*</p> <p><u>SMA's Not Populated:</u> CLKout1, CLKout1*, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout7, CLKout7*, CLKout9, CLKout9*, CLKout11, CLKout11*</p>	<p>Analog, Output</p>	<p>Clock outputs with programmable output buffers.</p> <p>The output terminations by default on the evaluation board are shown below, and the output type selected by default in CodeLoader is indicated by an asterisk (*):</p> <table border="1" data-bbox="784 808 1442 1335"> <thead> <tr> <th data-bbox="784 808 1065 877">Clock output pair</th> <th data-bbox="1065 808 1442 877">Default Board Termination</th> </tr> </thead> <tbody> <tr> <td data-bbox="784 877 1065 915">CLKout0</td> <td data-bbox="1065 877 1442 915">LVPECL*</td> </tr> <tr> <td data-bbox="784 915 1065 953">CLKout1</td> <td data-bbox="1065 915 1442 953">LVPECL</td> </tr> <tr> <td data-bbox="784 953 1065 991">CLKout2</td> <td data-bbox="1065 953 1442 991">LVPECL*</td> </tr> <tr> <td data-bbox="784 991 1065 1029">CLKout3</td> <td data-bbox="1065 991 1442 1029">LVPECL</td> </tr> <tr> <td data-bbox="784 1029 1065 1066">CLKout4</td> <td data-bbox="1065 1029 1442 1066">LVDS* / LVCMOS</td> </tr> <tr> <td data-bbox="784 1066 1065 1104">CLKout5</td> <td data-bbox="1065 1066 1442 1104">LVDS / LVCMOS</td> </tr> <tr> <td data-bbox="784 1104 1065 1142">CLKout6</td> <td data-bbox="1065 1104 1442 1142">LVDS* / LVCMOS</td> </tr> <tr> <td data-bbox="784 1142 1065 1180">CLKout7</td> <td data-bbox="1065 1142 1442 1180">LVDS / LVCMOS</td> </tr> <tr> <td data-bbox="784 1180 1065 1218">CLKout8</td> <td data-bbox="1065 1180 1442 1218">LVDS* / LVCMOS</td> </tr> <tr> <td data-bbox="784 1218 1065 1255">CLKout9</td> <td data-bbox="1065 1218 1442 1255">LVDS / LVCMOS</td> </tr> <tr> <td data-bbox="784 1255 1065 1293">CLKout10</td> <td data-bbox="1065 1255 1442 1293">LVPECL*</td> </tr> <tr> <td data-bbox="784 1293 1065 1335">CLKout11</td> <td data-bbox="1065 1293 1442 1335">LVPECL</td> </tr> </tbody> </table> <p>Each CLKout pair has a programmable LVDS, LVPECL, or LVCMOS buffer. The output buffer type can be selected in CodeLoader in the Clock Outputs tab via the CLKoutX_TYPE control.</p> <p>All clock outputs are AC-coupled to allow safe testing with RF test equipment.</p> <p>All LVPECL clock outputs are source-terminated using 240-ohm resistors.</p> <p>If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state).</p>	Clock output pair	Default Board Termination	CLKout0	LVPECL*	CLKout1	LVPECL	CLKout2	LVPECL*	CLKout3	LVPECL	CLKout4	LVDS* / LVCMOS	CLKout5	LVDS / LVCMOS	CLKout6	LVDS* / LVCMOS	CLKout7	LVDS / LVCMOS	CLKout8	LVDS* / LVCMOS	CLKout9	LVDS / LVCMOS	CLKout10	LVPECL*	CLKout11	LVPECL
Clock output pair	Default Board Termination																											
CLKout0	LVPECL*																											
CLKout1	LVPECL																											
CLKout2	LVPECL*																											
CLKout3	LVPECL																											
CLKout4	LVDS* / LVCMOS																											
CLKout5	LVDS / LVCMOS																											
CLKout6	LVDS* / LVCMOS																											
CLKout7	LVDS / LVCMOS																											
CLKout8	LVDS* / LVCMOS																											
CLKout9	LVDS / LVCMOS																											
CLKout10	LVPECL*																											
CLKout11	LVPECL																											

Connector Name	Signal Type, Input/Output	Description						
<p>OSCCout0, OSCout0*, OSCout1, OSCout1*</p>	<p>Analog, Output</p>	<p>Buffered outputs of OSCin port.</p> <p>The output terminations on the evaluation board are shown below, the output type selected by default in CodeLoader is indicated by an asterisk (*):</p> <table border="1" data-bbox="784 449 1442 600"> <thead> <tr> <th data-bbox="784 449 1065 520">OSC output pair</th> <th data-bbox="1065 449 1442 520">Default Board Termination</th> </tr> </thead> <tbody> <tr> <td data-bbox="784 520 1065 562">OSCCout0</td> <td data-bbox="1065 520 1442 562">LVPECL* (fixed)</td> </tr> <tr> <td data-bbox="784 562 1065 600">OSCCout1</td> <td data-bbox="1065 562 1442 600">LVPECL* (fixed)</td> </tr> </tbody> </table> <p>Only OSCout0 has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout0 buffer type can be selected in CodeLoader on the Clock Outputs tab via the OSCout0_TYPE control. OSCout1 has LVPECL buffer only but has programmable swing amplitude.</p> <p>Both OSCout pairs are AC-coupled to allow safe testing with RF test equipment.</p> <p>The OSCout0 and OSCout1 outputs are source-terminated using 240-ohm resistors.</p> <p>If OSCout0 is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state).</p>	OSC output pair	Default Board Termination	OSCCout0	LVPECL* (fixed)	OSCCout1	LVPECL* (fixed)
OSC output pair	Default Board Termination							
OSCCout0	LVPECL* (fixed)							
OSCCout1	LVPECL* (fixed)							
<p>Vcc</p>	<p>Power, Input</p>	<p>Main power supply input for the evaluation board.</p> <p>A 3.9 V DC power source applied to this SMA will, by default, source the onboard LDO regulators that power the inner layer planes that supply the LMK03806B.</p> <p>The LMK03806B contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.</p> <p>On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See schematics for more details.</p>						

Connector Name	Signal Type, Input/Output	Description
J1	Power, Input	<p>Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND).</p> <p>Apply power to either Vcc SMA or J1, but not both.</p>
OSCin, OSCin*	Analog, Input	<p>By default, these SMAs are not connected to the traces going to the OSCin/OSCin* pins of the LMK03806B. Instead, the onboard crystal drives the OSCin input of the device.</p> <p>A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF.</p> <p>Refer to the LMK03806 Datasheet section “Electrical Characteristics” for PLL Reference Input (OSCin) specifications.</p>
uWire	CMOS, Input/Output	<p>10-pin header for uWire programming interface and programmable logic I/O pins for the LMK03806B.</p> <p>The uWire interface includes CLKuWire, DATAuWire, and LEuWire signals.</p> <p>The programmable logic I/O signals accessible through this header include: SYNC. SYNC also has a dedicated SMA and test point.</p>

Connector Name	Signal Type, Input/Output	Description
<p style="text-align: center;">SYNC</p>	<p style="text-align: center;">CMOS, Input/Output</p>	<p>Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC.</p> <p>In the default CodeLoader mode, SYNC will asserted when the SYNC pin is low and the outputs to be synchronized will be held in a logic low state. When SYNC is unasserted, the clock outputs to be synchronized are activated and will be initially phase aligned with each other except for outputs programmed with different digital delay values.</p> <p>A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the Bits/Pins tab in CodeLoader.</p> <p>Refer to the LMK03806 Datasheet section “Clock Output Synchronization” for more information.</p>

Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50 ohm inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it's recommended to use phase-matched, 50-ohm cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

Appendix A: CodeLoader Usage

Code Loader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the optional USB-to-uWire cable available from <http://store.national.com/>. The part number is USB2UWIRE-IFACE.

Port Setup Tab

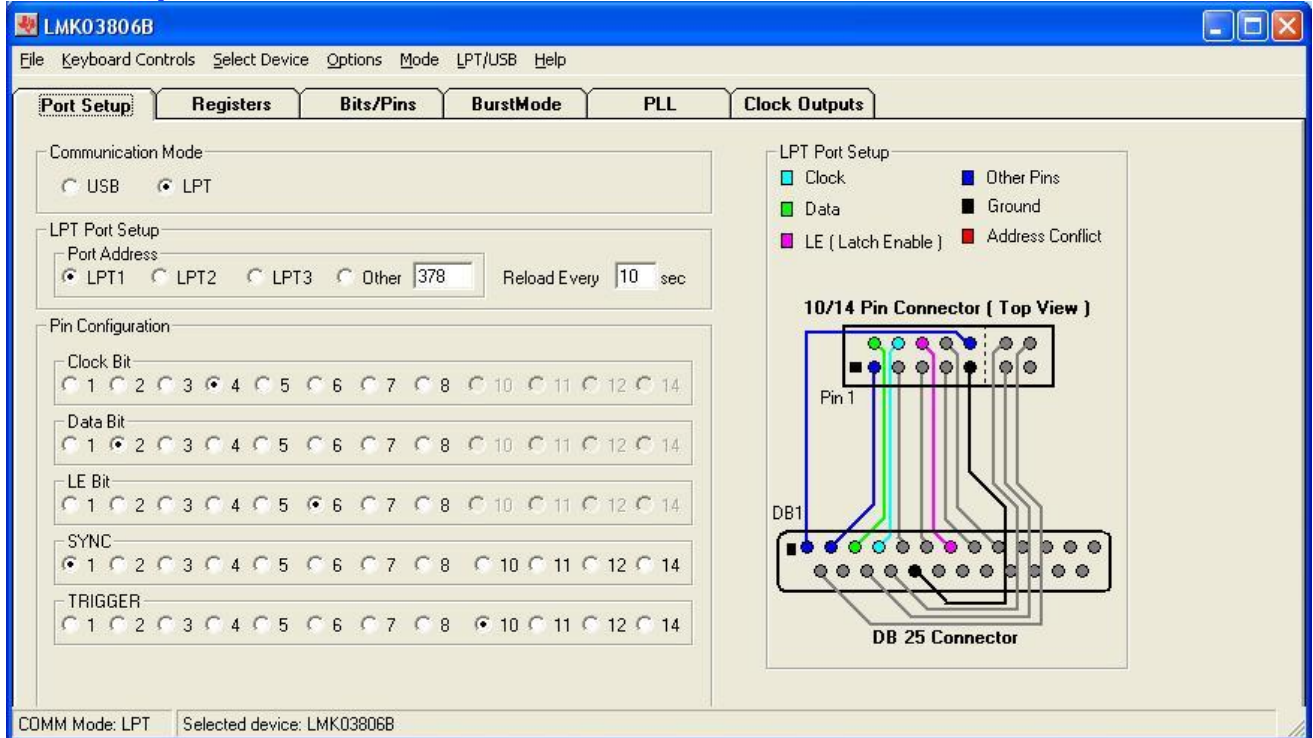


Figure 8: Port Setup tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally **does not** need to be changed by the user. Figure 8 shows the default settings.

Clock Outputs Tab

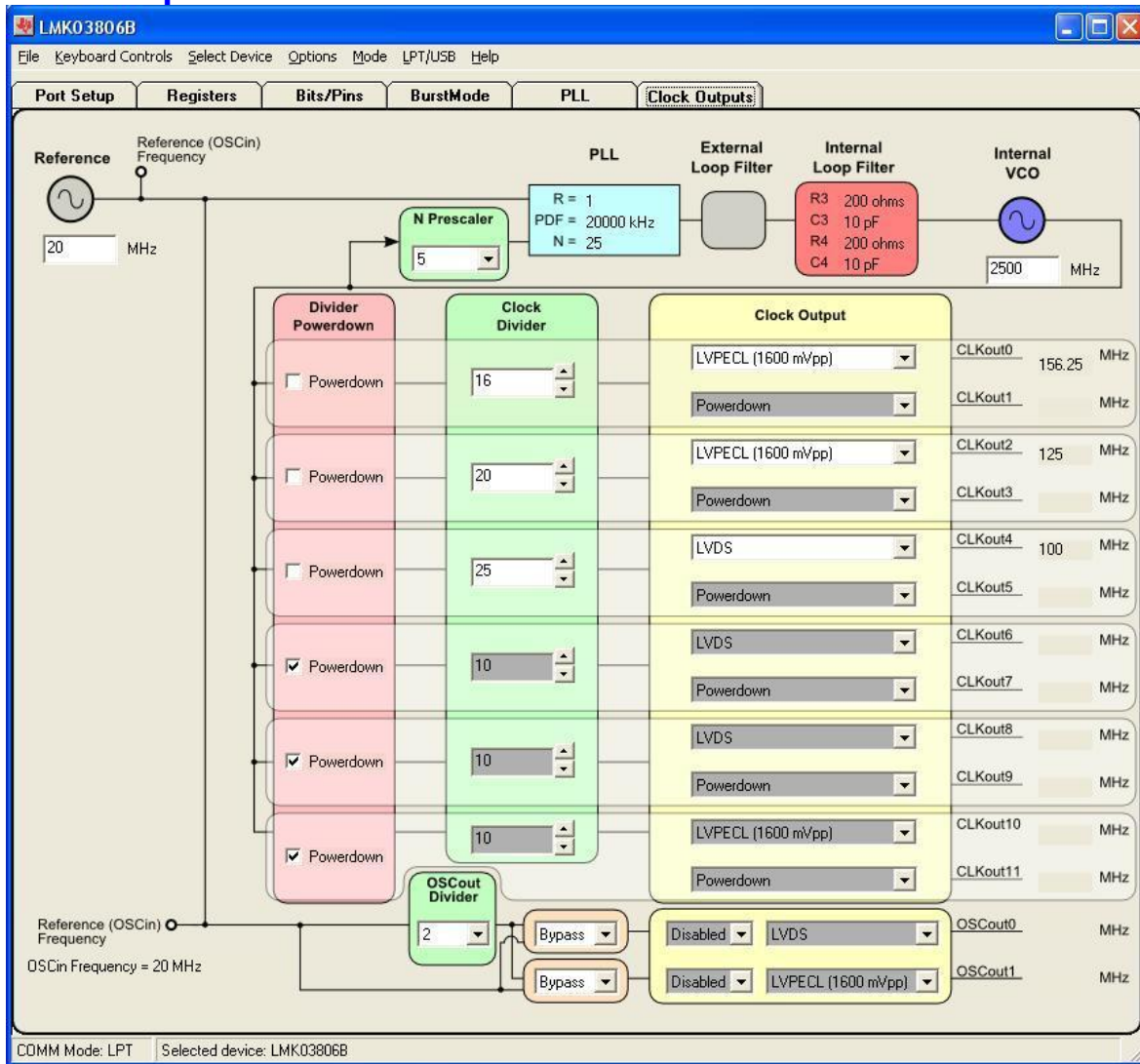


Figure 9: Clock Outputs tab

The **Clock Outputs** tab allows the user to control the output channel blocks, including:

- Clock Group Source from either Crystal or OSCIn
- Channel Powerdown (affects clock divider, and buffer blocks)
- Clock Divide value
- Clock Output format (per output)

Clicking on the cyan-colored PLL block that contains R, PDF and N values will bring the **PLL** tab into focus where these values may be modified, if needed.

Clicking on the values in the box containing the Internal Loop Filter component (R3, C3, R4, C4) allow one to step through the possible values. Left click to increase the component value, and right click to decrease the value. These values can also be changed in the **Bits/Pins** tab.

The Reference Oscillator value field may be changed in either the **Clock Outputs** tab or the **PLL** tab. The PLL Reference frequency should match the frequency of the onboard Crystal.

PLL Tab

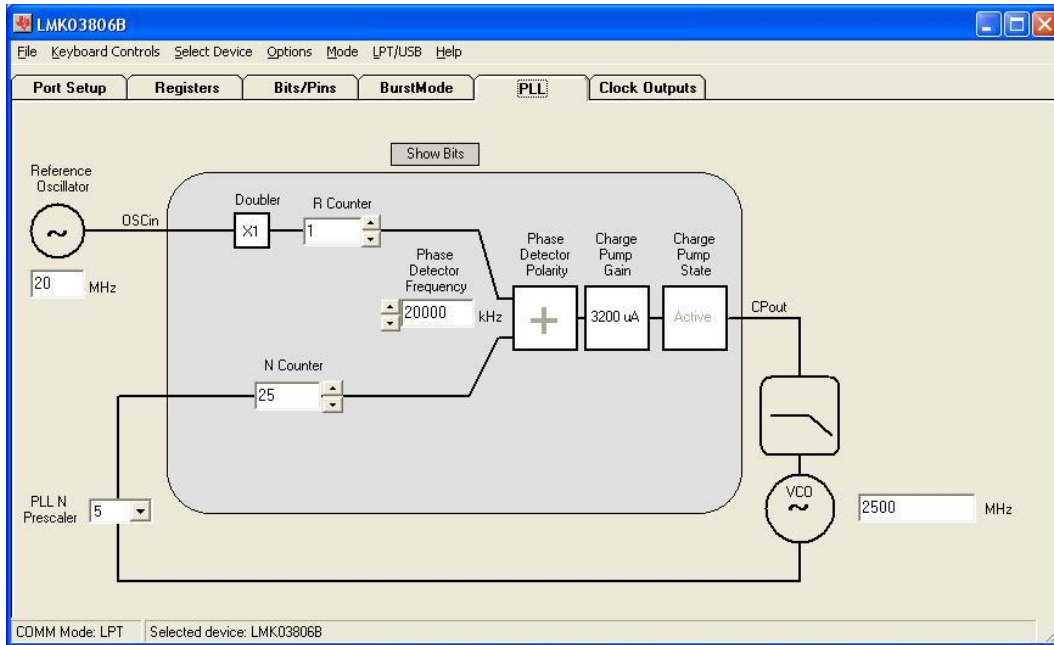


Figure 10: PLL tab

The PLL tab allows the user to change the following parameters in Table 4.

Table 4: Registers Controls and Descriptions in PLL tab

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	OSCin_FREQ	OSCin frequency from the External OSCin connector or Crystal.
Phase Detector Frequency (MHz)	n/s	PLL Phase Detector Frequency (PDF). This value is calculated as: $PLL\ PDF = OSCin\ Frequency * (2^{EN_PLL_REF_2X}) / (PLL_R)$.
VCO Frequency (MHz)	n/a	Internal VCO Frequency should be within the allowable range of the LMK03806B device. This value is calculated as: $VCO\ Frequency = PLL\ PDF * (PLL_N * PLL_P)$.
Doubler	EN_PLL_REF_2X	PLL Doubler. 0 = Bypass Doubler 1 = Enable Doubler
R Counter	PLL_R	PLL R Counter value (1 to 4095).
N Counter	PLL_N	PLL N Counter value (1 to 49140).
OScout Divider	PLL_P	PLL N Prescaler value (2 to 8).

Phase Detector Polarity	PLL_CP_POL	PLL Phase Detector Polarity. Click on the polarity sign to toggle polarity “+” or “-”.
Charge Pump Gain	PLL_CP_GAIN	PLL Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (100, 400, 1600, 3200 uA).
Charge Pump State	PLL_CP_TRI	PLL Charge Pump State. Click to toggle between Active and Tri-State.

Changes made on this tab will be reflected in the **Clock Outputs** tab. The VCO Frequency should conform to the specified internal VCO frequency range for the LMK03806B device (per **Error! Reference source not found.**).

Bits/Pins Tab

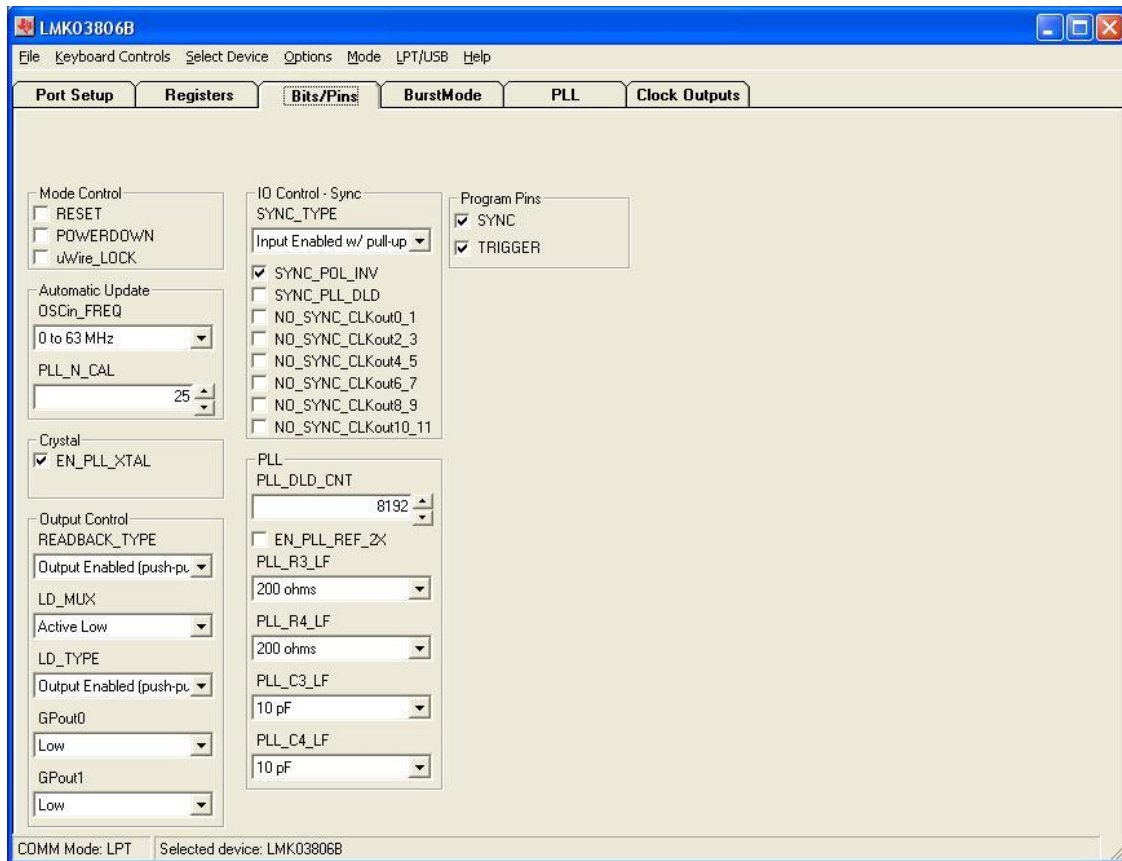


Figure 11: Bits/Pins tab

The **Bits/Pins** tab allows the user to program bits directly, many of which are not available on other tabs. Brief descriptions for the controls on this tab are provided in Table 5 to supplement the datasheet. Refer to the [LMK03806 Datasheet](#) for more information.

TIP: Right-clicking any register name in the **Bits/Pins** tab will display a Help prompt with the register address, data bit location/length, and a brief register description.

Table 5: Register Controls and Descriptions on Bits/Pins tab

Group	Register Name	Description
Mode Control	RESET	Resets the device to default register values. RESET must be cleared for normal operation to prevent an unintended reset every time R0 is programmed.
	POWERDOWN	Places the device in powerdown mode.
	uWire_LOCK	When checked, no other uWire programming will have effect. Must be unchecked to enable uWire programming of registers R0 to R30.
Crystal	EN_PLL_XTAL	Enables Crystal Oscillator
	XTAL_LVL	Sets peak amplitude on the tunable crystal. Values listed are for a 20 MHz crystal.
Output Control	Status0_MUX	Sets the selected signal on the Status0 pin.
	Status0_TYPE	Sets I/O pin type on the Status0 pin.
	Status1_MUX	Sets the selected signal on the Status1 pin.
	Status1_TYPE	Sets I/O pin type on the Status1 pin.
	GPO0	Sets logic level on the GPO0 pin.
	GPO1	Sets logic level on the GPO1 pin.
IO Control – Sync	SYNC_MUX	Sets the selected signal on the SYNC pin.
	SYNC_TYPE	Sets I/O pin type on the SYNC pin.
	SYNC_POL_INV	Sets polarity on SYNC input to active low when checked. Toggling this bit will initiate a SYNC event.
	SYNC_PLL_DLD	Engage SYNC mode until PLL DLD is true
	NO_SYNC_CLKoutX_Y	Synchronization will not affect selected clock outputs, where X = even-numbered output and Y = odd-numbered output.
	EN_SYNC	Must be set when using SYNC, but may be cleared after the SYNC event. When using dynamic digital delay (SYNC_QUAL = 1), EN_SYNC must always be set. Changing this value from 0 to 1 can cause a SYNC event, so clocks which should not be SYNCed when setting this bit should have the NO_SYNC_CLKoutX_Y bit set. NOTE: This bit is not a valid method of generating a SYNC event. Use one of the other SYNC generation methods to ensure a proper SYNC occurs.
PLL	PLL_WND_SIZE	If the phase error between the PLL reference and feedback clock is less than specified time, then the PLL lock counter increments.

	PLL_DLD_CNT	The reference and feedback of PLL must be within the window of phase error as specified by PLL_WND_SIZE for this many cycles before PLL digital lock detect is asserted.
	EN_PLL_REF_2X	Enables the doubler block to doubles the reference frequency into the PLL R counter. This can allow for frequency of 2/3, 2/5, etc. of OSCin to be used at the phase detector of PLL.
	PLL_R3_LF	Set the corresponding integrated PLL loop filter values: R3, R4, C3, and C4. It is also possible to set these values by clicking on the loop filter values on the Clock Outputs tab.
	PLL_R4_LF	
	PLL_C3_LF	
PLL_C4_LF		
Program Pins	SYNC	Sets these pins on the uWire header to logic high (checked) or logic low (unchecked).
	TRIGGER	

Registers Tab

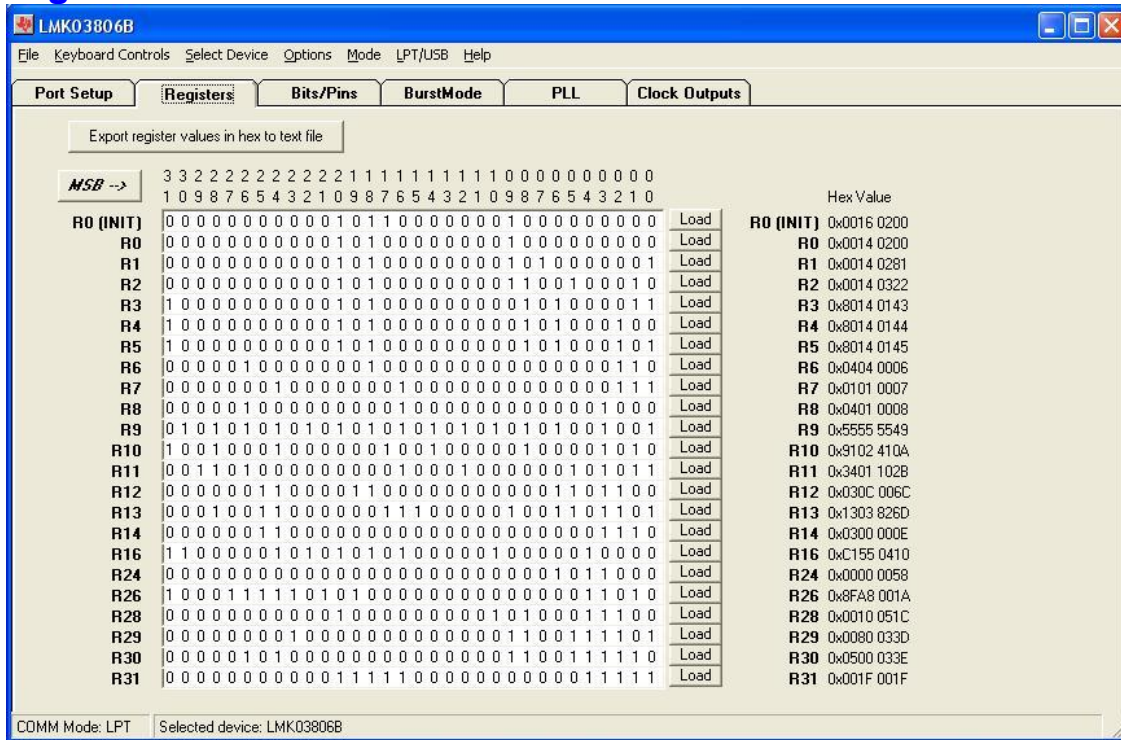


Figure 12: Registers Tab

The Registers tab shows the value of each register. This is convenient for programming the device to the desired settings, then exporting to a text file the register values in hexadecimal for use in your own application.

By clicking in the “bit field” it is possible to manually change the value of registers by typing ‘1’ and ‘0.’

Appendix B: Typical Phase Noise Performance Plots

PLL

VCO Clock Output Phase Noise

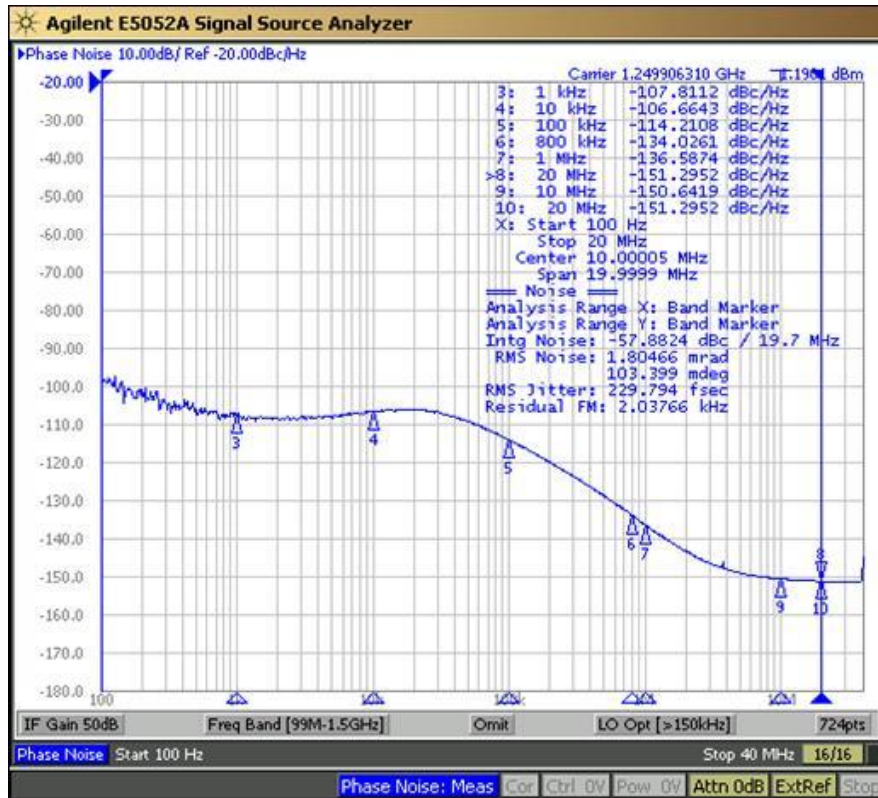


Figure 13: LMK03806B PLL VCO div2 LVPECL Phase Noise

Table 6: LMK03806B PLL VCO div2 Phase Noise and RMS Jitter (fs)

Offset	Phase Noise (dBc/Hz)
100 Hz	-98.3
1 kHz	-107.8
10 kHz	-106.6
100 kHz	-114.2
1 MHz	-136.6
10 MHz	-150.6
20 MHz	-151.3
RMS Jitter (fs) 12 kHz to 20 MHz	215
RMS Jitter (fs) 100 Hz to 20 MHz	229

Clock Outputs (CLKout)

The LMK03806 Family features programmable LVDS, LVPECL, and LVC MOS buffer modes for the CLKoutX and OSCout0 output pairs. The OSCout1 output pair has a LVPECL buffer. Included below are various phase noise measurements for each output format.

CLKout Phase Noise (div12 and div24)

For the LMK03806B, the internal VCO frequency is 2500 MHz. The divide-by-8 CLKout frequency is 312.5 MHz, and the divide-by-16 CLKout frequency is 156.25 MHz.

Table 7: LMK03806B Phase Noise and RMS Jitter for Different CLKout Output Formats and Frequencies

Offset	div8 LVPECL	div8 LVDS	div8 LVC MOS	div16 LVPECL	div16 LVDS	div16 LVC MOS
100 Hz	-110.4	-107.6	-108.9	-114.9	-116.6	-114.9
1 kHz	-120.2	-120.2	-120.5	-125.5	-127.0	-125.2
10 kHz	-119.3	-119.3	-119.1	-125.5	-125.2	-125.3
100 kHz	-126.6	-126.6	-126.4	-132.7	-132.5	-132.5
1 MHz	-148.5	-147.8	-148.3	-154.1	-152.7	-153.8
10 MHz	-157.1	-154.2	-156.2	-160.3	-156.5	-159.6
20 MHz	-157.8	-154.3	-156.3	-159.0	-156.5	-159.9
RMS Jitter (fs) 12 kHz to 20 MHz	206	213	211	207	229	227
RMS Jitter (fs) 100 Hz to 20 MHz	223	229	227	225	241	232

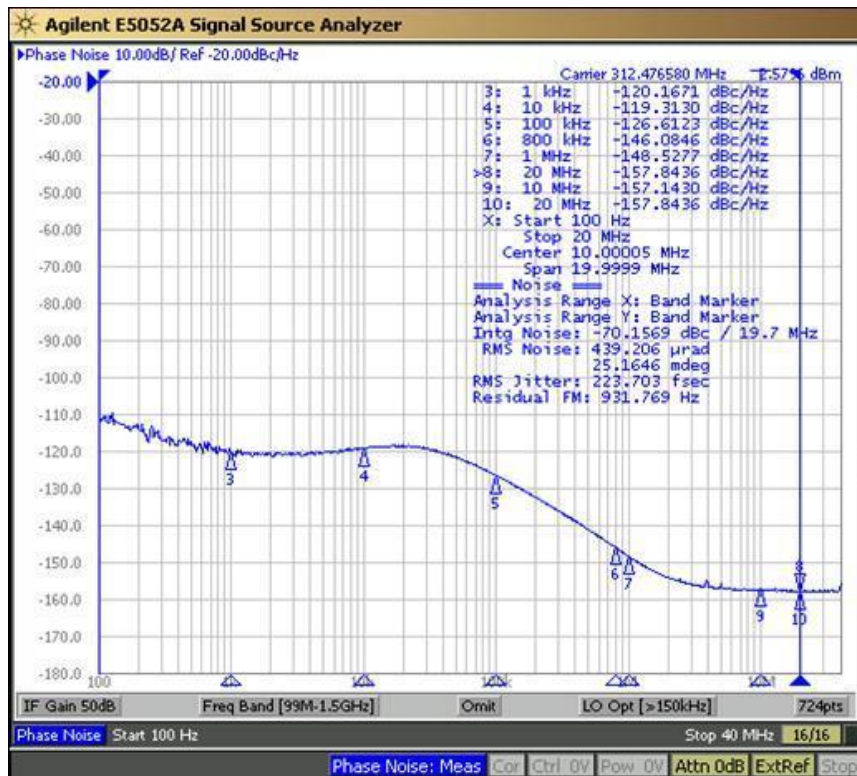


Figure 14: LMK03806B div8 CLKout LVPECL Phase Noise

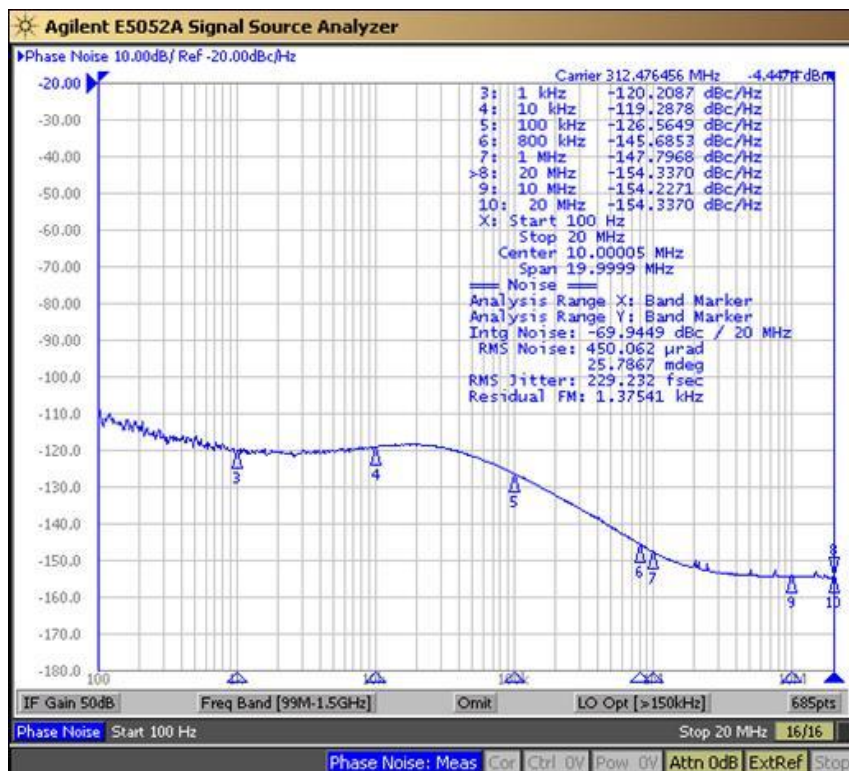


Figure 15: LMK03806B div8 CLKout LVDS Phase Noise

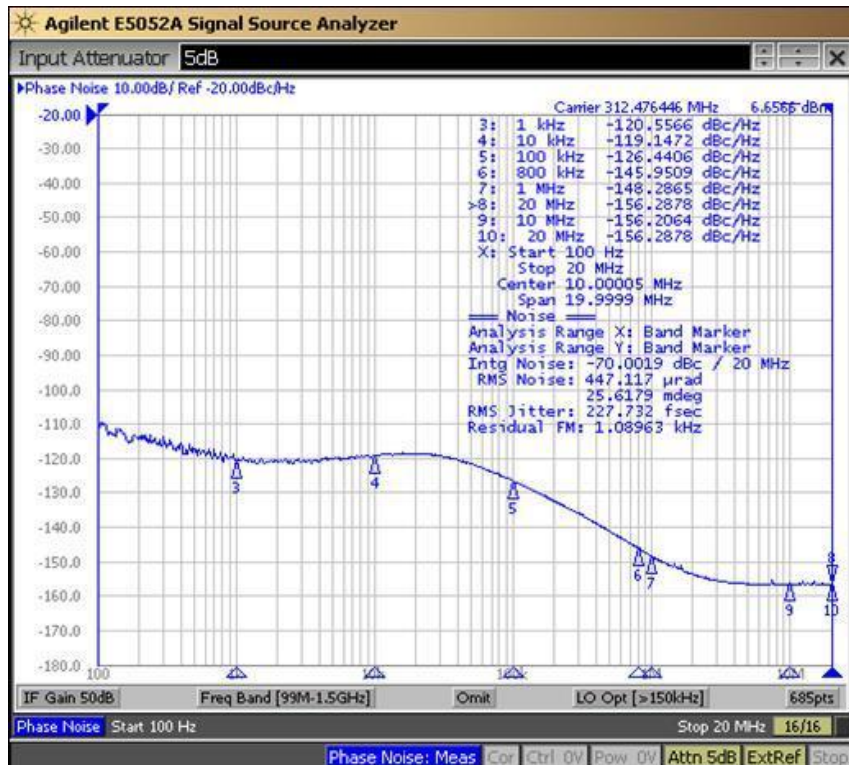


Figure 16: LMK03806B div8 CLKout LVCMOS Phase Noise

Appendix C: Schematics

Power Supplies

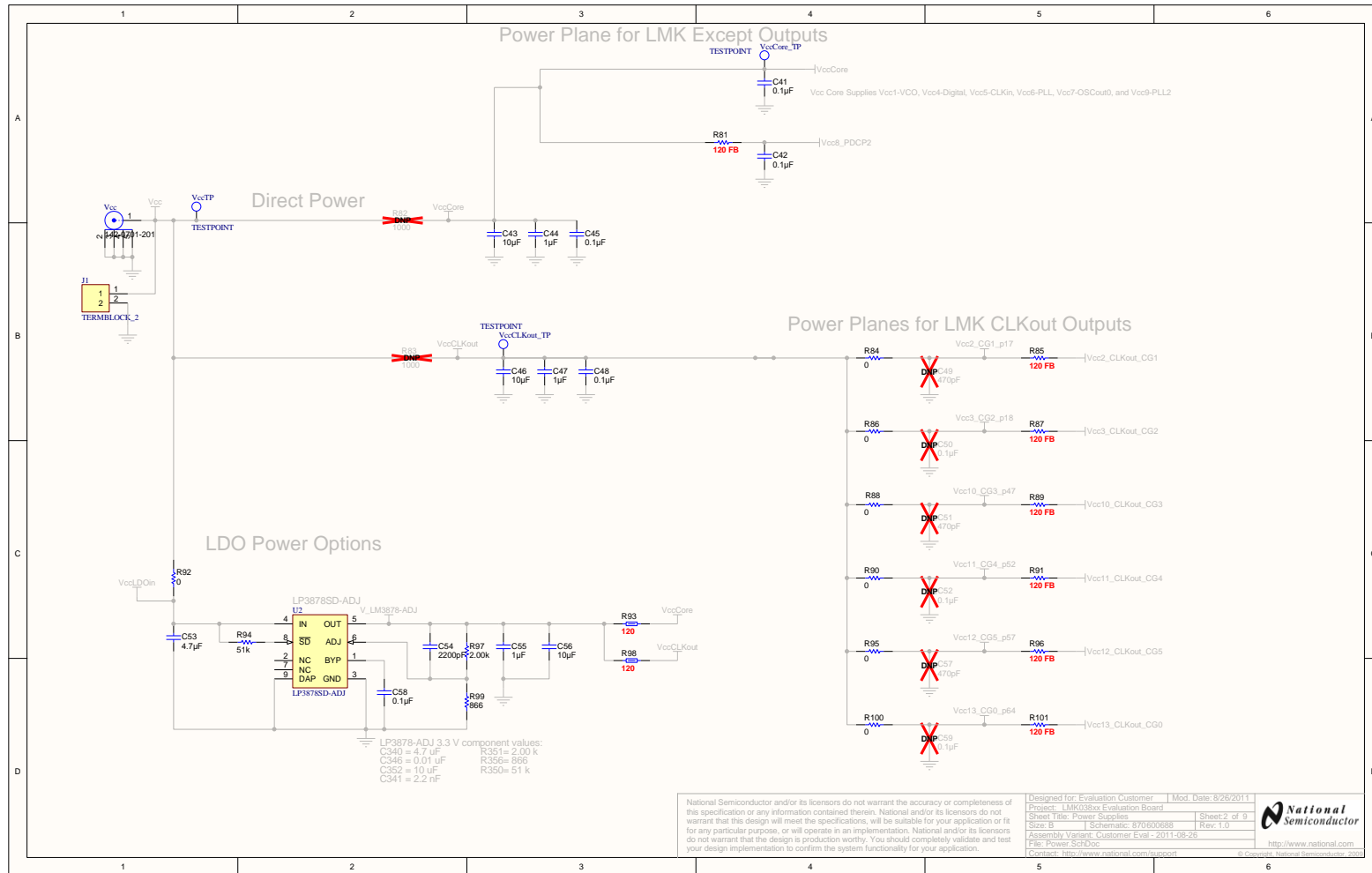


Figure 17 - LMK03806 Power Supply Schematic

LMK03806B Device with Loop Filter and Crystal Circuits

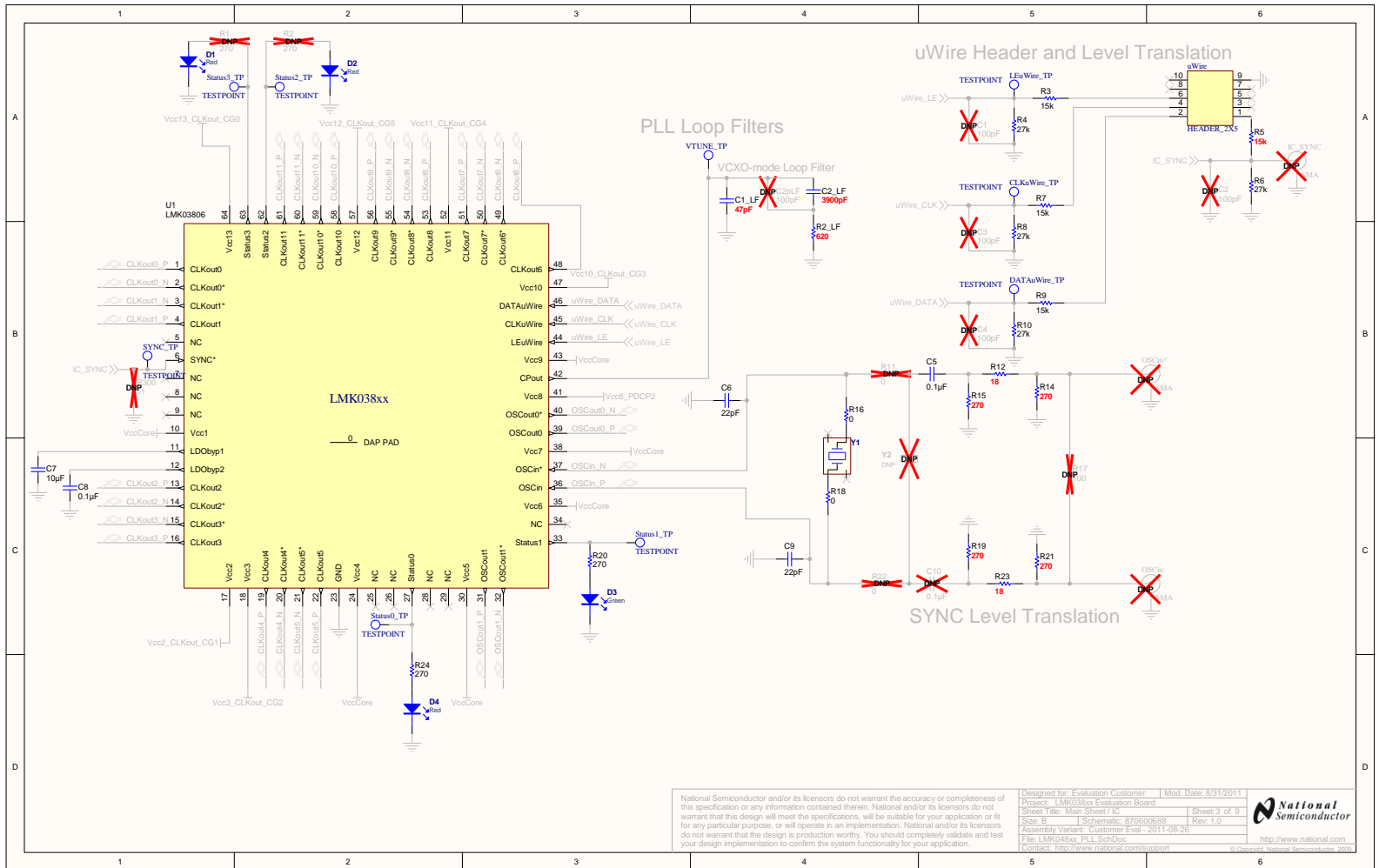


Figure 18 - LMK03806 Device Schematic

Outputs, (OSCont0/1, CLKout0/1/2/3)

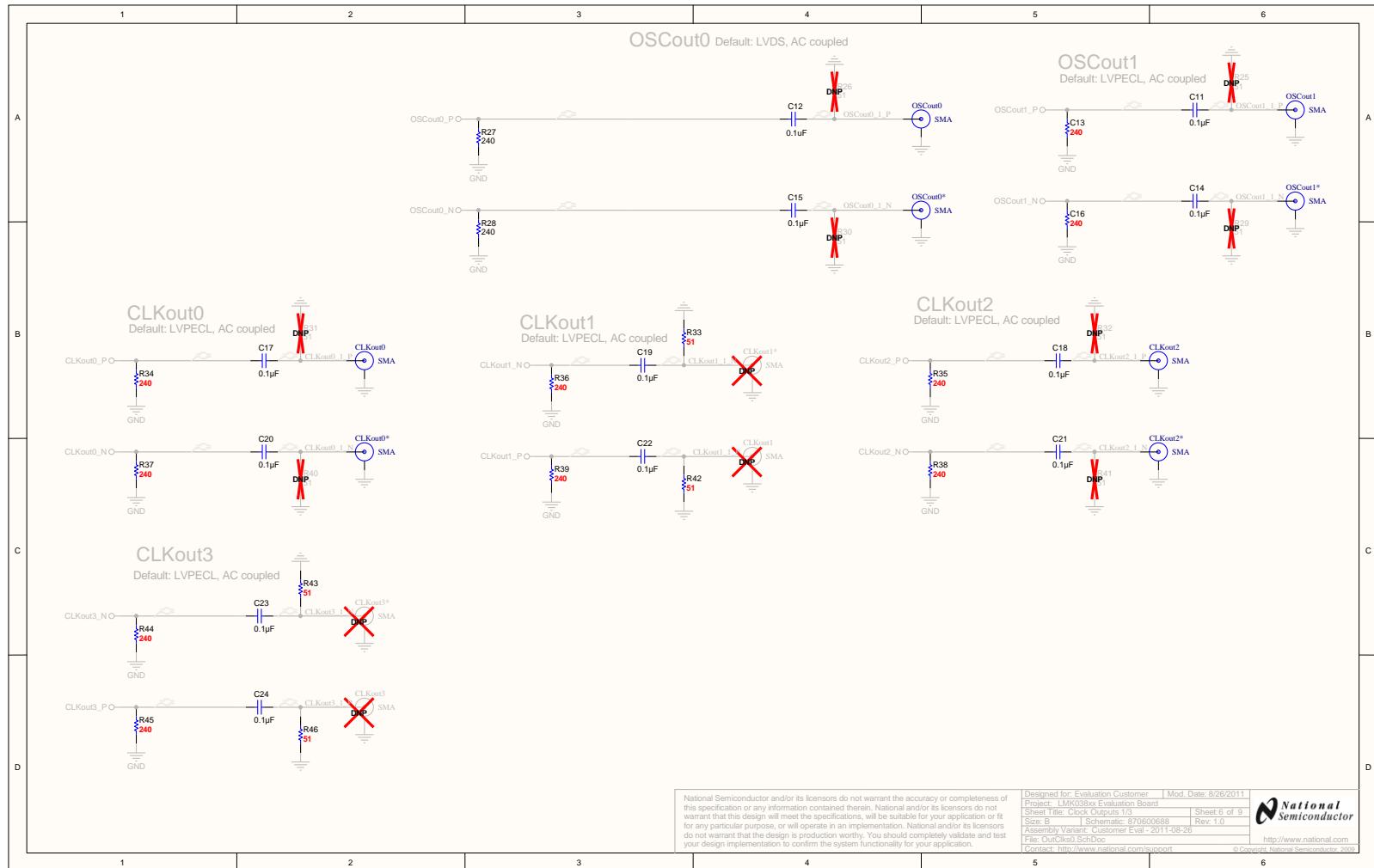


Figure 19 - Outputs, (OSCont, CLKout0/1/2/3) Schematics

Clock Outputs (CLKout 4/5/6/7)

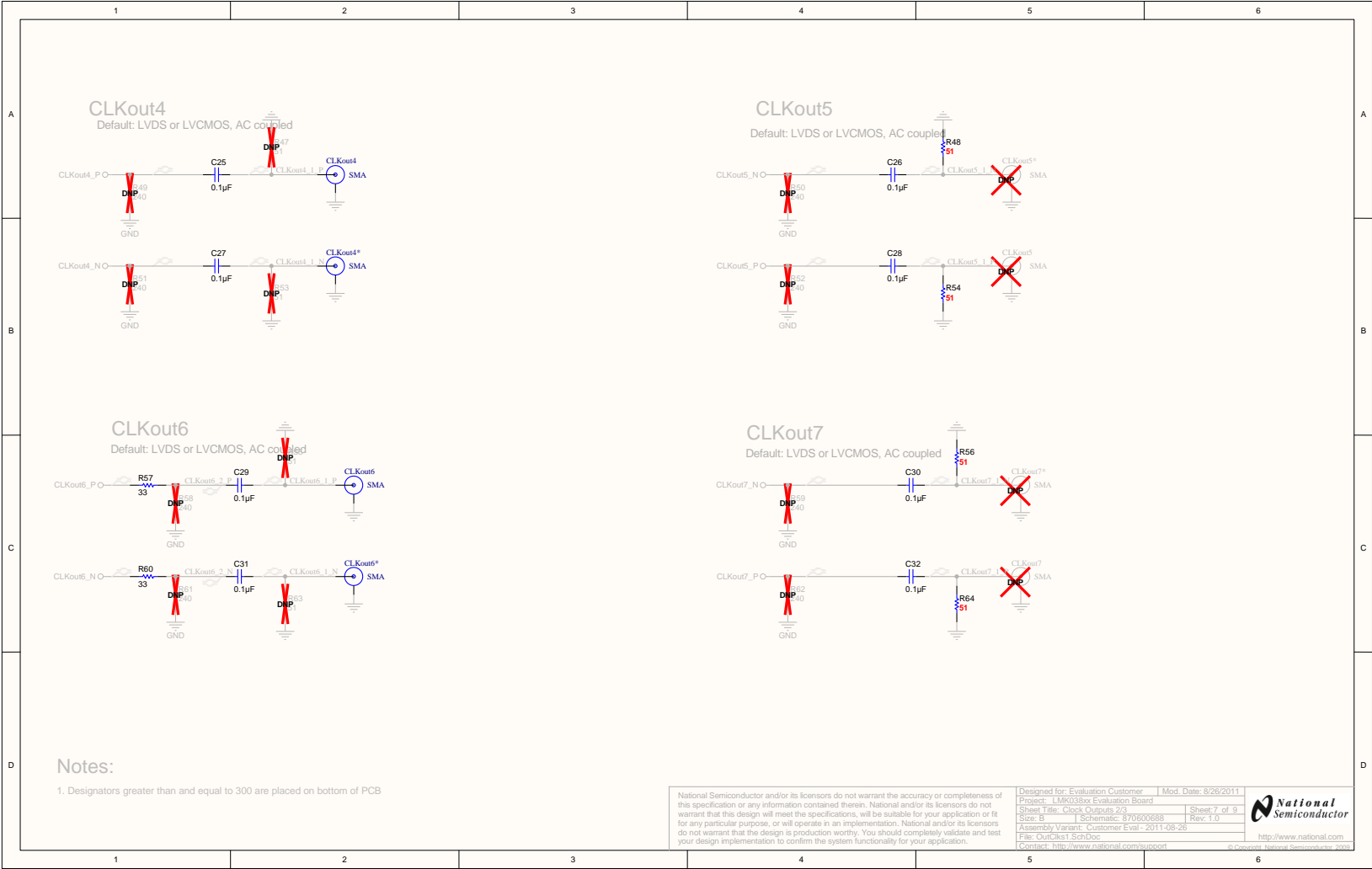


Figure 20 - LMK03806 Clock Outputs 4 through 7 Schematics

Clock Outputs (CLKout8/9/10/11)

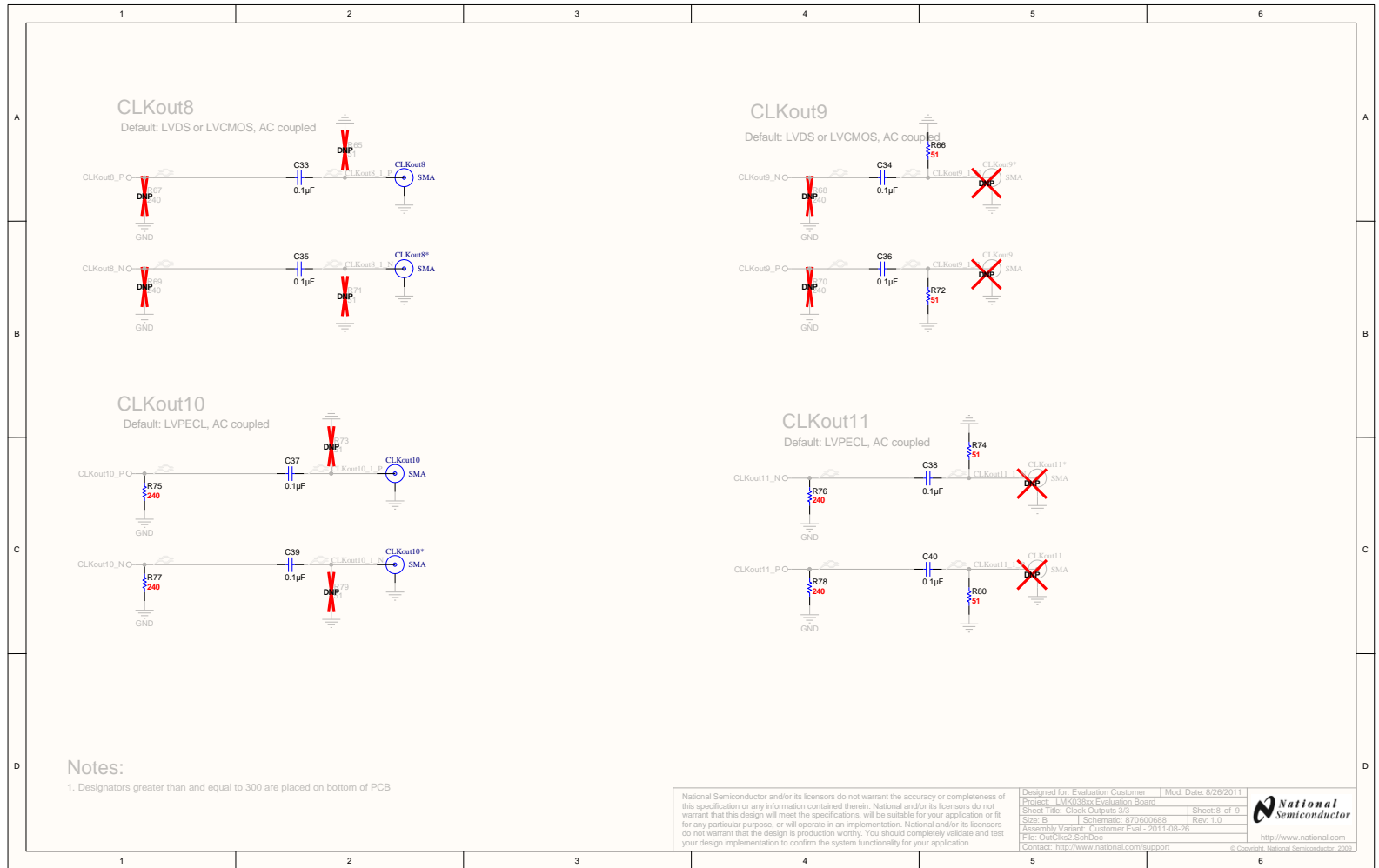


Figure 21 - LMK03806 Clock Outputs 8 through 11 Schematics

Appendix D: Bill of Materials

Table 8: Bill of Materials for LMK03806 Evaluation Boards

Item	Designator	Description	RoHS	Manufacturer	PartNumber	Quantity	Required
1	C1_LF	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	Y	Kemet	C0603C470J5GACTU	1	30
2	C2_LF	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0603	Y	MuRata	GRM188R71H392KA01D	1	30
3	C5, C8, C12, C15, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C45, C48	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Y	Kemet	C0603C104J3RACTU	31	930
4	C6, C9	CAP, CERM, 22pF, 50V, +/-5%, C0G/NP0, 0603	Y	AVX	06035A220JAT2A	2	60
5	C7, C43, C46, C56	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	Y	Kemet	C0805C106K8PACTU	4	120
6	C11, C14, R16, R18, R84, R86, R88, R90, R95, R100	RES, 0 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW06030000Z0EA	10	300
7	C13, C16, R27, R28, R34, R35, R36, R37, R38, R39, R44, R45, R75, R76, R77, R78	RES, 240 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603240RJNEA	16	480
8	C31	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Y	Kemet	C0603C104K3RACTU	1	30
9	C44, C47, C55	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	Y	Kemet	C0603C105K8PACTU	3	90
10	C53	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	Y	Kemet	C0603C475K8PACTU	1	30
11	C54	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Y	Kemet	C0603C222K5RACTU	1	30

12	C58	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Y	Kemet	C0603C104K4RACTU	1	30
13	CLKout0, CLKout0*, CLKout2, CLKout2*, CLKout4, CLKout4*, CLKout6, CLKout6*, CLKout8, CLKout8*, CLKout10, CLKout10*, OScout0, OScout0*, OScout1, OScout1*	Connector, SMT, End launch SMA 50 Ohm	Y	Emerson Network Power	142-0701-851	16	480
14	D1, D2, D4	LED 2.8X3.2MM 565NM RED CLR SMD	Y	Lumex Opto/Components Inc.	SML-LX2832IC	3	90
15	D3	LED 2.8X3.2MM 565NM GRN CLR SMD	Y	Lumex Opto/Components Inc.	SML-LX2832GC	1	30
16	J1	CONN TERM BLK PCB 5.08MM 2POS OR	Y	Weidmuller	1594540000	1	30
17	R2_LF	RES, 620 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603620RJNEA	1	30
18	R3, R5, R7, R9	RES, 15k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060315K0JNEA	4	120
19	R4, R6, R8, R10	RES, 27k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060327K0JNEA	4	120
20	R12, R23	RES, 18 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060318R0JNEA	2	60
21	R14, R15, R19, R20, R21, R24	RES, 270 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603270RJNEA	6	180
22	R33, R42, R43, R46, R48, R54, R56, R64, R66, R72, R74, R80	RES, 51 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060351R0JNEA	12	360
23	R57, R60	RES, 33 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060333R0JNEA	2	60
24	R81, R85, R87, R89, R91, R93, R96, R98, R101	FB, 120 ohm, 500 mA, 0603	Y	Murata	BLM18AG121SN1D	9	270

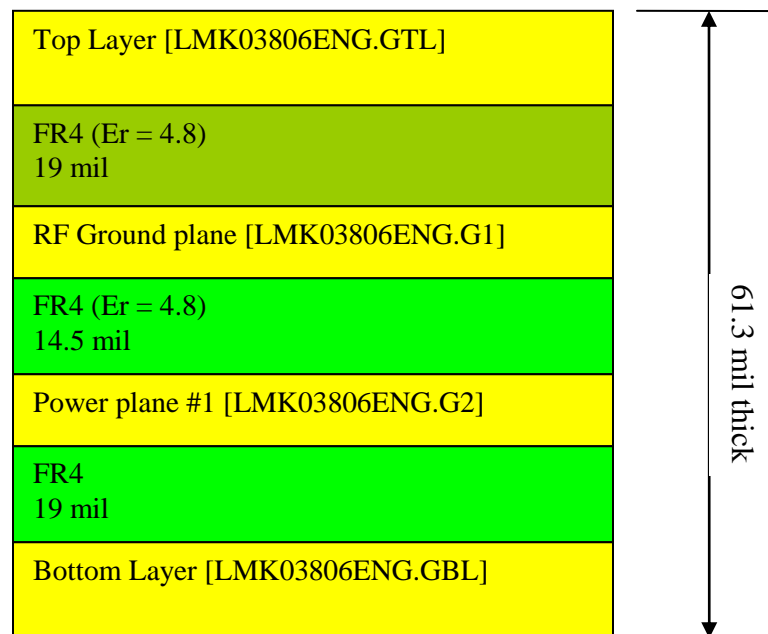
25	R92	RES, 0 ohm, 5%, 0.125W, 0805	Y	Vishay-Dale	CRCW08050000Z0EA	1	30
26	R94	RES, 51k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060351K0JNEA	1	30
27	R97	RES, 2.00k ohm, 1%, 0.1W, 0603	Y	Vishay-Dale	CRCW06032K00FKEA	1	30
28	R99	RES, 866 ohm, 1%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603866RFKEA	1	30
29	S1, S2, S3, S4, S5, S6	0.875" Standoff	Y	VOLTREX	SPCS-14	6	180
30	U1	LMK03806		Texas Instruments	LMK03806BISQ	1	30
31	U2	Micropower 800mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications	Y	Texas Instruments	LP3878SD-ADJ	1	30
32	uWire	Low Profile Vertical Header 2x5 0.100"	Y	FCI	52601-G10-8LF	1	30
33	Vcc	Connector, TH, SMA	Y	Emerson Network Power	142-0701-201	1	30
34	Y1		Y	Used in BOM report	Used in BOM report	1	30
35	C1, C2, C2pLF, C3, C4	CAP, CERM, 100pF, 50V, +/-5%, COG/NP0, 0603	Y	Kemet	C0603C101J5GACTU	0	0
36	C10	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Y	Kemet	C0603C104J3RACTU	0	0
37	C49, C50, C51, C52, C57, C59	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Y	Kemet	C0603C104K3RACTU	0	0
38	CLKout1, CLKout1*, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout7, CLKout7*, CLKout9, CLKout9*, CLKout11, CLKout11*, IC_SYNC, OSCin, OSCin*	Connector, SMT, End launch SMA 50 Ohm	Y	Emerson Network Power	142-0701-851	0	0
39	R1, R2	RES, 270 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603270RJNEA	0	0
40	R11, R22	RES, 0 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW06030000Z0EA	0	0
41	R17	RES, 100 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603100RJNEA	0	0

42	R25, R26, R29, R30, R31, R32, R40, R41, R47, R53, R55, R63, R65, R71, R73, R79, R300	RES, 51 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060351R0JNEA	0	0
43	R49, R50, R51, R52, R58, R59, R61, R62, R67, R68, R69, R70	RES, 240 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603240RJNEA	0	0
44	R82, R83	FB, 1000 ohm, 600 mA, 0603	Y	Murata	BLM18HE102SN1D	0	0
45	Y2				DNP_XTAL	0	0

Appendix E: PCB Layers Stackup

6-layer PCB Stackup includes:

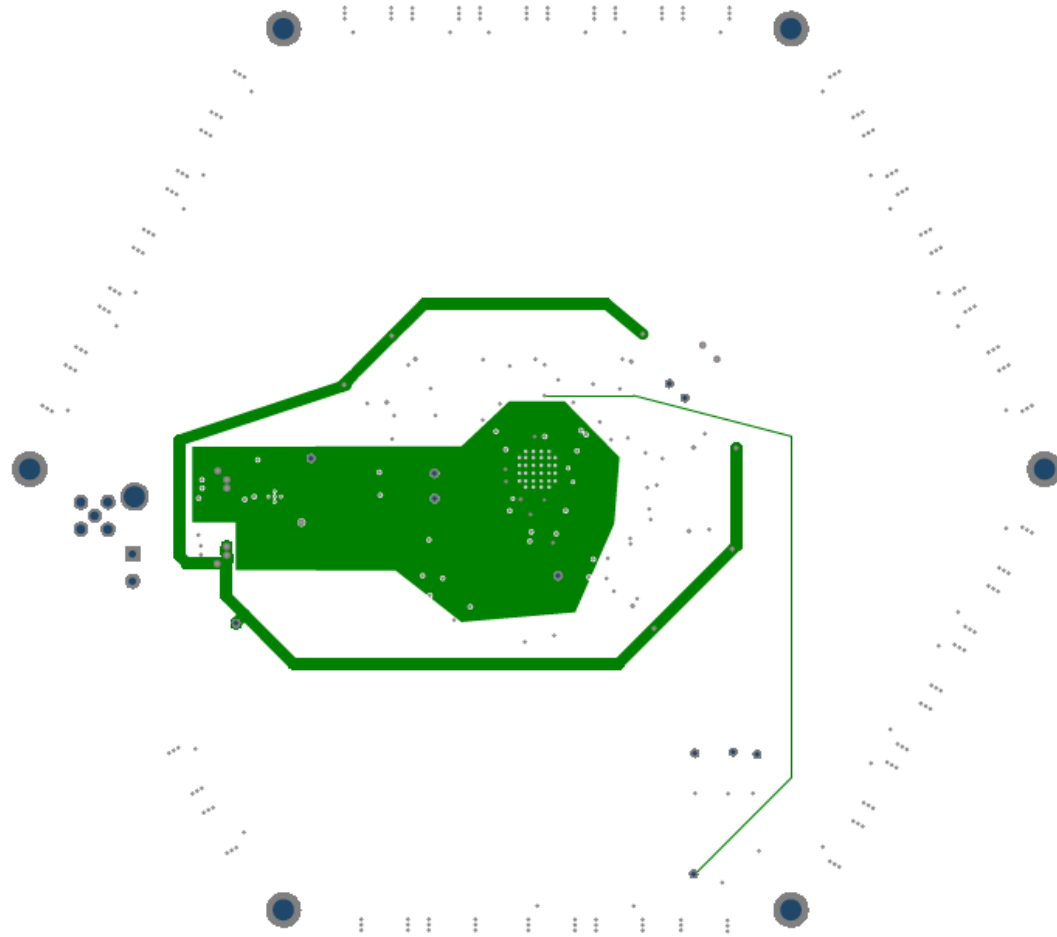
- Top Layer for high-priority high-frequency signals (2 oz.)
- FR4 Dielectric, 19 mils
- RF Ground plane (1 oz.)
- FR4, 14.5 mils
- Power plane (1 oz.)
- FR4, 19 mils
- Bottom Layer copper clad for thermal relief (2 oz.)



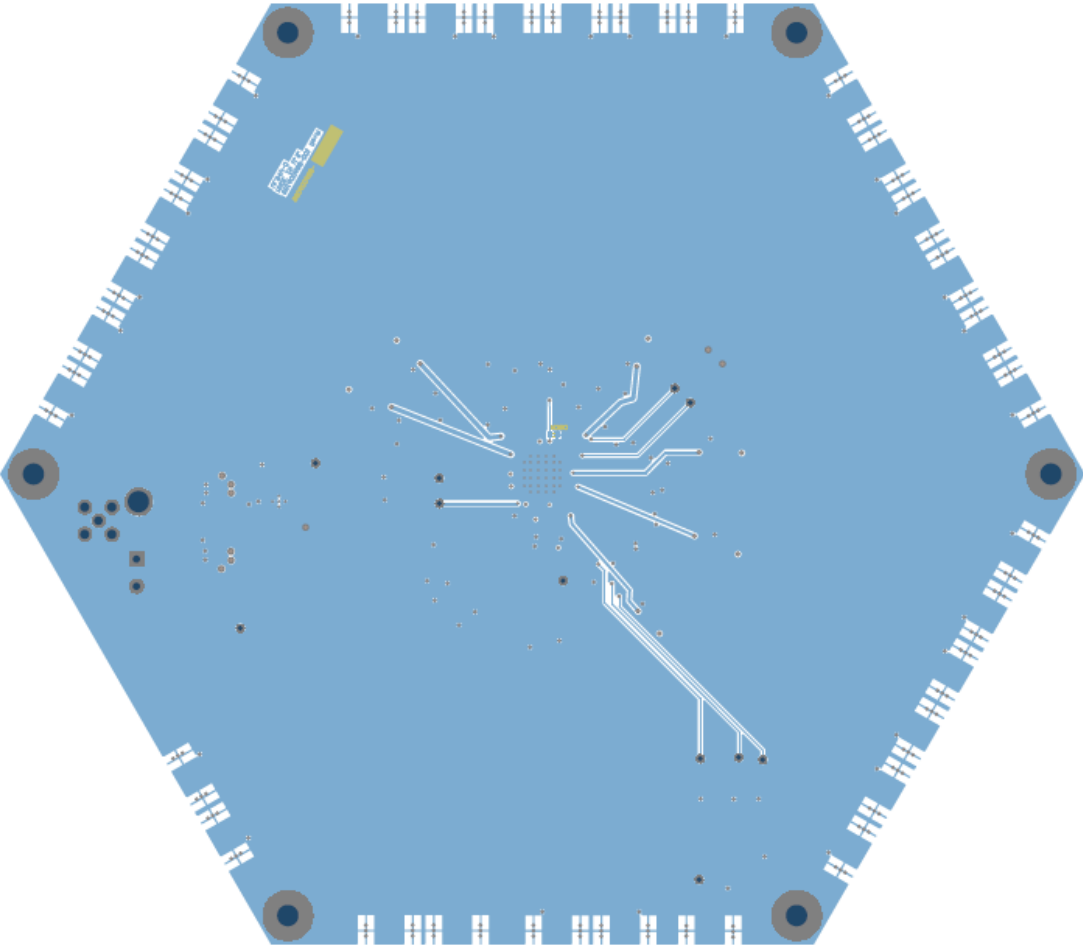
Layer #2 – RF Ground Planes



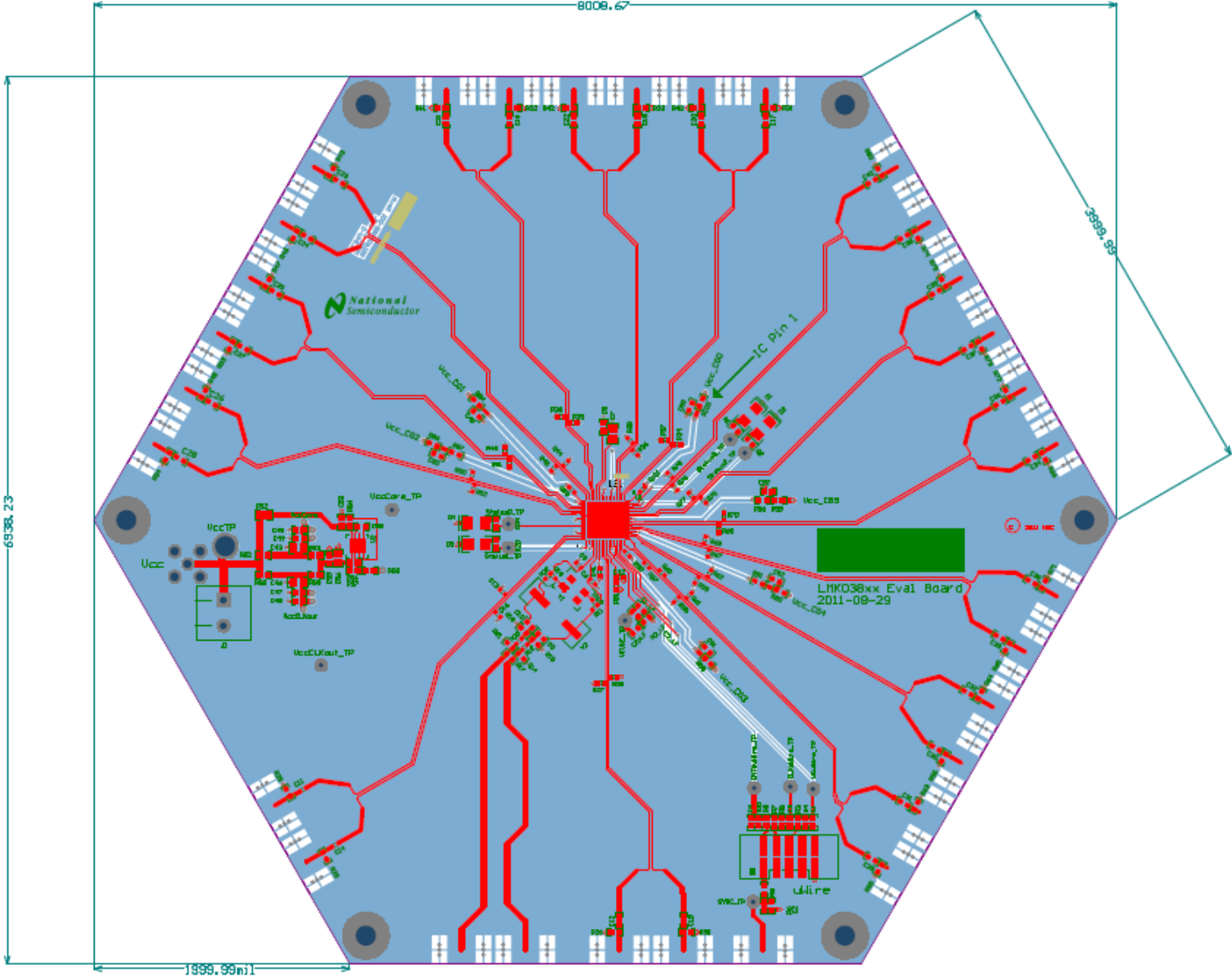
Layer #3 – Vcc Planes



Layer #4 – Bottom



Layers #1 and 6 – Top and Bottom (Composite)



Appendix G: Properly Configuring LPT Port

When trying to solve any communications issue, it is most convenient to verify communication by programming the POWERDOWN bit to confirm normal or low supply current consumption of the evaluation board.

LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click “LPT/USB” → “Check LPT.” If the driver properly loads then the following message is displayed:

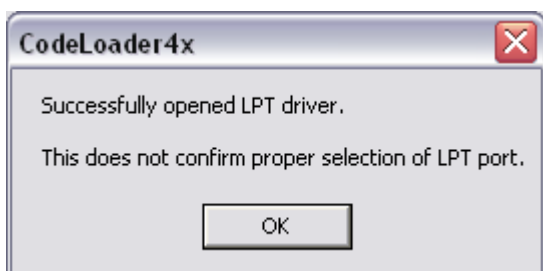


Figure 22: Successfully Opened LPT Driver

Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.

The PC must be rebooted after install for LPT support to work properly.

Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the Properties of the LPT1 port and viewing Resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the traditional port mapping:

Port	Address
LPT1	0x378
LPT2	0x278
LPT3	0x3BC

If a non-standard address is used, use the “Other” port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer’s BIOS settings. The port address can be set in CodeLoader in the Port Setup tab as shown in Figure 23.

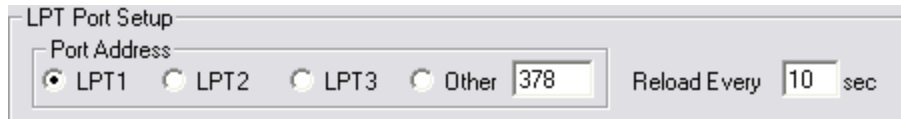


Figure 23: Selecting the LPT Port Address

Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are “Normal,” “Output,” or “AT.” It is possible to enter BIOS setup during the initial boot up sequence of the computer.

Appendix H: Troubleshooting Information

If the evaluation board is not behaving as expected, the most likely issues are...

- 1) Board communication issue
- 2) Incorrect Programming of the device
- 3) Setup Error

Refer to this checklist for a practical guide on identifying/exposing possible issues.

1) Confirm Communications

Refer to Appendix G: Properly Configuring LPT Port to troubleshoot this item.

Remember to load device with Ctrl+L.

This Page Left Intentionally Blank