National Semiconductor

LMK02000EVAL-2

LMK02000 EVB, No VCXO

Precision Clock Conditioner

Evaluation Board Operating Instructions

10-29-2007

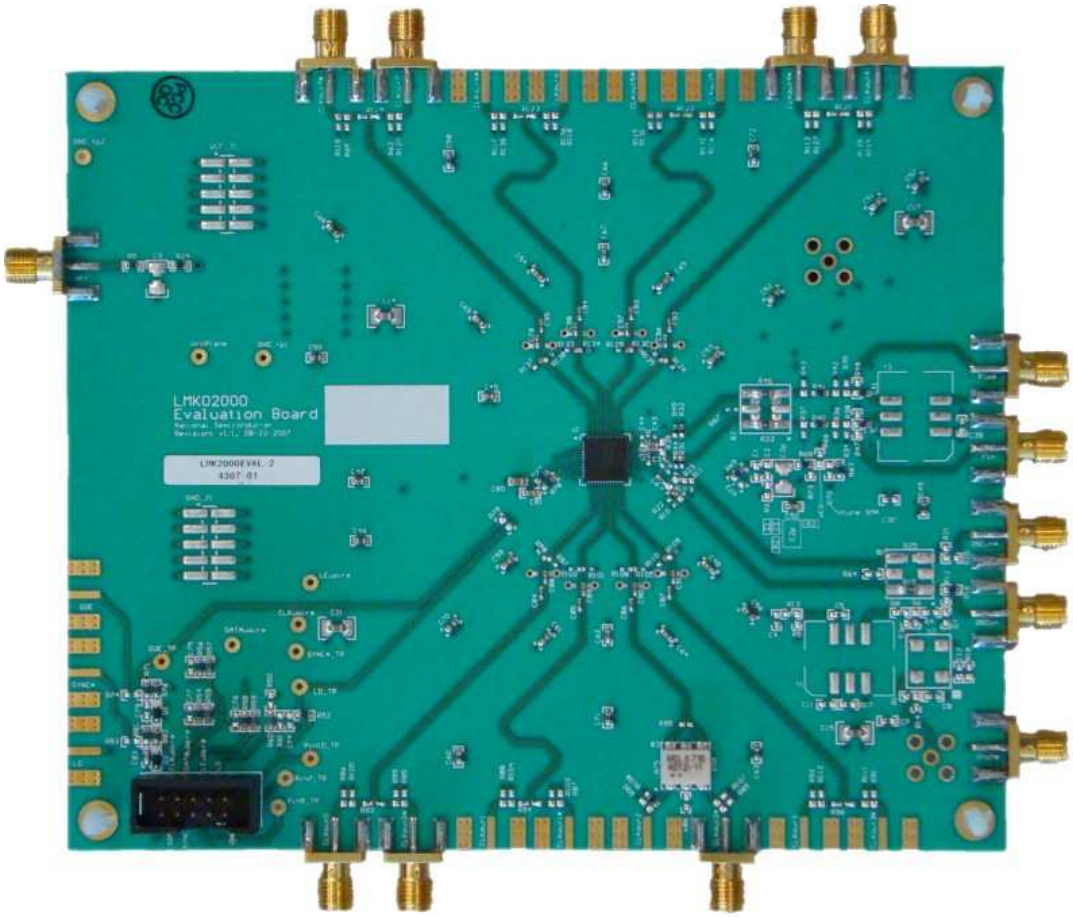

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TABLE OF CONTENTS

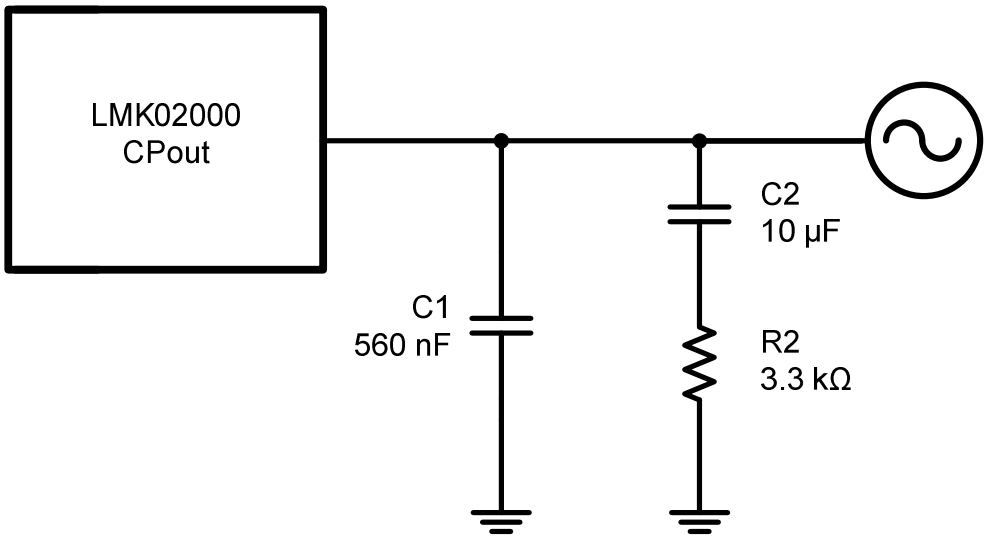
General Description

The LMK02000EVAL-2 Evaluation Board simplifies evaluation of the LMK02000 Precision Clock Conditioner by providing a PCB with the LMK02000 placed and an empty footprint for a user VCXO. The package consists of an evaluation board, an LPT to 10 pin uWire cable, and CodeLoader software. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The purpose of the *CodeLoader* software is to program the internal registers of the LMK02000 device through a MICROWIRE™ interface.

The loop filter of the LMK02000EVAL-2 Evaluation board is not placed allowing for the user to place a loop filter of their own design.

Please refer to the LMK02000EVAL-1 Evaluation Board Instructions for example measurements made with the TCO-2111AA 245.76 MHz VCXO.

Example Loop Filter …for use with TCO-2111AA and 1.2288 MHz Phase Detector Frequency (Fcomp)			
Phase Margin	64º	**Kϕ**	400 uA
Loop Bandwidth	20 Hz	**Fcomp**	1.2288 MHz
Crystal Frequency	12.288 MHz	**Output Frequency**	246.76 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	20 kHz/Volt



Loop filter #1 is selected by placing a 0 ohm resistor on pads R68 and R69.

Loop filter #2 is selected by placing a 0 ohm resistor on pads R72 and R73 and is provided for user convenience. I.e. it is simple to experiment with two loop filters while only changing two resistors.

Read first, Basic Operation

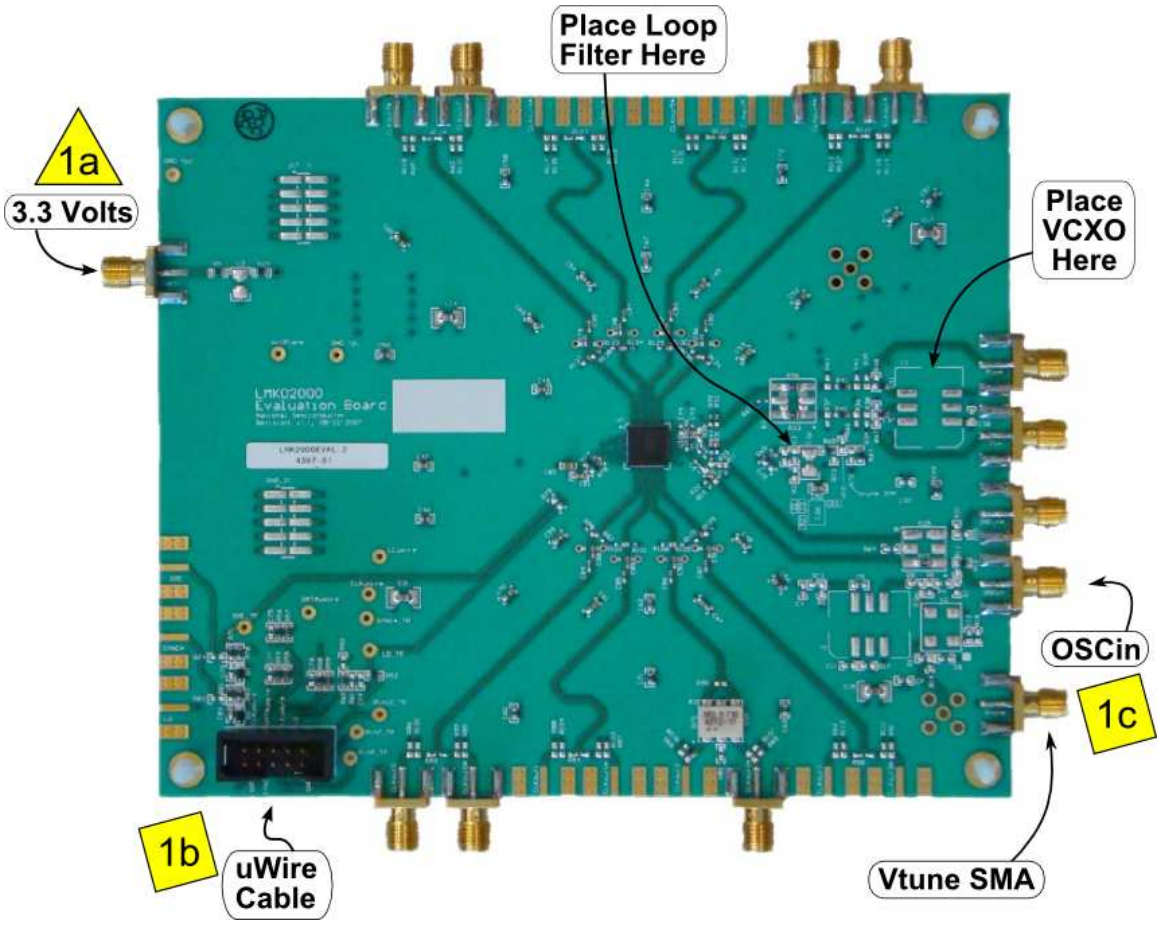
To prepare the computer for use with the evaluation board CodeLoader4 must be installed. Reference the document, *"Installing CodeLoader 4"* and *"Installing USB Driver"* as needed to assist in this task before continuing with the hardware setup.

Note: The instructions below are for an assumed 245.76 MHz VCXO (Epson TCO-2111AA 245.76 MHz), a 12.288 MHz reference, and the example loop filter. Since the VCXO, reference, and loop filter are user supplied on the LMK02000EVAL-2, please adapt the following instructions to your specific case.

For basic operation… with the assumption of a loop filter and on board VCXO being placed…

1) Setup hardware
   a) Connect a low noise **3.3 V** power supply to the **Vcc** connector located at the top left of the board
   b) Connect the LPT to 10 pin uWire cable to the **uWire** header located in the lower left.
   c) Connect a suitable reference oscillator to OSCin. The example default loop filter expects a 12.288 MHz signal. If a signal generator is used, set the power level on a signal generator to 8 dBm.

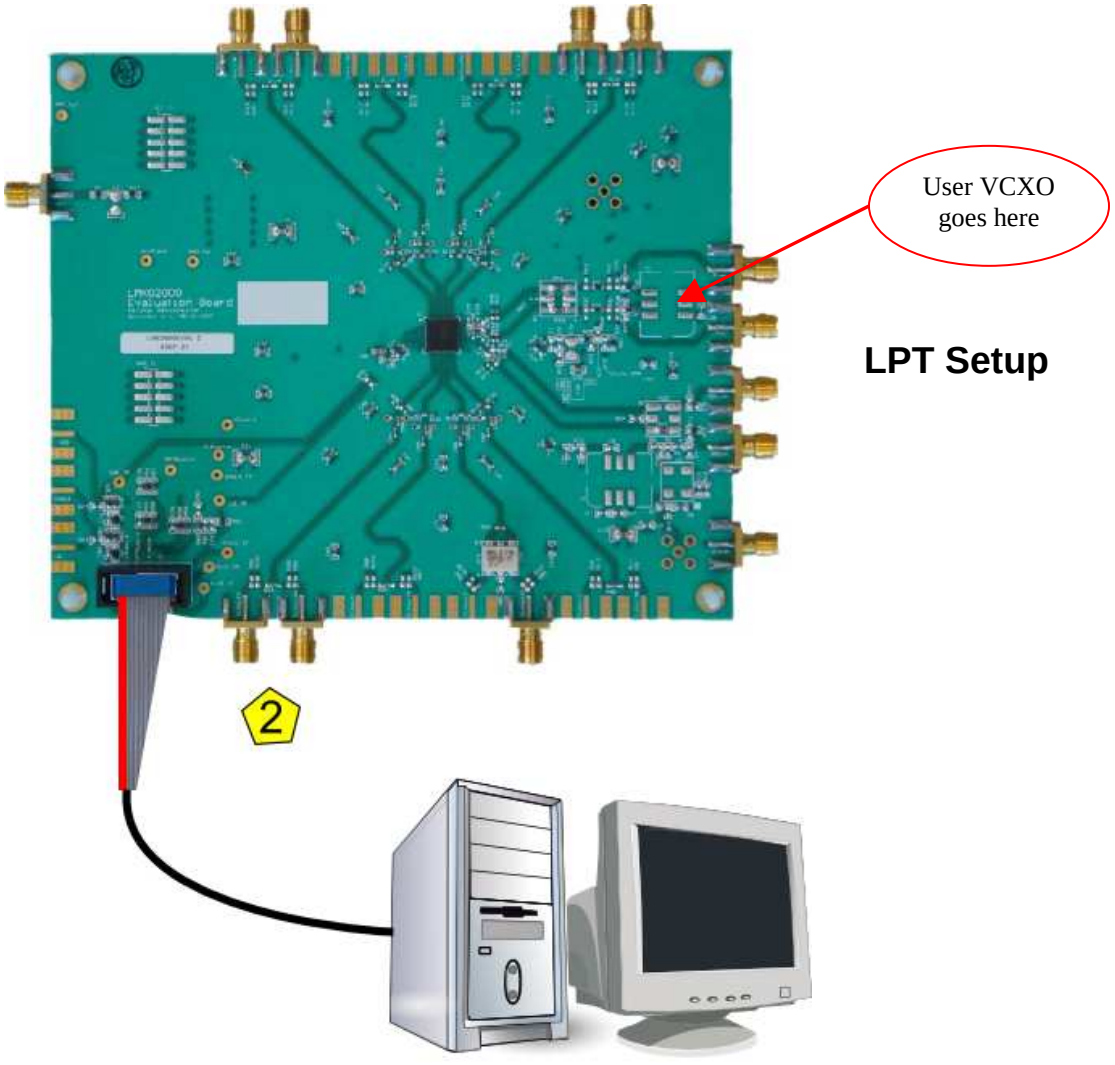
Note: It is also possible to not place the on board VCXO and use the Fin/Fin* connectors with an external signal source. When using an external signal source, Vtune SMA can be used (be sure to connect it to the loop filter by shorting R70).



Read first, Basic Operation (Continued)

2) Connect…
   - PC directly to the evaluation board with the LPT to 10 pin uWire cable, plugging the cable into an LPT port on the computer. This setup is shown below. **The cable can be removed after programming to minimize noise and EMI.**

     or
   - Available separately, the USB <--> uWire board can be connected to the PC with a USB cable. The board provides a 10 pin ribbon cable to connect to the uWire header on the evaluation board as done in step 1b (instead of the LPT to 10 pin uWire cable).



LPT Setup

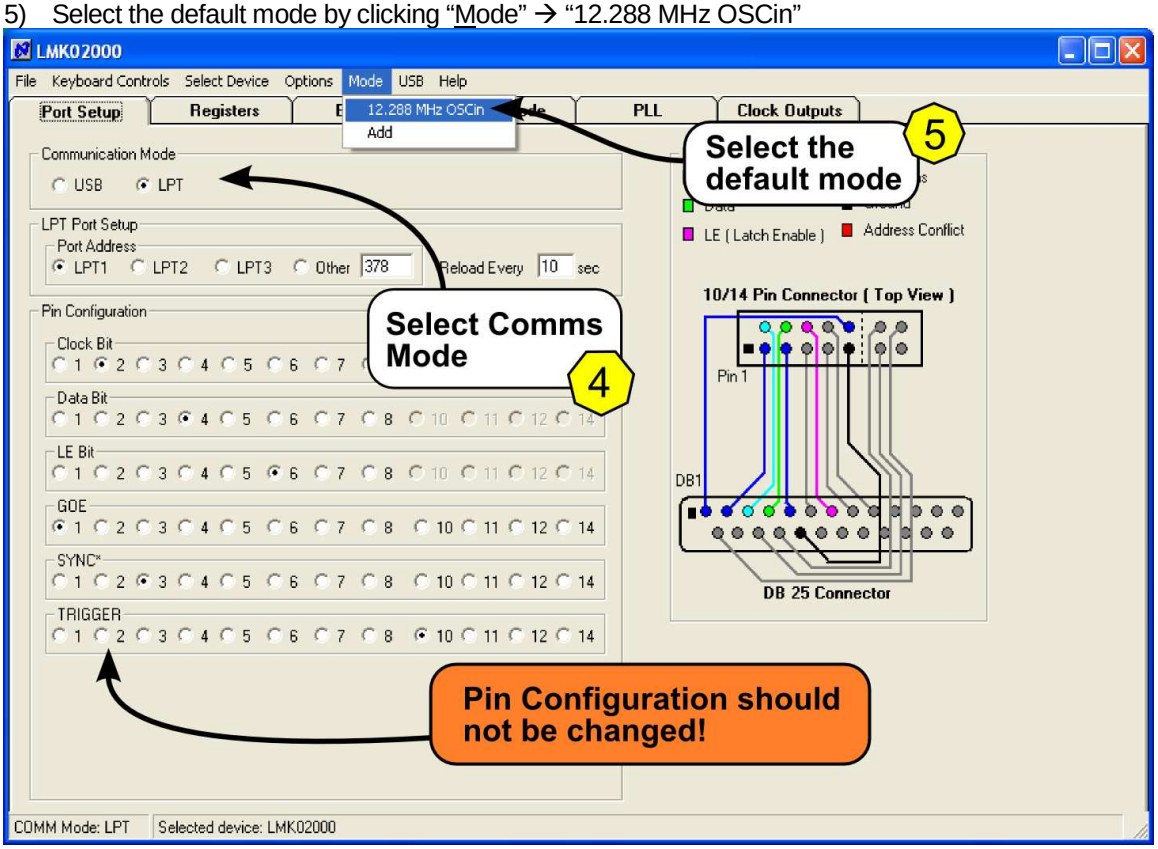
LPT Cable to PC

Read first, Basic Operation (Continued)

3) Start CodeLoader 4.

4) Select the USB or LPT Communication Mode on the Port Setup tab as appropriate.

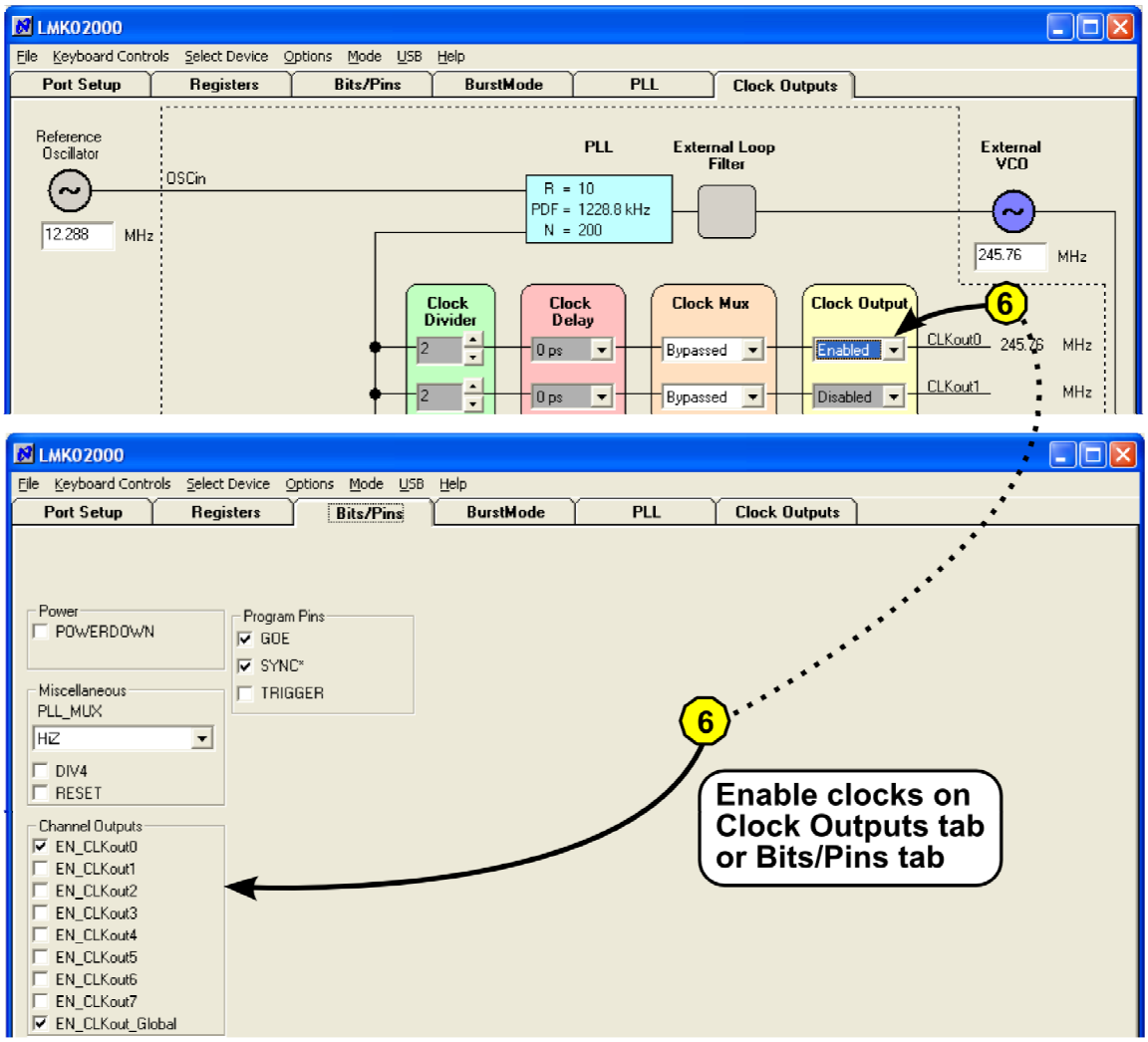
5) Select the default mode by clicking "Mode" → "12.288 MHz OSCin"



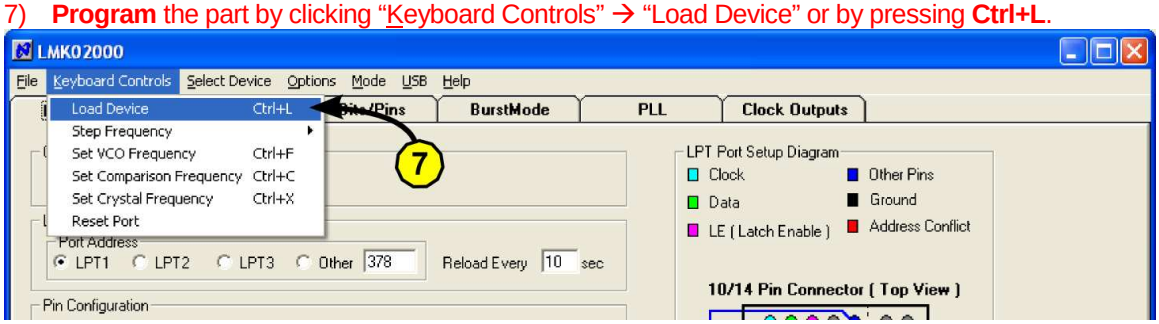
Note: If a different reference or VCXO frequency is used… select this default mode then change the PLL reference and or VCXO frequency. Then when everything in the program is set to defaults as preferred, add the mode to the mode list by clicking, Mode -> Add. Then enter the description. Now in the future a default programming can quickly be set by selecting, Mode -> "Your Description."

Read first, Basic Operation (Continued)

6) **Enable output to be measured**, any of CLKout(0-7) or EN_Fout from either Clock Outputs or Bits/Pins tab.



7) **Program** the part by clicking "Keyboard Controls" → "Load Device" or by pressing **Ctrl+L**.



8) Make measurements… After programming, the **uWire cable can be unplugged from the evaluation board to minimize noise and EMI.**

Board Information

OSCin

By default the board is configured to use an off board reference. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

Single ended OSCin using off board reference [default]	
0 ohm	R15, R16 (RF path)
51 ohm	R22 (Termination)
0.1 uF	C6, C10 (C9 is a 0.1 uF 0402 cap which may be moved to C10)
Open	C9 (Remove stub from OSCin*) R64 (Default) R12 (No stub on OSCin) R10, R19 (Other termination resistors) R1, R9, R13, R14 (Remove power from on-board oscillator for noise reasons)
No Effect	R3, R4, R6, R7, R8 (No effect because R12 is open) R11, R20, R21, R23, R25 (No effect because C9 is open)

Differential OSCin using off board reference	
0 ohm	R15, R16, R20, R25 (RF path)
100 ohm	R19 (Termination)
0.1 uF	C6, C9 (C10 is a 0.1 uF 0402 cap which may be moved to C9)
Open	C10 (Don't AC ground OSCin*) R64 (Default) R12 (No stub on OSCin) R10, R11, R22, R23 (Other termination options) R21 (Do not ground OSCin*) R1, R9, R13, R14 (Remove power from on-board oscillator for noise reasons)
No Effect	R3, R4, R6, R7, R8 (No effect because R12 is open)

Single ended OSCin using on board reference	
User XO	Y2 (User XO placed here. LMK0300xCEVAL boards places Crystek XO P/N: C3391-xx.xxx MHz
0 ohm	R3, R4, R12, R15 (RF path) R14 (Power XO)
51 ohm	R22 (Termination)
0.1 uF	C6, C10 (C9 is a 0.1 uF 0402 cap which may be moved to C10)
Open	C9 (Remove stub from OSCin*) R64 (Default) R16 (R12 & R16 mutually exclusive) R10, R19 (Other termination resistors) R1, R9, R13 (Remove power from unused on-board oscillator for noise reasons) R8 (R8 & R3 is mutually exclusive)
No Effect	R11, R20, R21, R23, R25 (No effect because C9 is open)
Optional	R4, R6, R7 (Are for pad to keep input power levels valid)

Fin

By default the board is configured to use an LVPECL VCXO on Y3.

It is also possible to configure the board to use an off board Fin source for locking the loop (when Vtune is used from on/board with external VCO/VCXO) or for distribution of a signal (set charge pump to tri-state). Below are several possible configurations for driving Fin.

LVPECL VCXO on Fin [default]	
Place VCXO	Y3 – Place your VCXO here. This setup assumes it is an LVPECL VCXO. **Upon shipment the LMK02000EVAL-2 has no VCXO in this position, it is open.**
0 ohm	C37, R40, R33, C41, R41, R46 (RF path) R30 (Vcc to VCXO from plane voltage)
120 ohm	R31, R32 (default LVPECL termination to Vcc – 2V)
82 ohm	R44, R45 (default LVPECL termination to Vcc – 2V)
0.1 uF	C34, C40 (C44 is a 0.1 uF 0402 cap which may be moved to C40. Fin/Fin* must be AC coupled)
Open	R39 (Other termination options) R34, R35, R67, C43 (Default) R36, R37, R42, R43 (Optional pad – along with R40 and R41) R47, R48 (Optional Fin/Fin* input / stub remover) R29 (Optionally power VCXO from VCO_VCXO_Vcc SMA – if used remove R30 for plane Vcc)

Off board VCO/VCXO/TCXO thru Fin/Fin* SMAs	
As required	R31, R32, R39, R44, R45 (Terminate VCO/VCXO/TCXO as required)
As required/ 0.1 uF	C34, C40 (C44 is a 0.1 uF 0402 cap which may be moved to C40 for single ended. Fin/Fin* must be AC coupled)
0 ohm	R47, R40, R33, R48, R41, R46 (RF path)
Open	R29, R30 (Remove power from onboard VCXO if placed) R34, R35, R67, C43 (Default) R36, R37, R42, R43 (Optional pad – along with R40 and R41) C37, C41 (Optional VCXO input / remove stub)
No Effect	Y3 (On board VCXO is bypassed / unpowered)

Loop Filter

The PCB allows for two separate loop filters to be placed. Four resistors switch loop filter #1 or #2 into the circuit.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [top side]	R68 & R69 shorted	C1, C2, C2p, R2	No filter placed
Loop Filter #2 [bottom side]	R72 & R73 shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	No filter placed

Features of the board

- Either one of two loop filters can be selected by shorting either (R68 & R69 or R72 & R73).
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to National Semiconductor's traditional reference designators associated with loop filters.

Recommended Equipment

Power Supply

The Power Supply should be a low noise power supply. An Agilent 6623A Triple power supply with external LC filters or an HP E3610A with external LC filters was used in creating these evaluation board instructions. The LC filters on the outputs help to reduce noise from the power supplies.

Phase Noise / Spectrum Analyzer

Due to the high performance of the LMK02000 and typical VCXOs the local oscillator noise of most spectrum analyzers is too high and measurements will be of the local oscillator of the spectrum analyzer, not the LMK02000/VCXO under test. An Agilent E5052A was used for all phase noise measurements in this document.

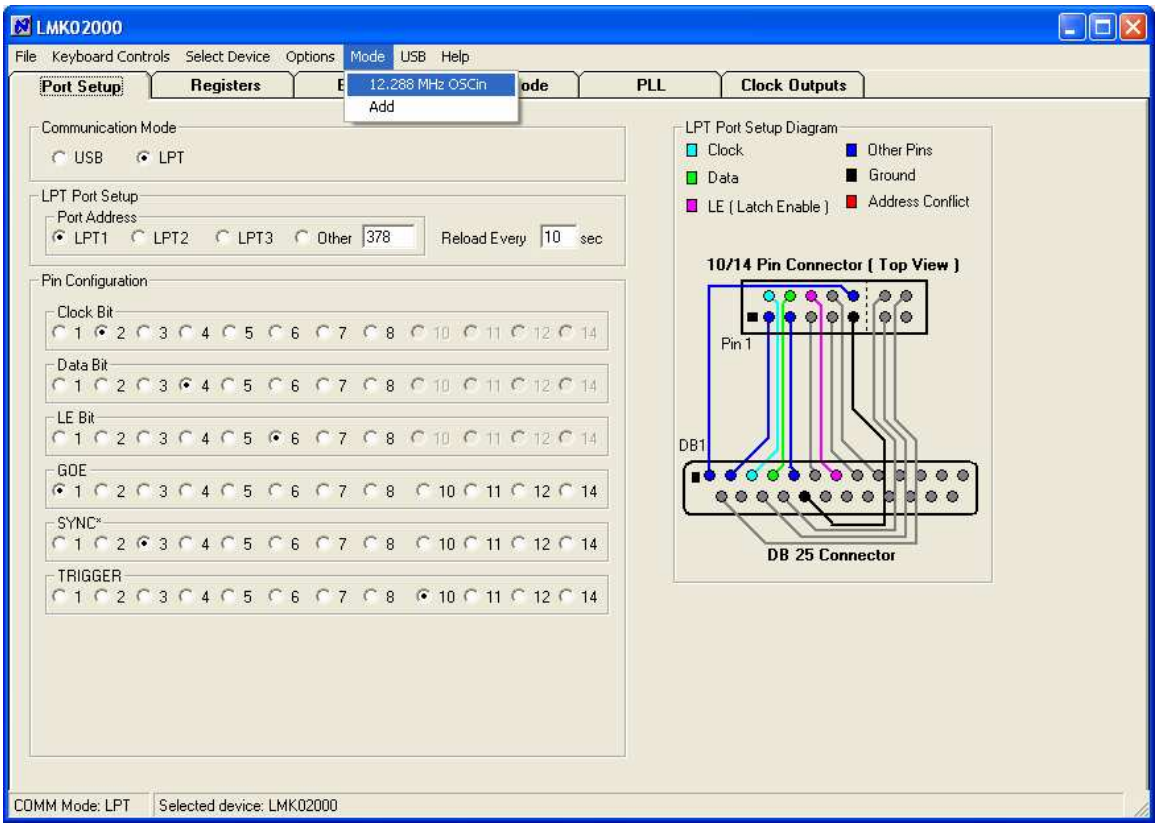
Oscilloscope

For measuring delay an Agilent Infiniium DSO81204A was used.

Reference Oscillator

A recovered clock (LVDS or LVPECL) may drive OSCin. If a signal generator (sine wave) is used, program the power to 8 dBm to ensure a fast slew rate.

CodeLoader Settings

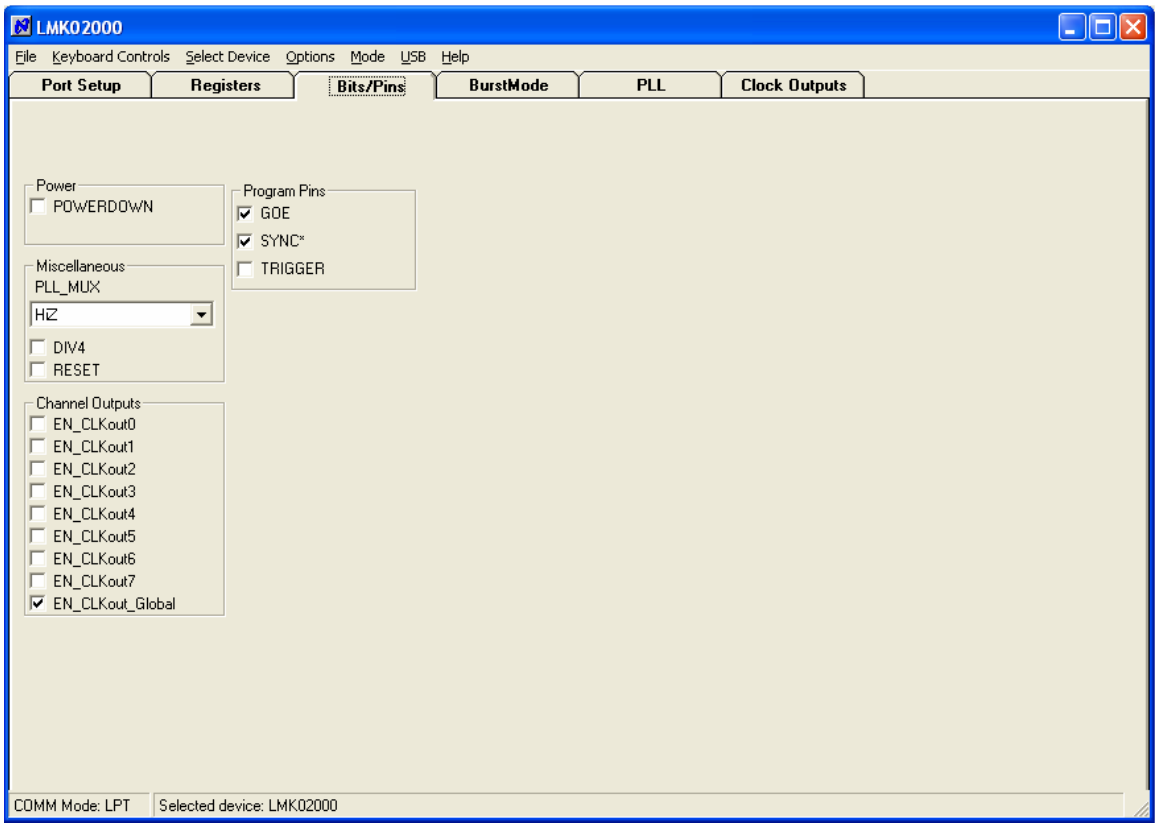


The Port Setup tab tells CodeLoader what signals are assigned to which pins. If this is wrong, the part will not program.

The default mode for all programming registers can be restored to the default state by clicking Mode → "12.288 MHz OSCin" The default reference oscillator used for these instructions is 12.288 MHz and the restored mode expects a 12.288 MHz OSCin signal. **For the loaded mode to take affect the device must be loaded by pressing Ctrl+L.** However, this will not restore the default Pin Configuration. If any Pin Configuration settings are accidentally changed, refer to the above diagram to fix the Pin Configuration.

Note: If a different reference or VCXO frequency is used… select this default mode (12.288 MHz) then change the PLL reference and or VCXO frequency. When everything in the program is set to defaults as preferred, add the mode to the mode list by clicking, Mode -> Add. Then enter the description. Now in the future a default programming can quickly be set by selecting, Mode -> "Your Description."

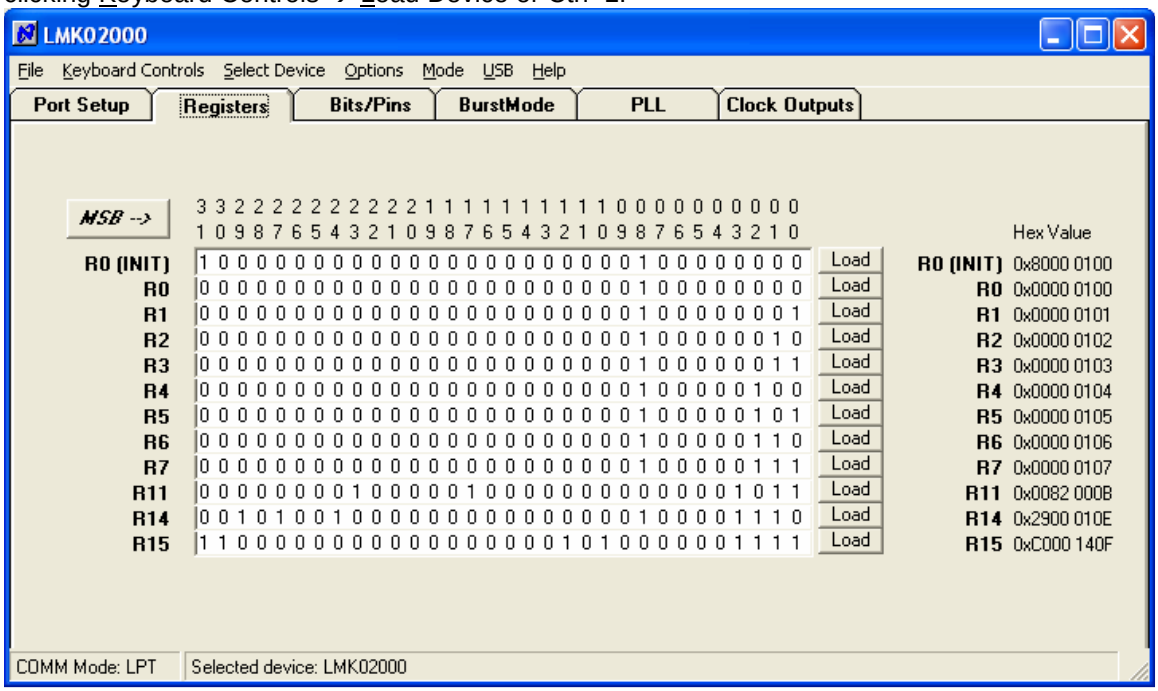
The Bits/Pins tab shows some of the internal registers which are not accessible from any of the other visual tabs like “PLL” and “Clock Outputs.” *Right click on any of the bits for description.*



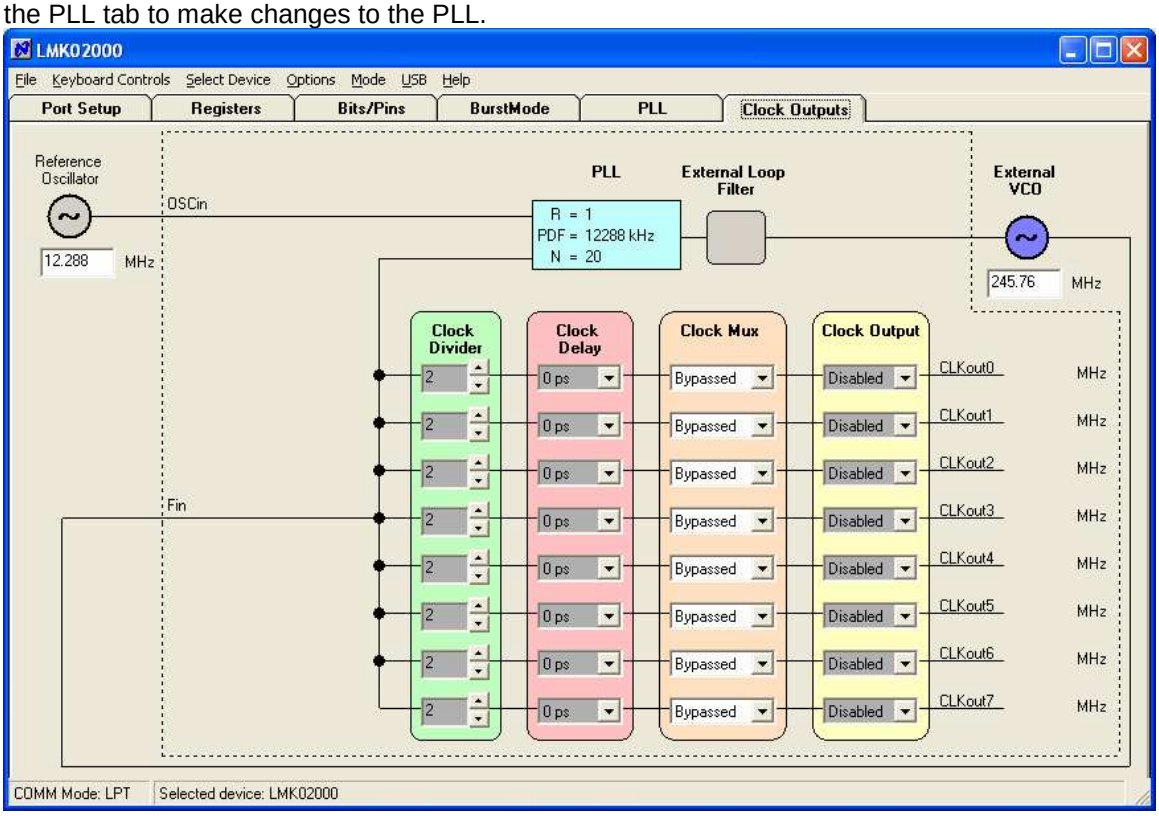
Program Bits	
POWERDOWN	Powers the part down.
PLL_MUX	Programmable to many different values to support Lock Detect or aid troubleshooting.
DIV4	Shall be checked for PDF frequencies greater than 20 MHz.
RESET	The registers can be defaulted by checking and unchecking RESET. Software bits will not reflect this.
EN_CLKout0..7	Enable CLKout bits from CLKout0 to CLKout7. Also accessible from Clock Outputs tab.
EN_CLKout_Global	Enable all clock outs. If unselected then the EN_CLKouts are overridden and the outputs are all disabled.

Program Pins	
GOE	Set Global Output Enable to high or low logic level.
SYNC*	Set SYNC* pin to high or low logic level.
TRIGGER	Set auxiliary trigger pin to high or low logic level.

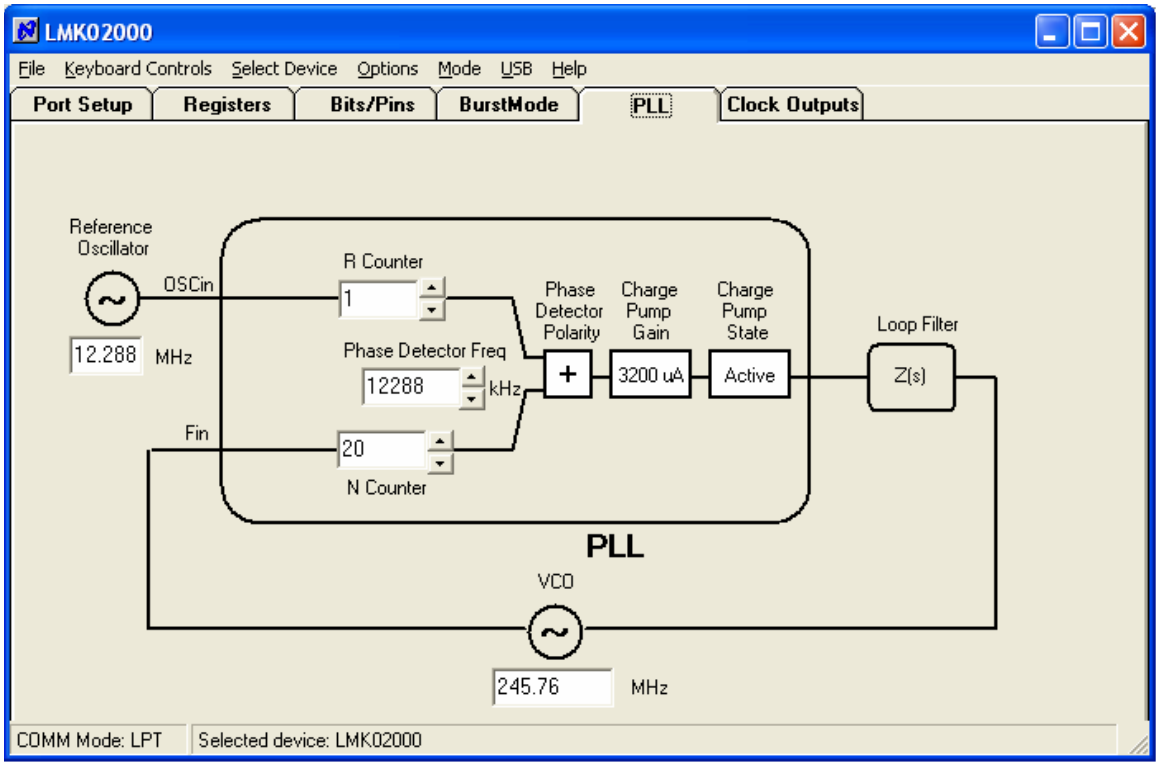
The Registers tab shows the raw bits which will be programmed when device is loaded by clicking Keyboard Controls → Load Device or Ctrl+L.



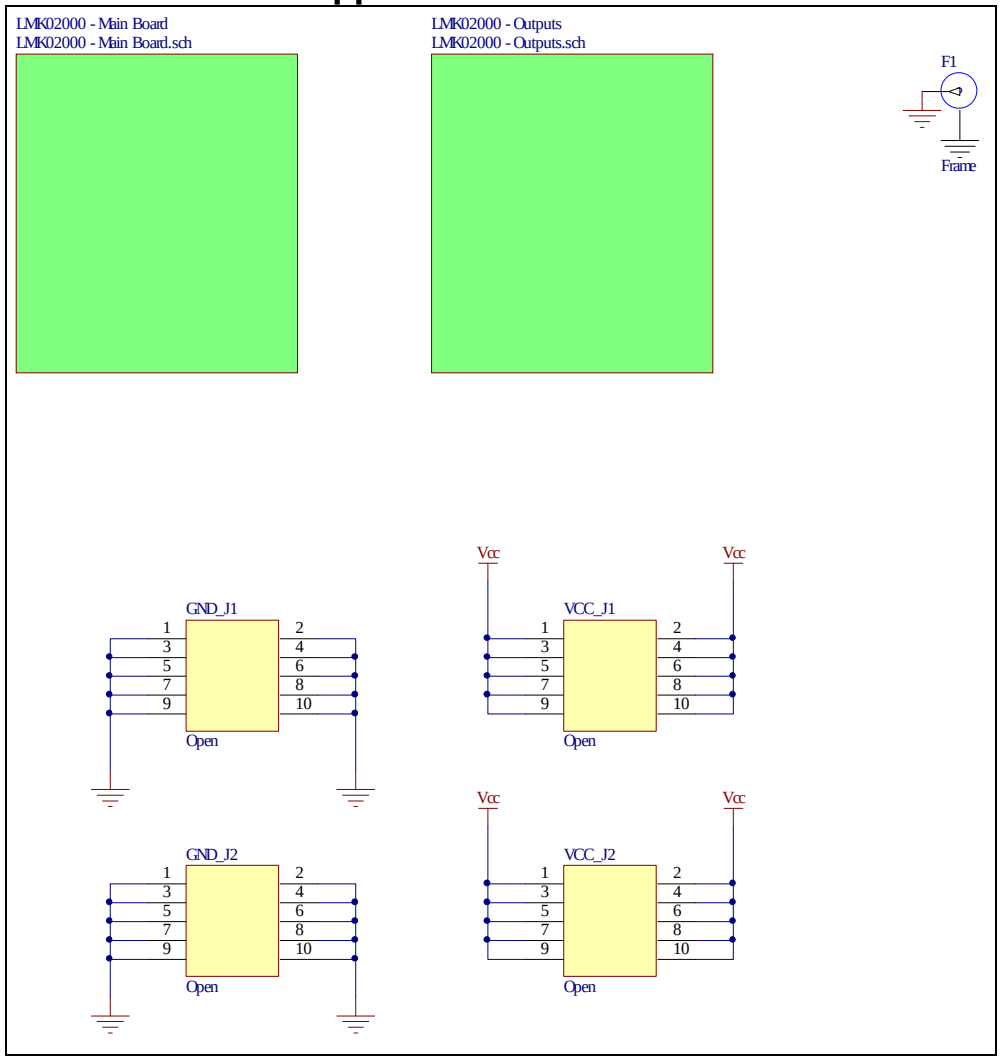
The Clock Outputs tab allows the user to visualize the clock distribution portions of the device. From this tab the device's dividers, delays, clock output muxes, and output drivers can be programmed along with internal loop filter values. The PLL block shows the R and N divider values however to change these values either click on the PLL tab or the blue PLL box to access the PLL tab to make changes to the PLL.

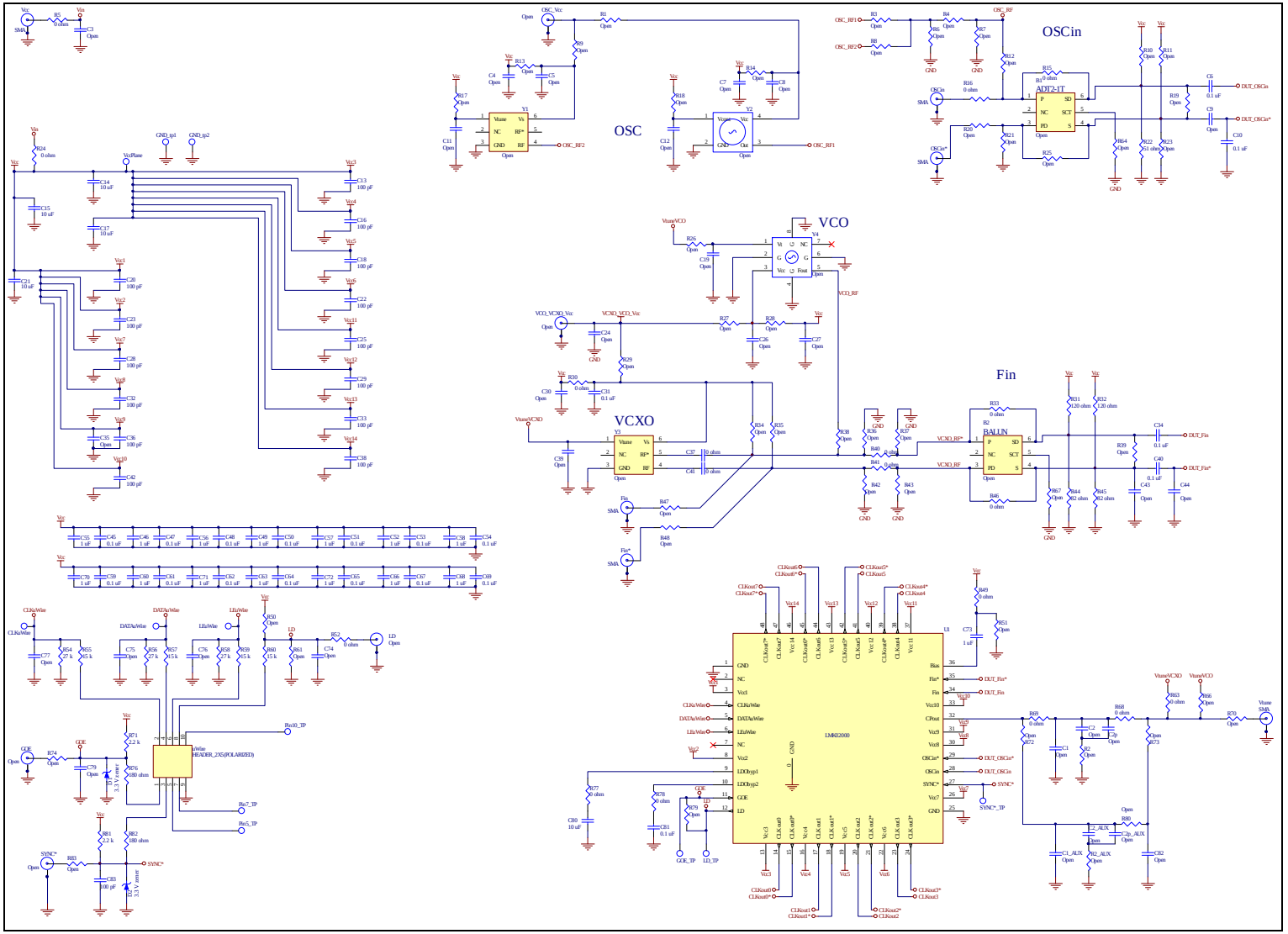


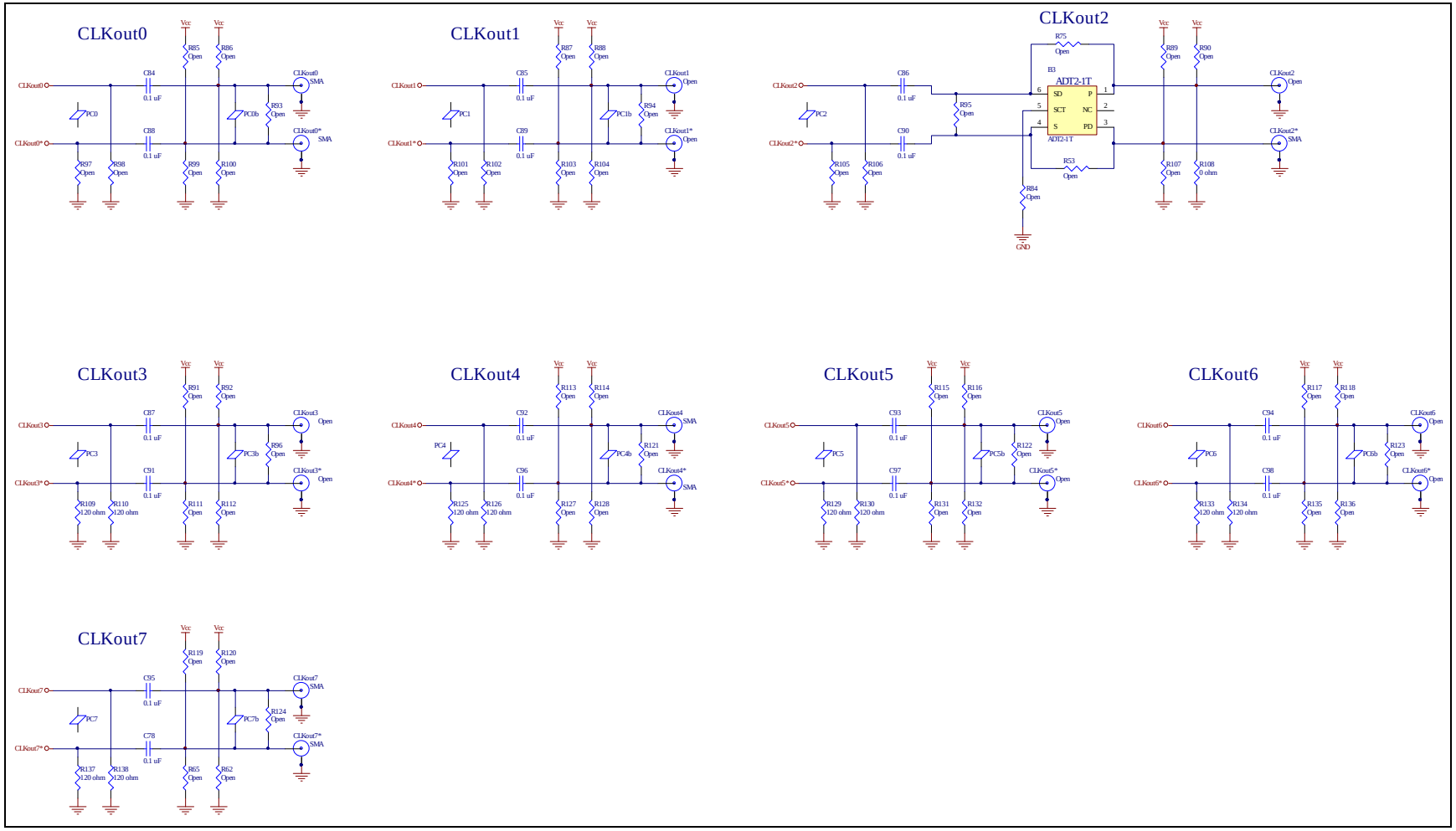
The PLL tab shows a conventional PLL diagram.



Appendix A: Schematic




OSC
OSCin
VCO
VCXO
Fin
ADT2-1T
BALUN
LMK02000

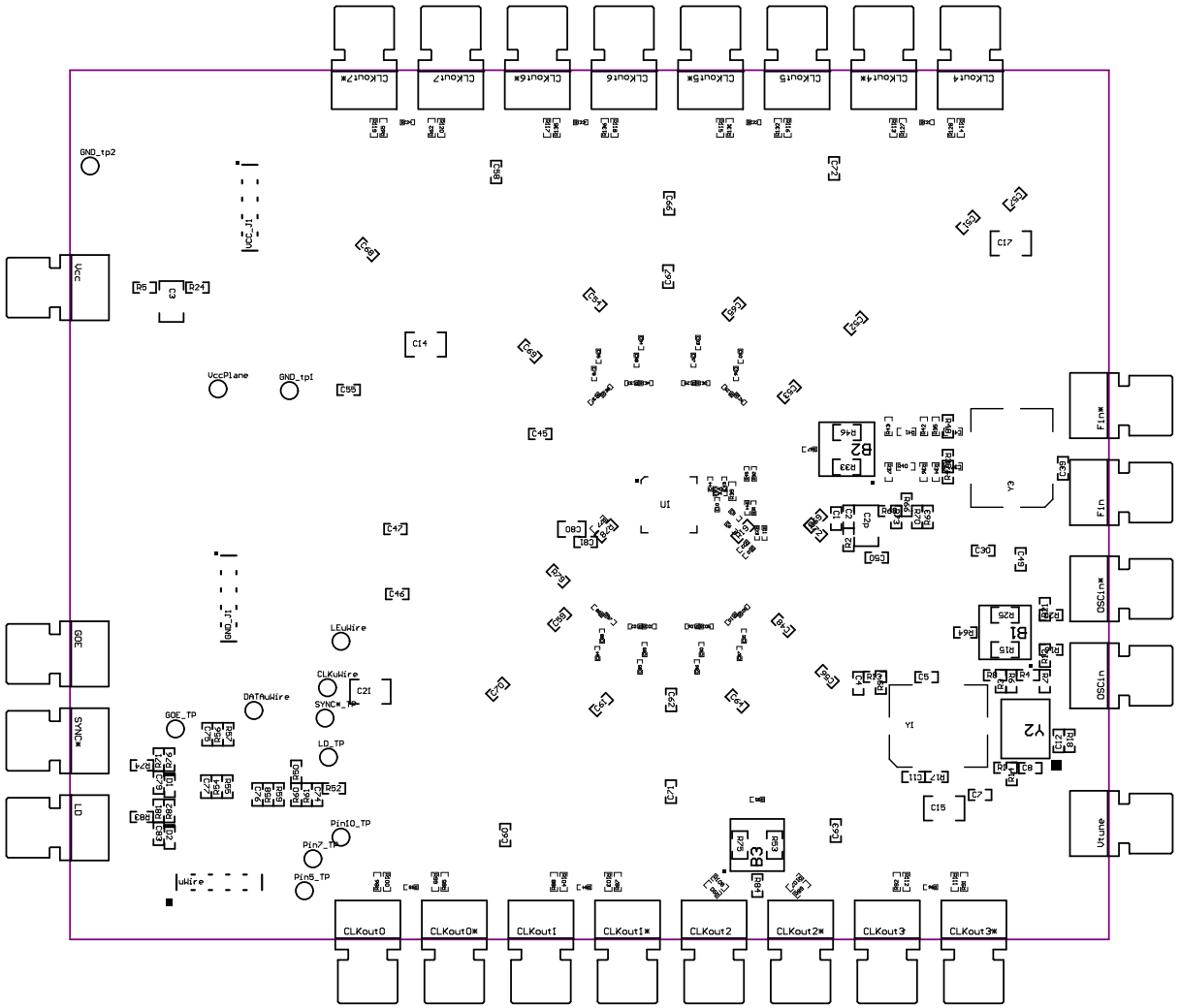

CLKout0
CLKout1
CLKout2
CLKout3
CLKout4
CLKout5
CLKout6
CLKout7
ADT2-1T
GND

Appendix B: Bill of Materials

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
100 pF	Kemet	C0402C101J5GAC	14	C13, C16, C18, C20, C22, C23, C25, C28, C29, C32, C33, C36, C38, C42
100 pF	Kemet	C0603C101J5GAC	1	C83
0.1 uF	Kemet	C0402C104J4RAC	20	C6, C10, C34, C40, C78, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98
0.1 uF	Kemet	C0603C104J3RAC	16	C31, C45, C47, C48, C50, C51, C53, C54, C59, C61, C62, C64, C65, C67, C69, C81
1 uF	Kemet	C0603C105K8VAC	14	C46, C49, C52, C55, C56, C57, C58, C60, C63, C66, C68, C70, C71, C72
1 uF	Kemet	C0603C105K8VAC	1	C73
10 uF	Kemet	C0805C106K9PAC	4	C14, C15, C17, C21
10 uF	Kemet	C0805C106K9PAC	1	C80
Resistors				
0 ohm	Vishay	CRCW0603000ZRT1	7	C37, C41, R40, R41, R49, R77, R108
0 ohm	Vishay	CRCW0603000ZRT1	9	R5, R16, R24, R30, R52, R63, R68, R69, R78
0 ohm	Yageo	RC0805JR-070RL	3	R15, R33, R46
51 ohm	Yageo	CRCW040251R0FKED	1	R22
82 ohm	Vishay/Dale	CRCW040282R0JNED	2	R44, R45
120 ohm	Vishay	CRCW0402120RJNED	12	R31, R32, R109, R110, R125, R126, R129, R130, R133, R134, R137, R138
180 ohm	Vishay	CRCW0603181JRT1	2	R76, R82
2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R71, R81
15 k	Vishay	CRCW0603153JRT1	4	R55, R57, R59, R60
27 k	Vishay	CRCW0603273JRT1	3	R54, R56, R58
Other				
ADT2-1T	Minicircuits	ADT2-1T	1	B3
SMA	Johnson	142-0701-851	13	CLKout0, CLKout0*, CLKout2*, CLKout4, CLKout4*, CLKout7,

	Components			CLKout7*, Fin, Fin*, OSCin, OSCin*, Vcc, Vtune
3.3 V zener	Comchip	CZRU52C3V3	2	D1, D2
PCB	Printed Circuits Corp	LMK02000 v1.1 08-22-2007	1	PCB
LMK02000	National Semiconductor	LMK02000 I	1	U1
HEADER_2X5(POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
SPCS-8	SPC Technology	SPCS-8	4	Standoffs in the four corners (insert from bottom)
Open				
Open	-	Open	1	B1
Open	-	Open	1	B2
Open	-	603	56	C1, C2, C2_AUX, C4, C5, C7, C8, C11, C12, C19, C26, C27, C30, C39, C74, C75, C76, C77, C79, C82, R1, R2, R2_AUX, R3, R4, R6, R7, R8, R9, R12, R13, R14, R17, R18, R19, R20, R21, R26, R27, R28, R29, R38, R47, R48, R50, R61, R64, R66, R70, R72, R73, R74, R79, R80, R83, R84
Open	-	805	2	C1_AUX, C24
Open	-	Open	3	C2p, C2p_AUX, C3
Open	-	603	40	C35, R34, R35, R36, R37, R39, R42, R43, R51, R62, R65, R85, R86, R87, R88, R89, R90, R91, R92, R99, R100, R103, R104, R107, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R127, R128, R131, R132, R135, R136
Open	-	402	21	C9, C43, C44, R10, R11, R23, R67, R93, R94, R95, R96, R97, R98, R101, R102, R105, R106, R121, R122, R123, R124
Open	-	Open	12	CLKout1, CLKout1*, CLKout2, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout6, CLKout6*, GOE, LD, SYNC*
Open	-	Open	4	GND_J1, GND_J2, VCC_J1, VCC_J2
Open	-	Open	2	OSC_Vcc, VCO_VCXO_Vcc
Open	-	805	3	R25, R53, R75
Open	-	Open	4	Y1, Y2, Y3, Y4

Appendix C: Build Diagram



Bottom Build Diagram