

BIG GIG REFERENCE PLATFORM

ADC08/500/D500/D1000/D1020/D1500/D1520

MANUFACTURING KIT / REFERENCE DESIGN (A1)

National Semiconductor GHz 8 bit ADC + XILINX Virtex 4

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "N/A" are NOT ASSEMBLED.

Print Instructions:


- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.

SYSTEM CONFIGURATION

Module	Configuration	Description
FRONT END	2 channel DIFFERENTIAL	AC/ DC COUPLING ON I CHANNEL SIGNAL PATH. AC COUPLING ONLY ON Q CHANNEL SIGNAL PATH.
CLOCK SOURCE	DIFFERENTIAL	LMX231X PLL
FPGA		XC4VLX15 - 363 PIN BGA
USB I/F		CY7C64613 EZ USB

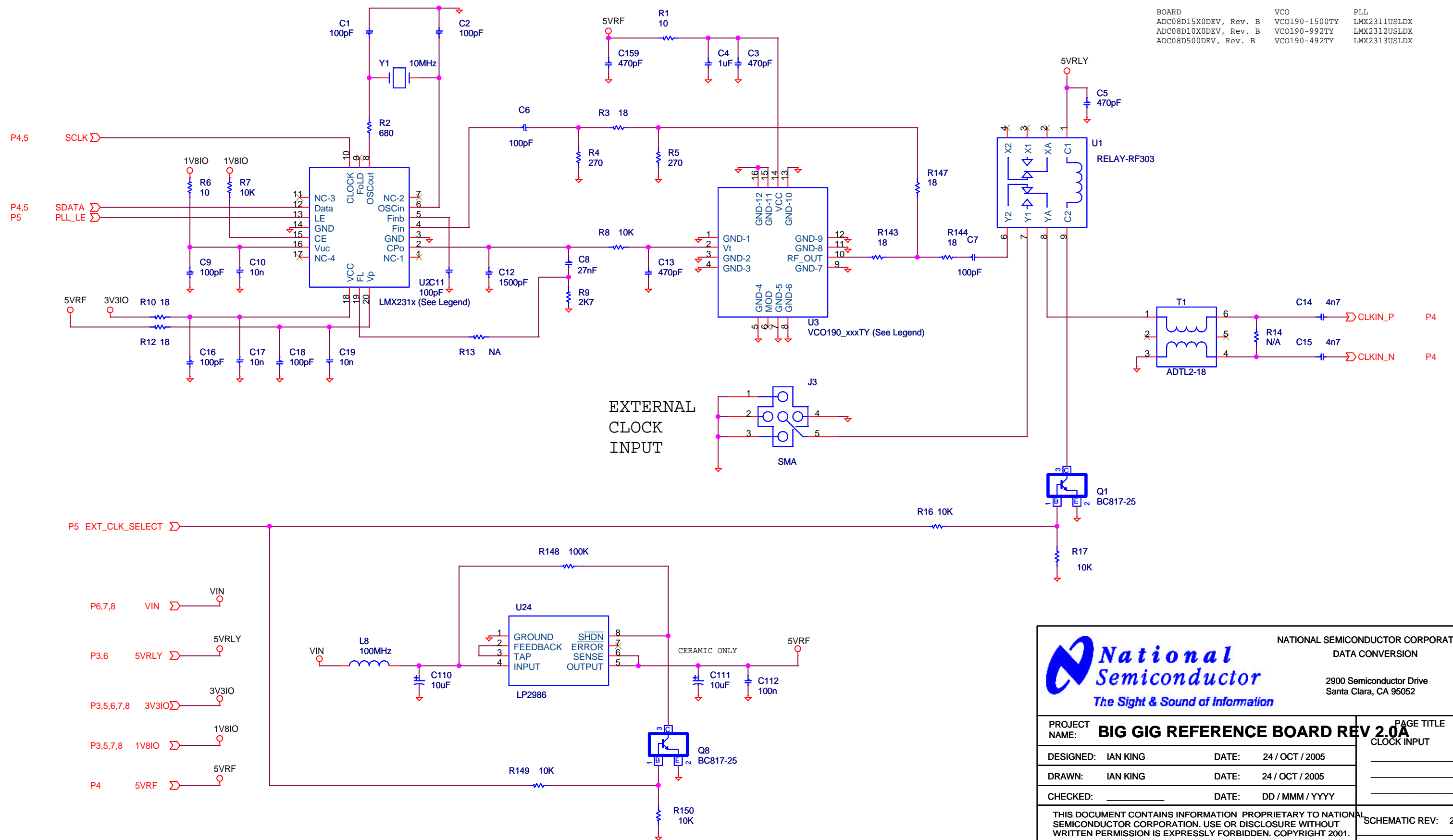
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DRAWN: IAN KING/ C. CHASE	DATE: May 9th 2006	LAYOUT REV:	REV 5.0
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VCO and PLL Legend

BOARD	VCO	PLL
ADC08D15X0DEV, Rev. B	VCO190-1500TY	LMX2311USLDX
ADC08D10X0DEV, Rev. B	VCO190-992TY	LMX2312USLDX
ADC08D500DEV, Rev. B	VCO190-492TY	LMX2313USLDX

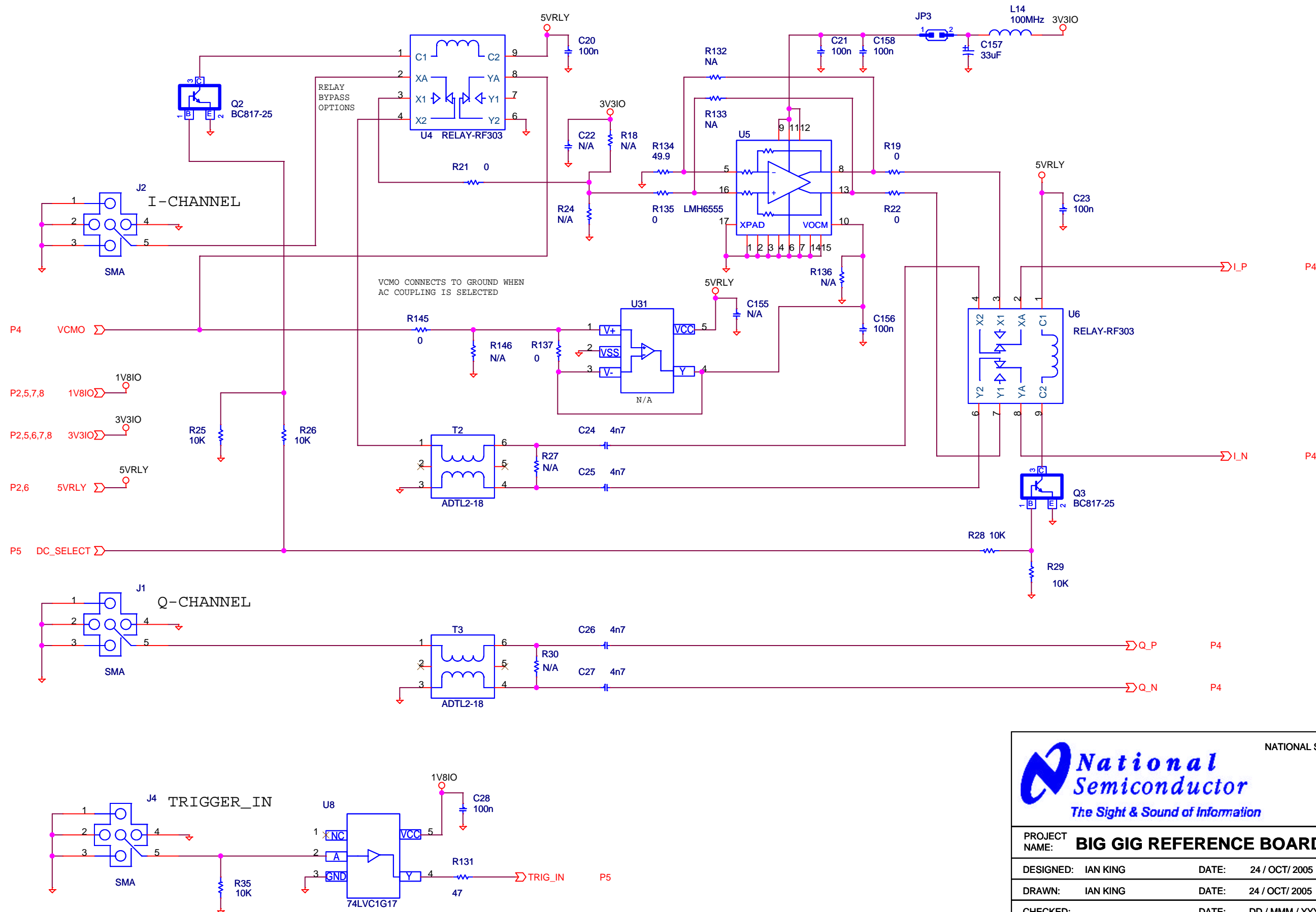




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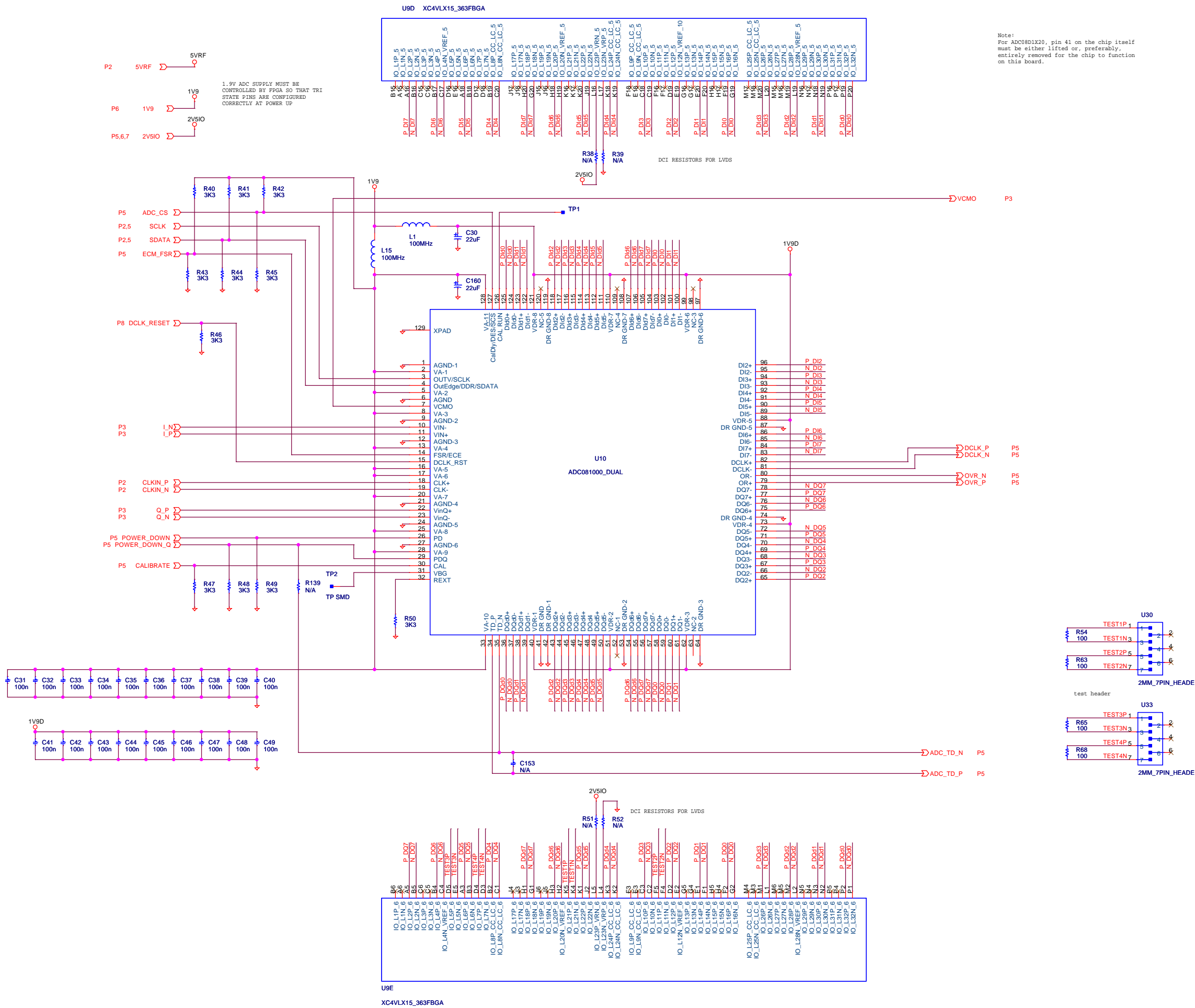
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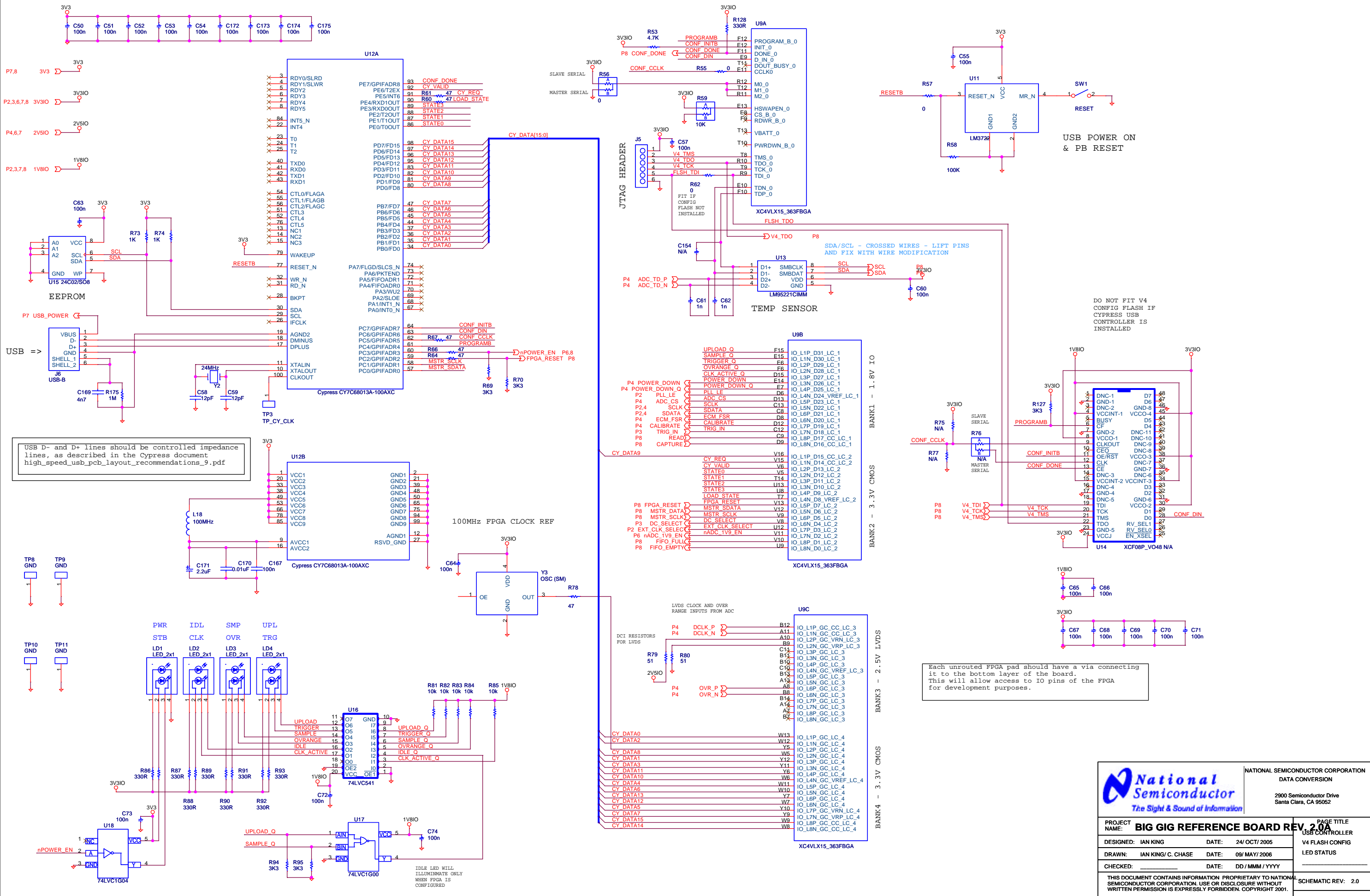
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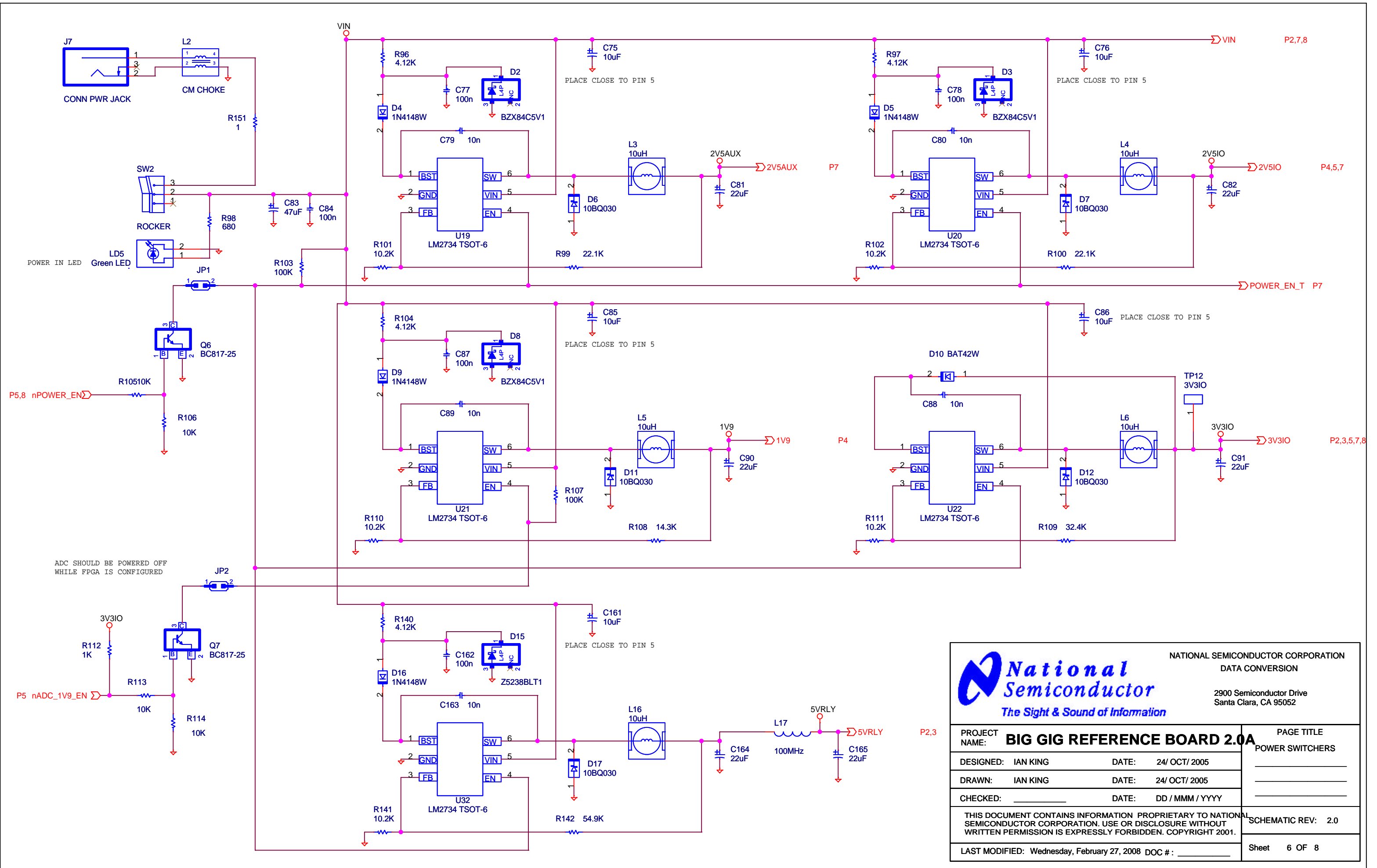
Note:
For ADC08D1X20, pin 41 on the chip itself must be either lifted or, preferably, entirely removed for the chip to function on this board.

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PROJECT NAME: BIG GIG REFERENCE BOARD REV 2.0A	DATE: 24/OCT/2005	PAGE TITLE: USB CONTROLLER	
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*POWER_EN = 1 - SWITCH RESG SHUTDOWN (STANDBY)
 *POWER_EN = 0 - SWITCH RESG ARE ON



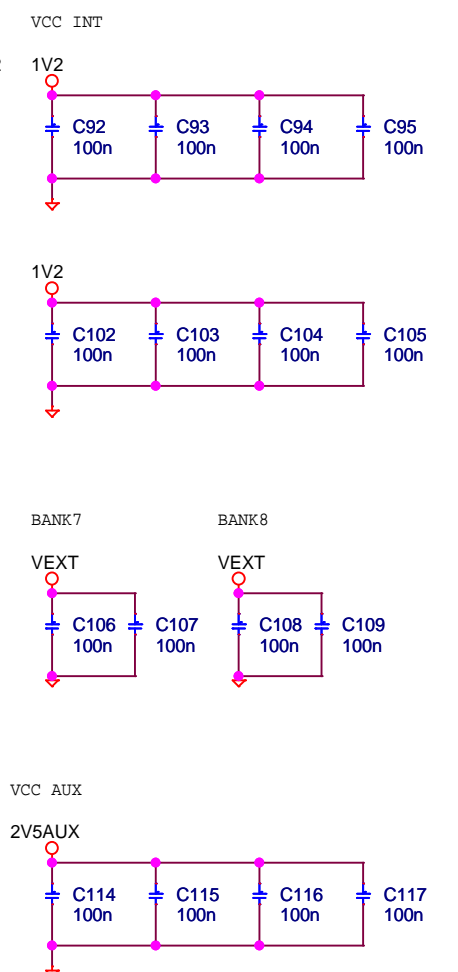
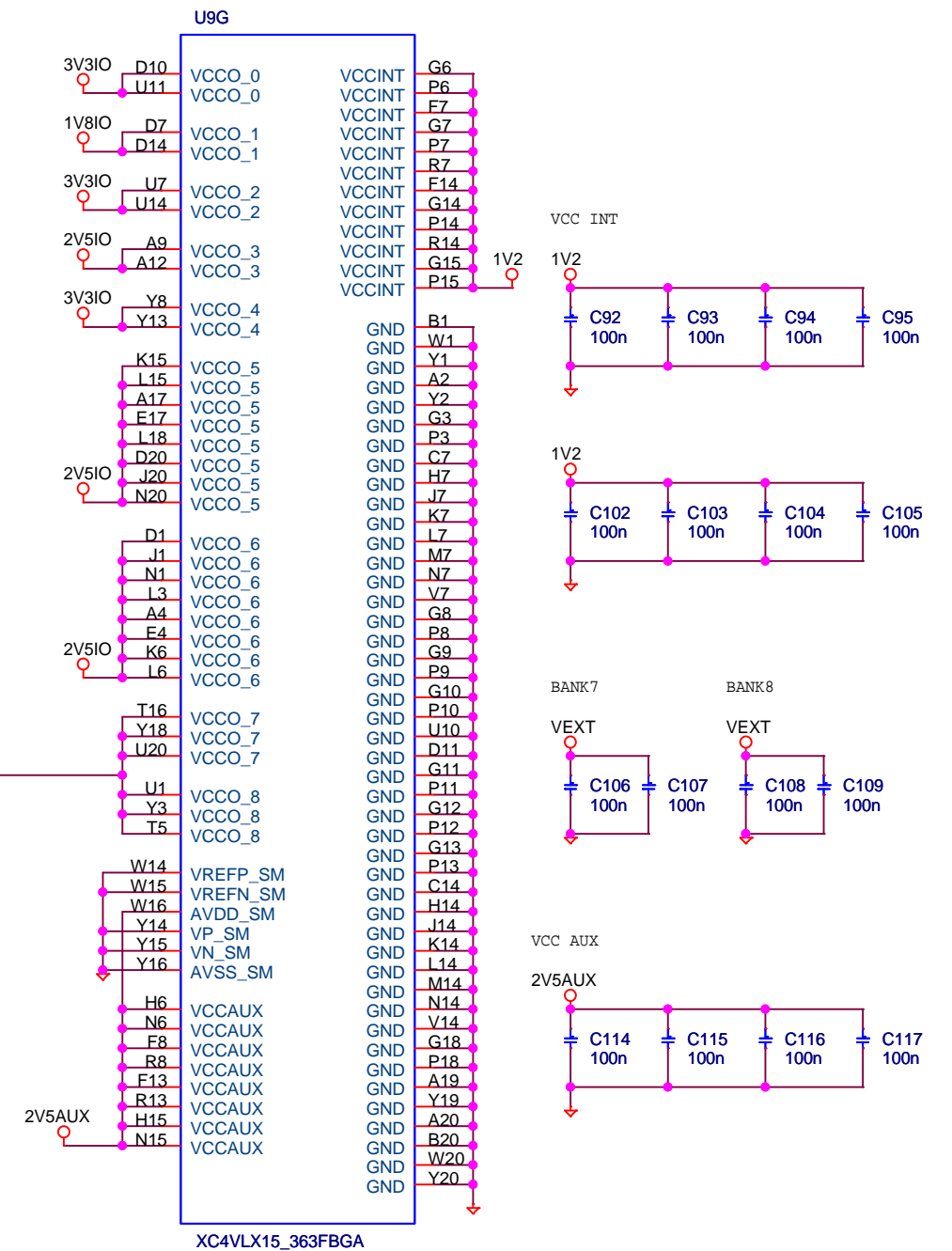
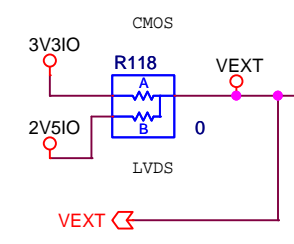
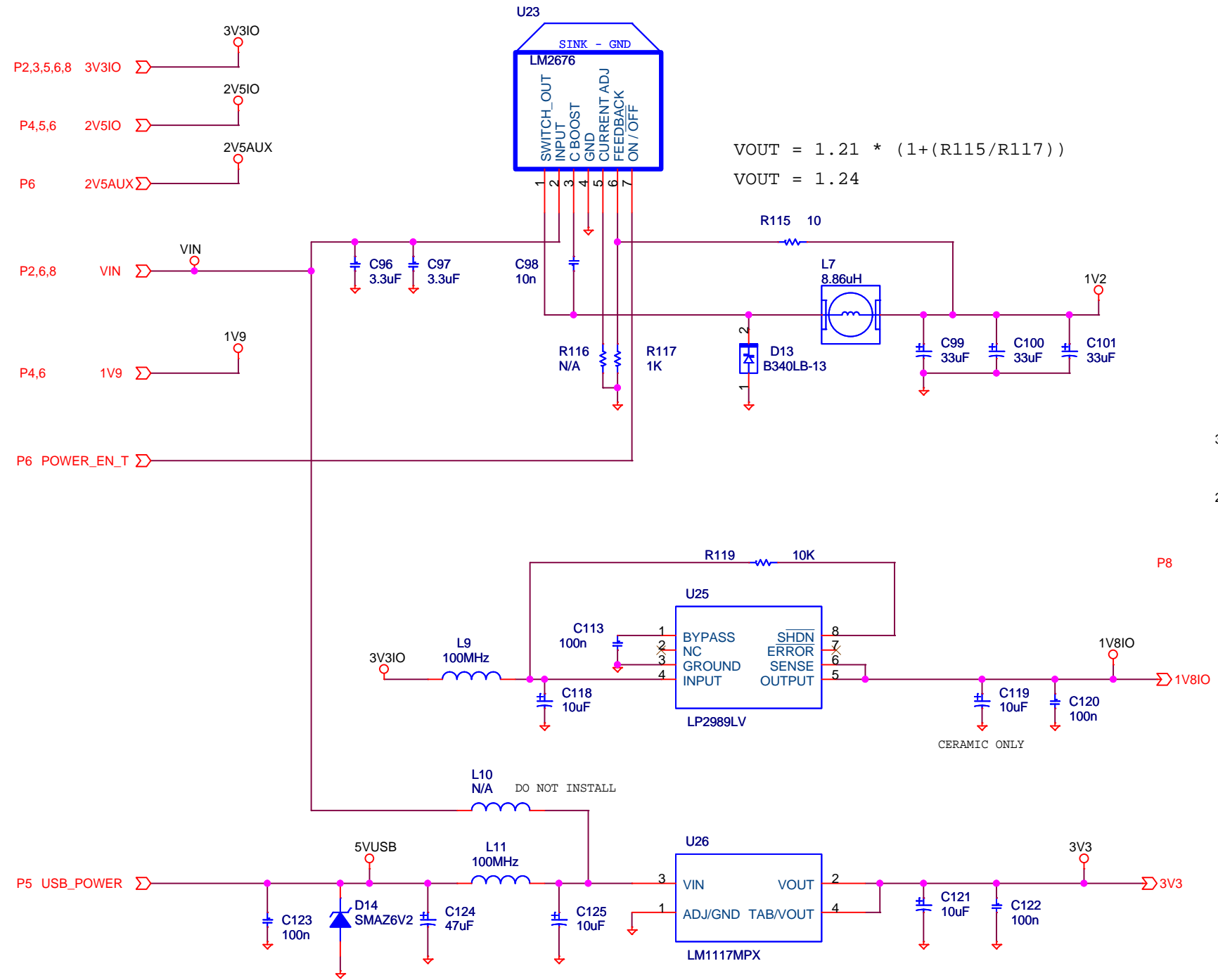
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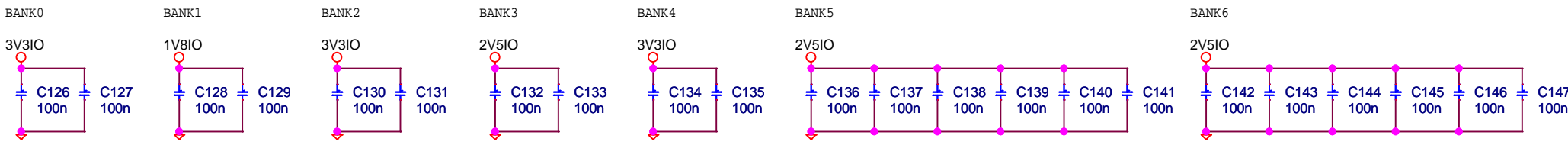


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0402 FPGA Decouplers

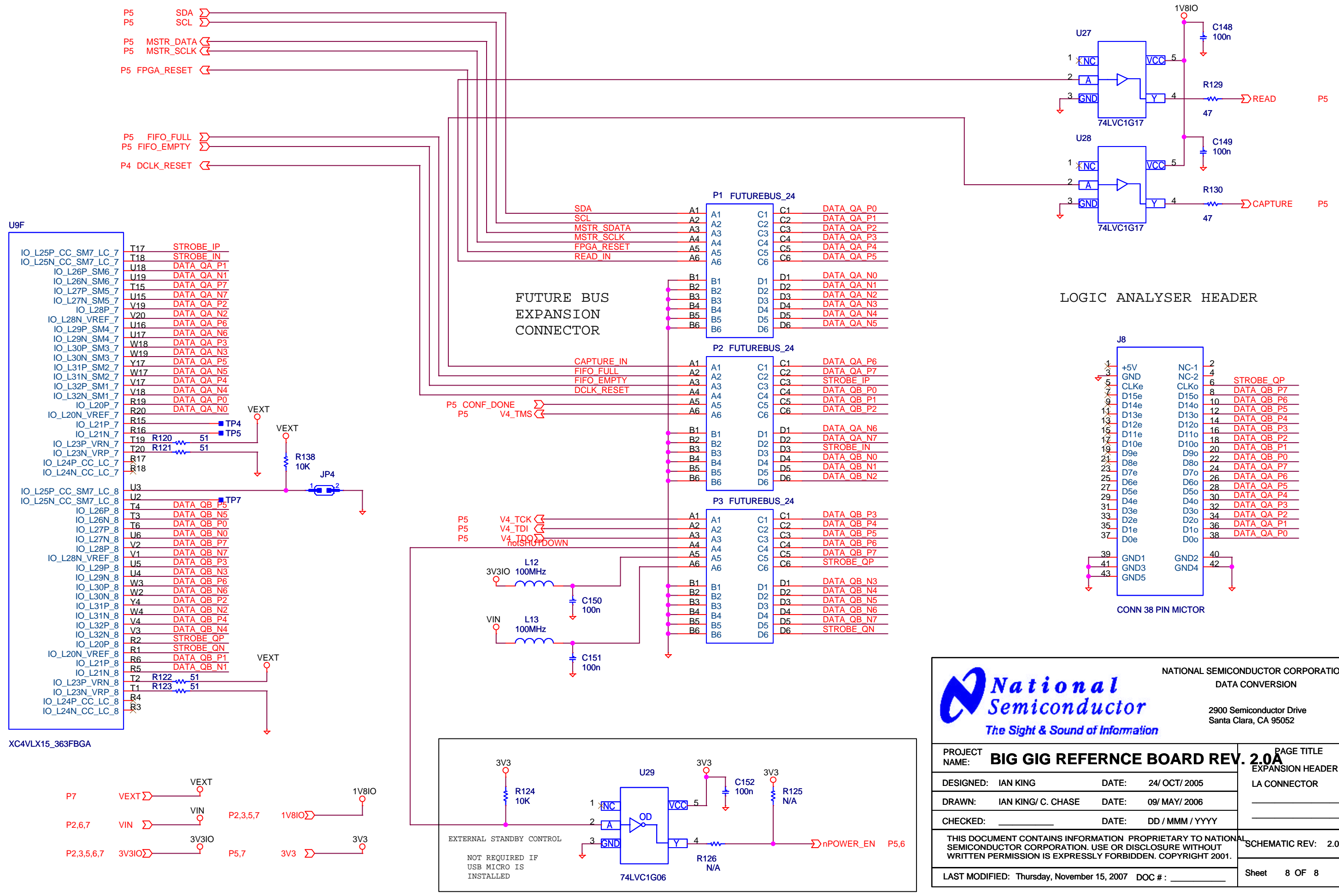


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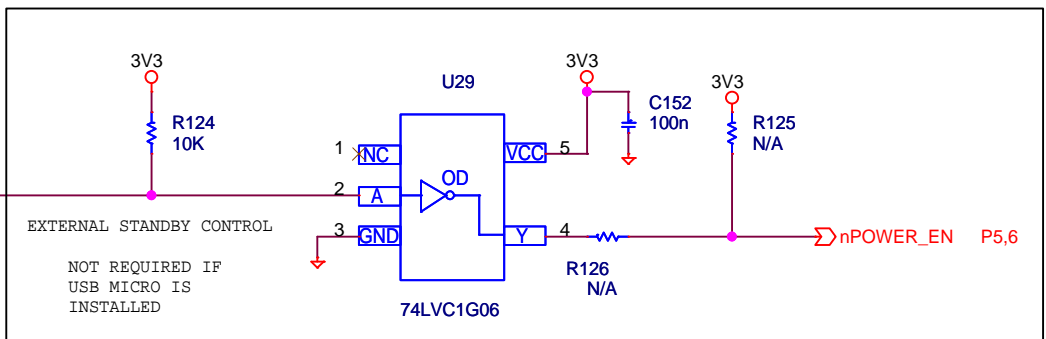
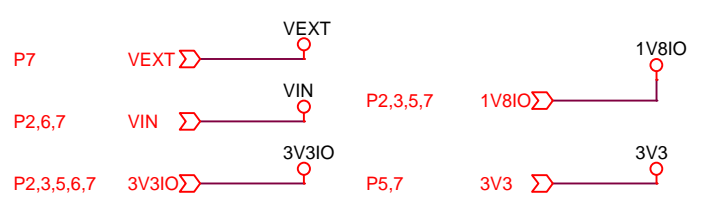
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U9F

IO_L25P_CC_SM7_LC_7	T17	STROBE_IP
IO_L25N_CC_SM7_LC_7	T18	STROBE_IN
IO_L26P_SM6_7	U18	DATA_QA_P1
IO_L26N_SM6_7	U19	DATA_QA_N1
IO_L27P_SM5_7	T15	DATA_QA_P7
IO_L27N_SM5_7	U15	DATA_QA_N7
IO_L28P_7	V19	DATA_QA_P2
IO_L28N_VREF_7	V20	DATA_QA_N2
IO_L29P_SM4_7	U16	DATA_QA_P6
IO_L29N_SM4_7	U17	DATA_QA_N6
IO_L30P_SM3_7	W18	DATA_QA_P3
IO_L30N_SM3_7	W19	DATA_QA_N3
IO_L31P_SM2_7	Y17	DATA_QA_P5
IO_L31N_SM2_7	W17	DATA_QA_N5
IO_L32P_SM1_7	V17	DATA_QA_P4
IO_L32N_SM1_7	V18	DATA_QA_N4
IO_L20P_7	R19	DATA_QA_P0
IO_L20N_VREF_7	R20	DATA_QA_N0
IO_L21P_7	R15	
IO_L21N_7	R16	
IO_L23P_VRN_7	T19	
IO_L23N_VRP_7	T20	
IO_L24P_CC_LC_7	R17	
IO_L24N_CC_LC_7	R18	
IO_L25P_CC_SM7_LC_8	U3	
IO_L25N_CC_SM7_LC_8	U2	
IO_L26P_8	T4	DATA_QB_P5
IO_L26N_8	T3	DATA_QB_N5
IO_L27P_8	T6	DATA_QB_P0
IO_L27N_8	U6	DATA_QB_N0
IO_L28P_8	V2	DATA_QB_P7
IO_L28N_VREF_8	V1	DATA_QB_N7
IO_L29P_8	U5	DATA_QB_P3
IO_L29N_8	U4	DATA_QB_N3
IO_L30P_8	W3	DATA_QB_P6
IO_L30N_8	W2	DATA_QB_N6
IO_L31P_8	Y4	DATA_QB_N2
IO_L31N_8	W4	DATA_QB_N2
IO_L32P_8	V4	DATA_QB_N4
IO_L32N_8	V3	DATA_QB_N4
IO_L20P_8	R2	STROBE_QP
IO_L20N_VREF_8	R1	STROBE_QN
IO_L21P_8	R6	DATA_QB_P1
IO_L21N_8	R5	DATA_QB_N1
IO_L23P_VRN_8	T2	
IO_L23N_VRP_8	T1	
IO_L24P_CC_LC_8	R4	
IO_L24N_CC_LC_8	R3	

XC4VLX15_363FBGA



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