



**DS40MB200-EVK**

**Signal Conditioning Mux-Buffer**

**Demo Board User Guide**

## **Introduction**

The DS40MB200 is a signal conditioning 2:1 multiplexer and 1:2 buffer designed to support port redundancy. Advanced signal conditioning features utilizing input equalization and output driver pre-emphasis enable data communication for FR4 backplane over 1-4Gb/s.

The DS40MB200 demo board is designed to assist customers to evaluate the functionality and performance. All input and output ports of the DS40MB200 are brought out to SMA connectors for accessibility to instrumentation.

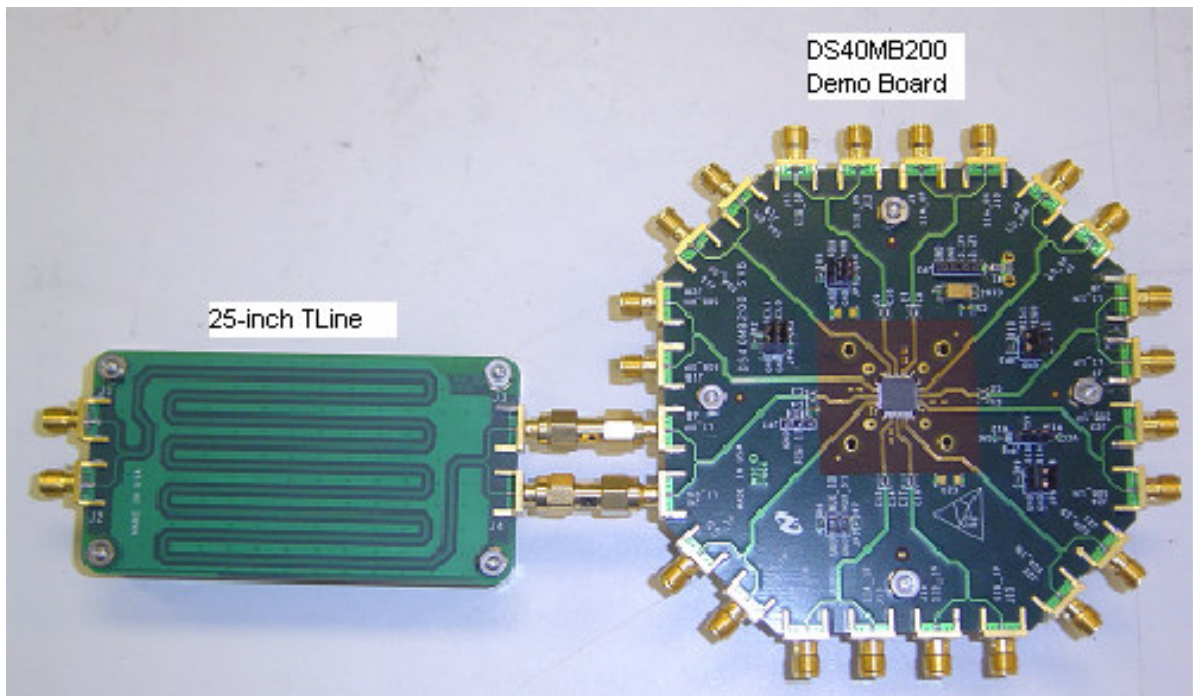
A 25-inch FR4 transmission line is provided along with the demo board to facilitate evaluation of the signal conditioning features. This 25-inch board trace has about 5dB loss from 375MHz to 1.9GHz. It is intended to use as the input transmission line to the DS40MB200, whose on-chip input equalizer is optimized to minimize the deterministic jitter caused by the input board trace. Customers can also connect the DS40MB200 to their backplanes for performance evaluation.

## **Evaluation Kit Content**

This evaluation kit consists of the following components:

- (1) DS40MB200 demo board
- (2) A 25-inch FR4 differential board trace
- (3) Demo Board User Guide (this document)
- (4) Demo board schematic

**DS40MB200 Demo Board and 25-inch TLine Board**



## Connection Diagram

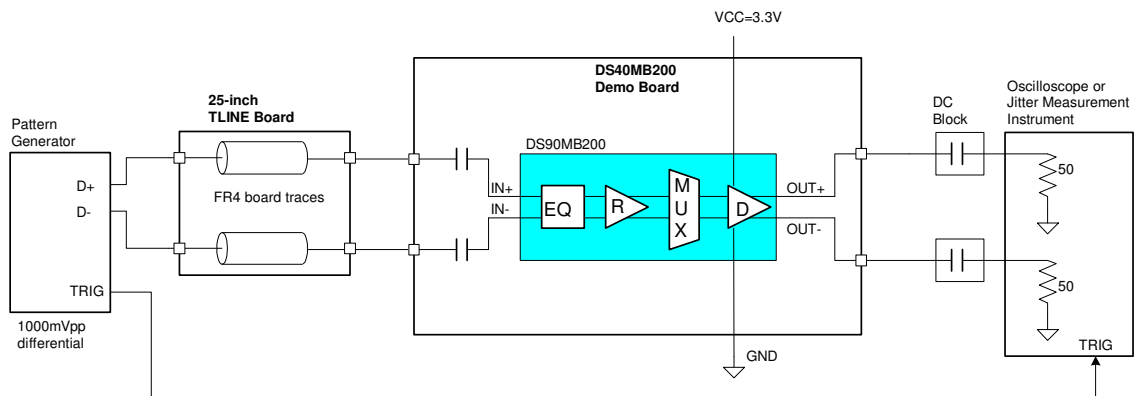


Figure 1. Typical connection for evaluation of the DS40MB200

<b>Power</b>		
VCC	JP2.3	3.3V $\pm$ 5%
GND	JP2.1	0V

<b>Pre-emphasis controls</b>		
PREL0	JP2.4	Set Pre-emphasis level for all outputs at the line side (LO_0 $\pm$ and LO_1 $\pm$ ). Open is logic 1. Strap to GND is logic 0.
PREL1	JP2.2	
PRES0	JP3.4	Set the pre-emphasis level for all outputs at the switch side (SOA_0 $\pm$ , SOB_0 $\pm$ , SOA_1 $\pm$ and SOB_1 $\pm$ ). Open is logic 1. Strap to GND is logic 0.
PRES1	JP3.2	

<b>Mux controls</b>		
MUX_S0	JP1.3	Set the multiplexer position to switch A or switch B. Open is logic 1. Strap to GND is logic 0.
MUX_S1	JP1.1	

<b>Loopback controls</b>		
LB0A	JP5.2	Enable or disable loopback. Open is logic 1.
LB0B	JP5.4	
LB1A	JP6.1	Strap to GND is logic 0.
LB1B	JB6.3	

<b>RSV control</b>		
RSV	JP8.2	Reserved for factory testing purposes. JP8.2 is permanently tied to GND.

### Logic control for data paths

Following tables list the logic states of the control pins used to configure the data paths of the DS40MB200. More detailed information about pin functions and pin descriptions can be found in the DS40MB200 datasheet.

Logic table for multiplex controls

<b>MUX_S0</b>	<i>Mux Function</i>
0	MUX_0 select switch_B input, SIB_0±.
1 (default)	MUX_0 select switch_A input, SIA_0±.

<b>MUX_S1</b>	<i>Mux Function</i>
0	MUX_1 select switch_B input, SIB_1±.
1 (default)	MUX_1 select switch_A input, SIA_0±.

Logic table for loopback controls

<b>LB0A</b>	<i>Loopback Function</i>
0	Enable loopback from SIA_0± to SOA_0±.
1	Normal mode. Loopback disabled.

<b>LB0B</b>	<i>Loopback Function</i>
0	Enable loopback from SIB_0± to SOB_0±.
1	Normal mode. Loopback disabled.

<b>LB1A</b>	<i>Loopback Function</i>
0	Enable loopback from SIA_1± to SOA_1±.
1	Normal mode. Loopback disabled.

<b>LB1B</b>	<i>Loopback Function</i>
0	Enable loopback from SIB_1± to SOB_1±.
1	Normal mode. Loopback disabled.

Line-side pre-emphasis controls

<b>PreL_[1:0]</b>	<i>Pre-emphasis level in mVpp</i>	<i>De-emphasis level in mVpp</i>	<i>Pre-emphasis in dB</i>
0 0	1200	1200	0
0 1	1200	849.53	-3
1 0	1200	600	-6
1 1	1200	425.78	-9

Switch-side pre-emphasis controls

<b>PreS_[1:0]</b>	<i>Pre-emphasis level in mVpp</i>	<i>De-emphasis level in mVpp</i>	<i>Pre-emphasis in dB</i>
0 0	1200	1200	0
0 1	1200	849.53	-3
1 0	1200	600	-6
1 1	1200	425.78	-9

### Typical output waveforms

The followings are typical eye diagrams of the DS40MB200 using the demo board connected as shown in Figure 1.

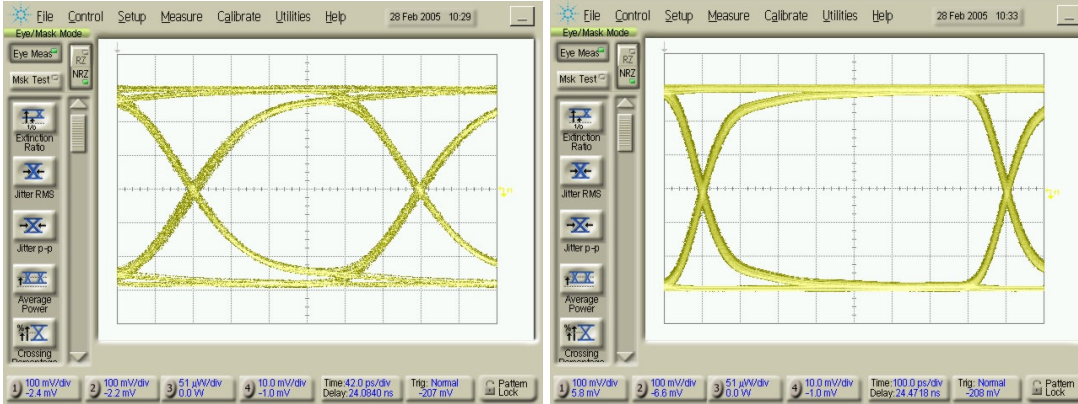


Figure 2a-b. Eye diagrams at 4 and 1.25 Gb/s, PRBS7 pattern, Pre-emphasis=0dB

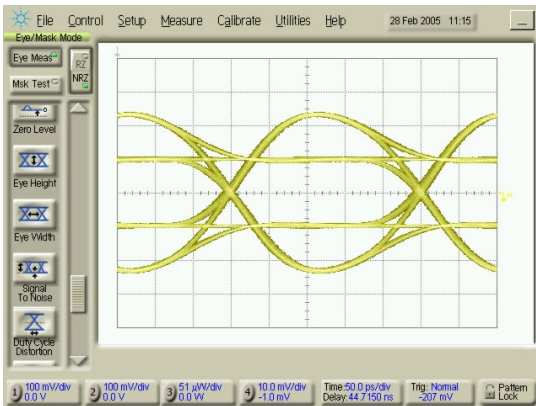


Figure 3. Eye diagram at 4 Gb/s, PRBS7 pattern, Pre-emphasis=9dB

## Reference Material

DS40MB200 datasheet

National web site <http://www.national.com/appinfo/lvds/>

# DS40MB200 demo board schematic

