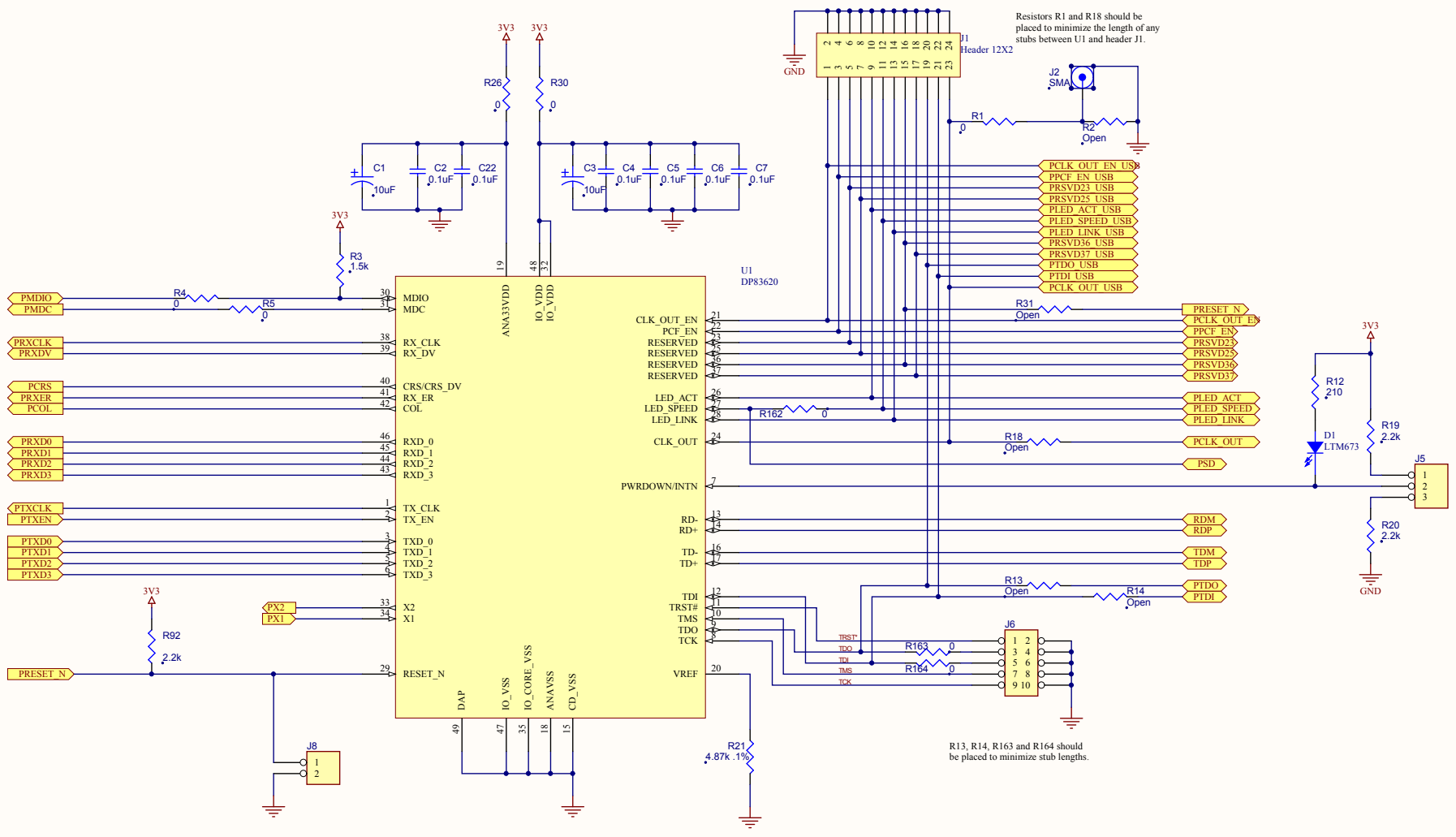


AN_EN	AN1	AN0	AUTO-NEG FORCED MODES	
0	0	0	10BASE-T	HALF-DUPLEX
0	0	1	10BASE-T	FULL-DUPLEX
0	1	0	100BASE-TX	HALF-DUPLEX
0	1	1	100BASE-TX	FULL-DUPLEX

AN_EN	AN1	AN0	AUTO-NEG ADVERTISED MODES	
1	0	0	10BASE-T	HALF/FULL-DUPLEX
1	0	1	100BASE-TX	HALF/FULL-DUPLEX
1	1	0	100BASE-TX	FULL-DUPLEX
1	1	1	10BASE-T	HALF/FULL-DUPLEX
			100BASE-TX	HALF/FULL-DUPLEX

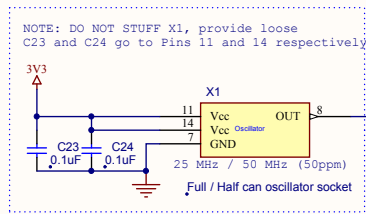
Title			
DP83620 TP&FX Demo Board - Cover			
Size	Document Number	Rev	
▲	870600596-001	1.4	
Date:	1/19/2011	Sheet	1 of 10



Resistors R1 and R18 should be placed to minimize the length of any stubs between U1 and header J1.

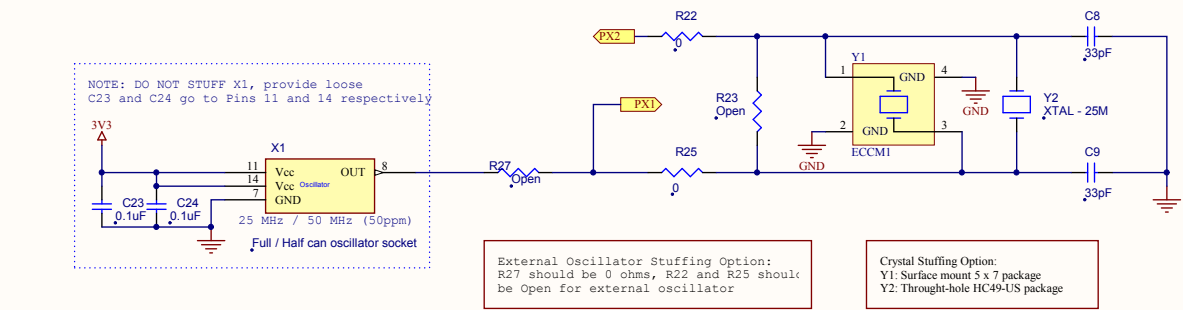
R13, R14, R163 and R164 should be placed to minimize stub lengths.

Title		
DP83620 TP&FX Demo Board - Ethernet PHY Page		
Size	Document Number	Rev
	870600596-001	1.4
Date:	1/19/2011	Sheet 2 of 10

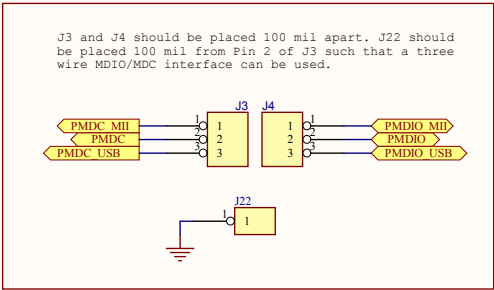
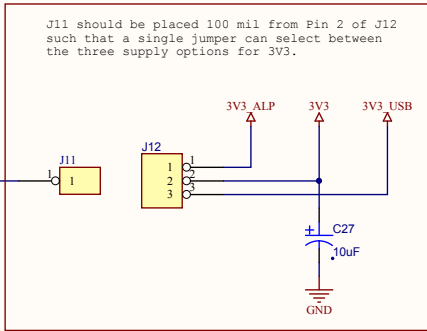


External Oscillator Stuffing Option:
R27 should be 0 ohms, R22 and R25 should be Open for external oscillator

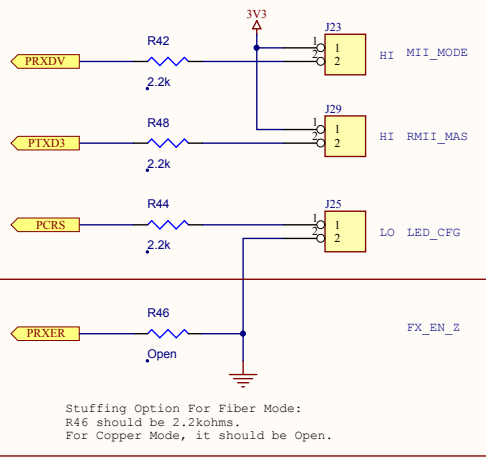
Crystal Stuffing Option:
Y1: Surface mount 5 x 7 package
Y2: Through-hole HC49-US package



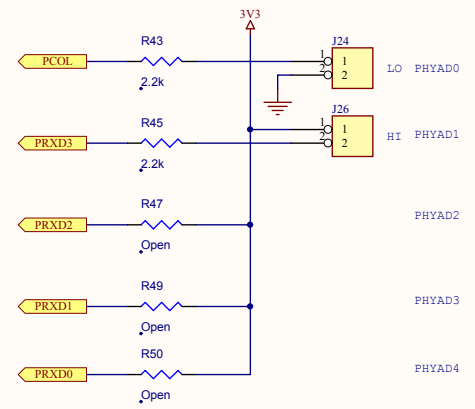
Stuffing Option:
R139 should be 0 ohms for MII Supply Operation
J55 should be shorted for 3V3 MII or Open for 5 V MII Operation



Title DP83620 TP&FX Demo Board - Power, Clock, MDIO Page		
Size A	Document Number 870600596-001	Rev 1.4
Date 1/19/2011	Sheet 3	of 10



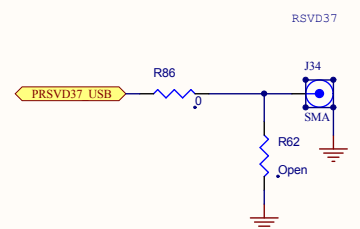
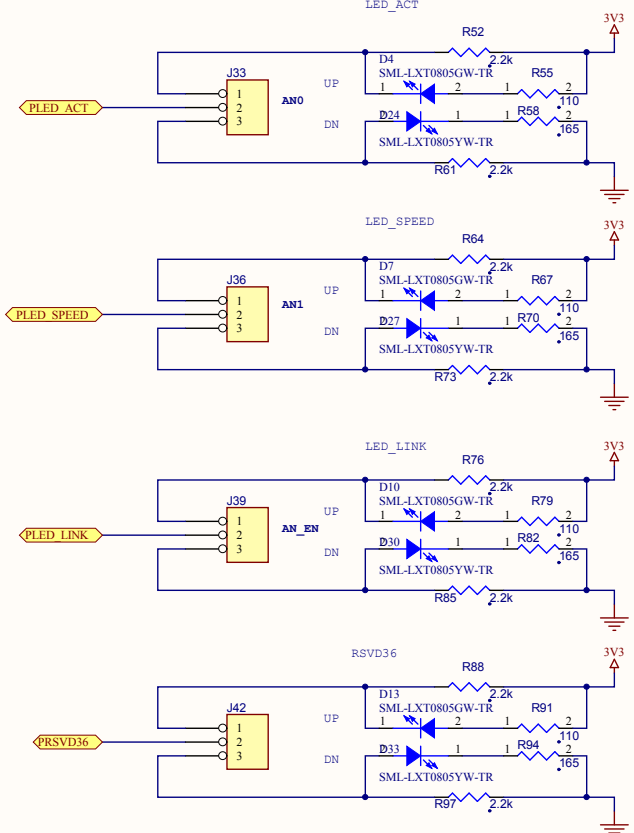
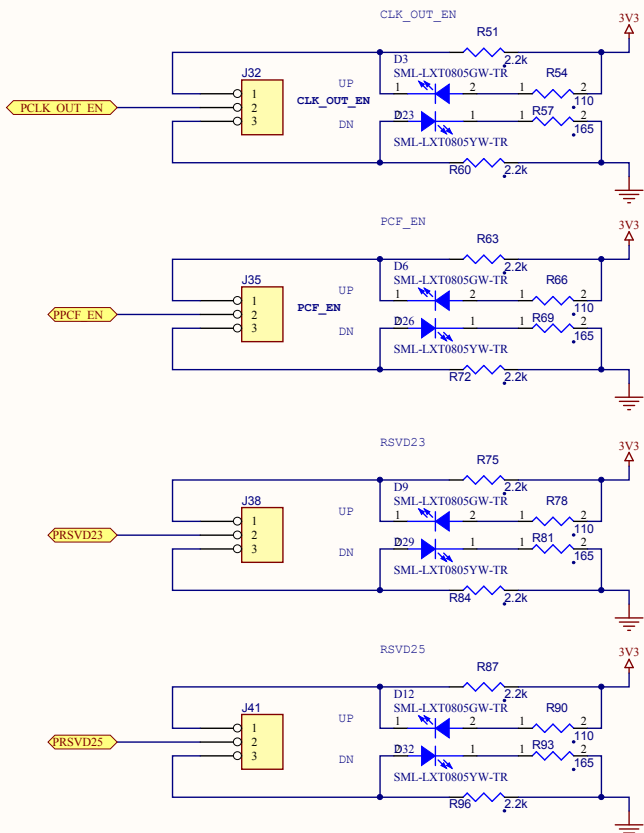
Stuffing Option For Fiber Mode:
 R46 should be 2.2kohms.
 For Copper Mode, it should be Open.



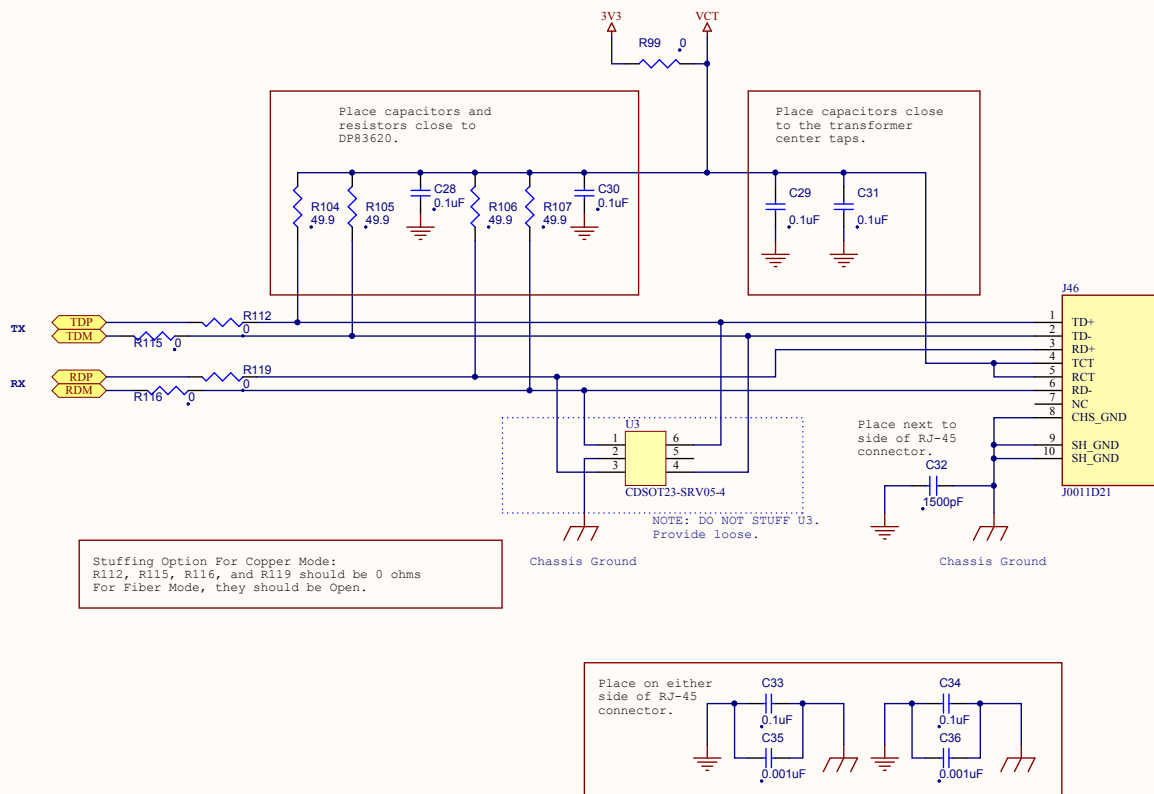
Phy Address Straps:

PHYAD1	PHYAD0	ADDRESS
0	0	0
0	1	1 (Default)
1	0	2
1	1	3

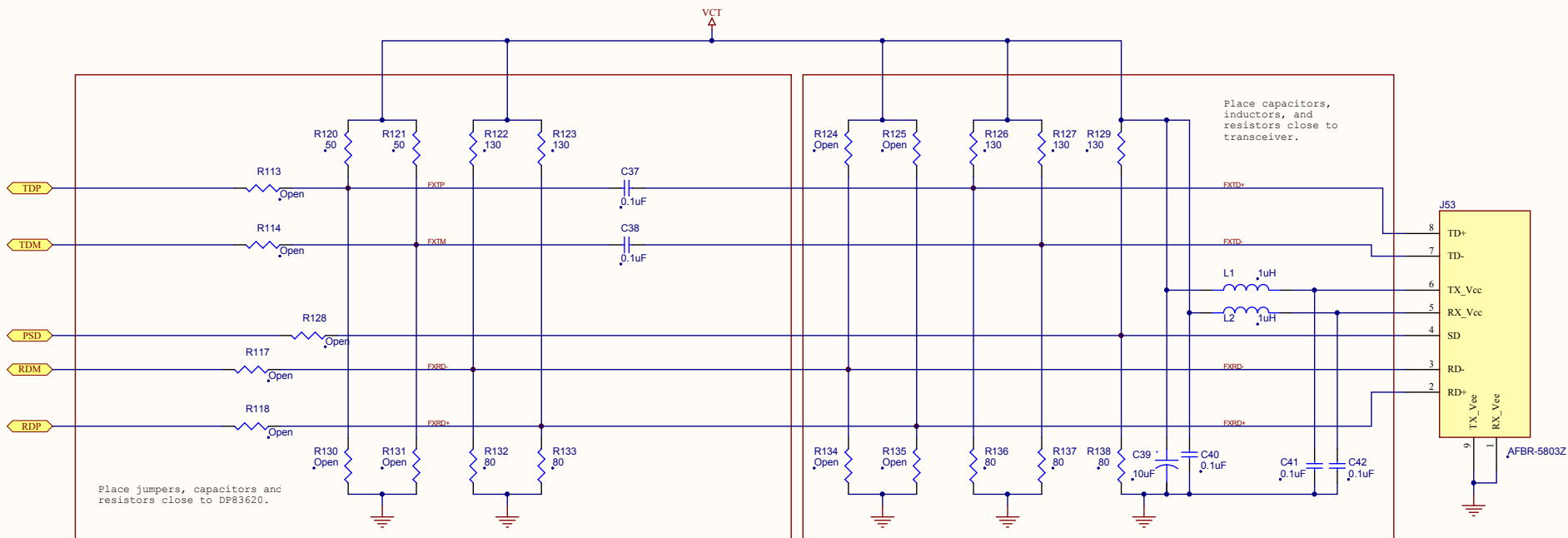
PHYAD2, PHYAD3 and PHYAD4 are internally strapped to 0.
 R47, R49 and R50 can be stuffed with 2.2kohm to allow selection of Phy addresses above 3.



Title		
DP83620 TP&FX Demo Board - Strap Options Page 2		
Size	Document Number	Rev
▲	870600596-001	1.4
Date:	1/19/2011	Sheet 5 of 10

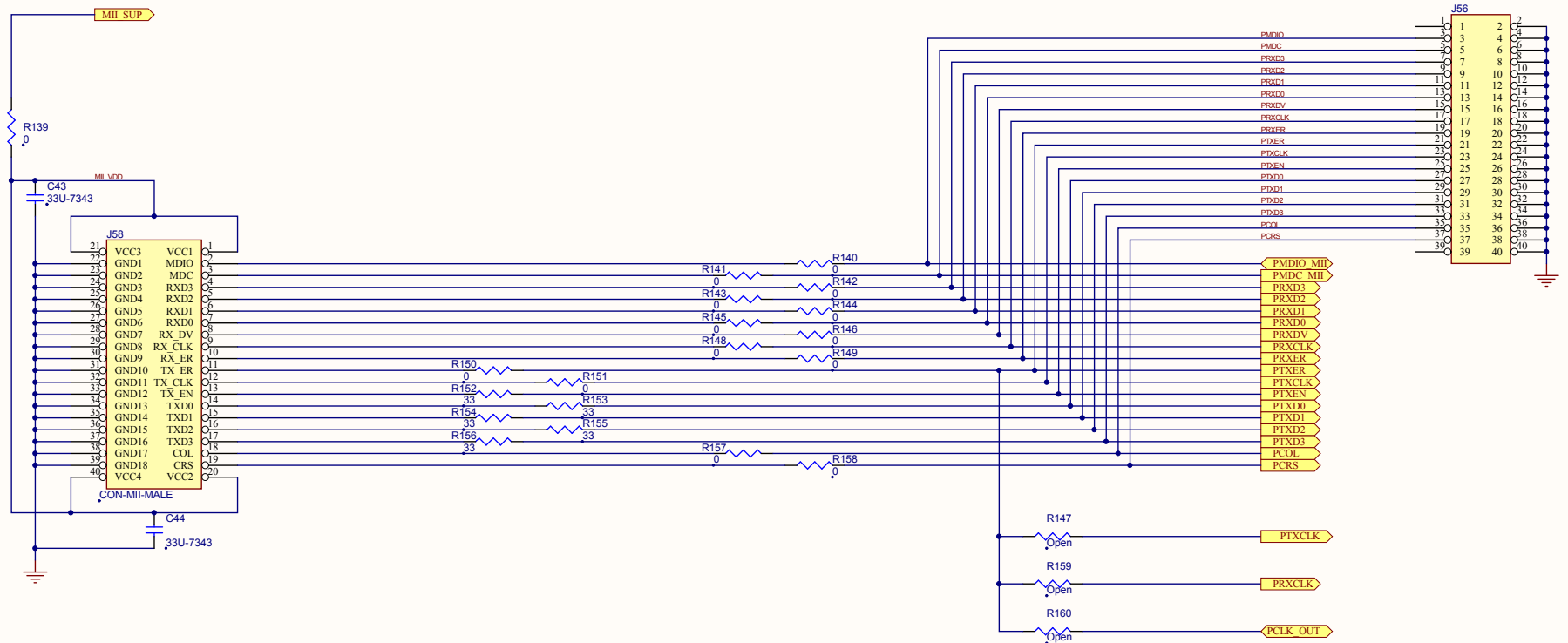


Title		DP83620 TP&FX Demo Board - TP Page	
Size	Document Number	Rev	
▲	870600596-001	1.4	
Date:	1/19/2011	Sheet	6 of 10



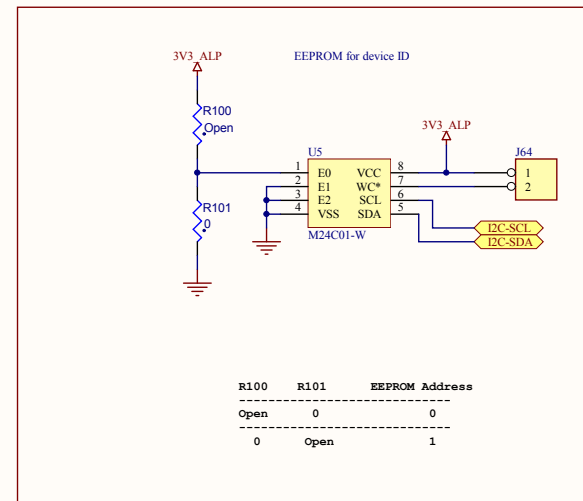
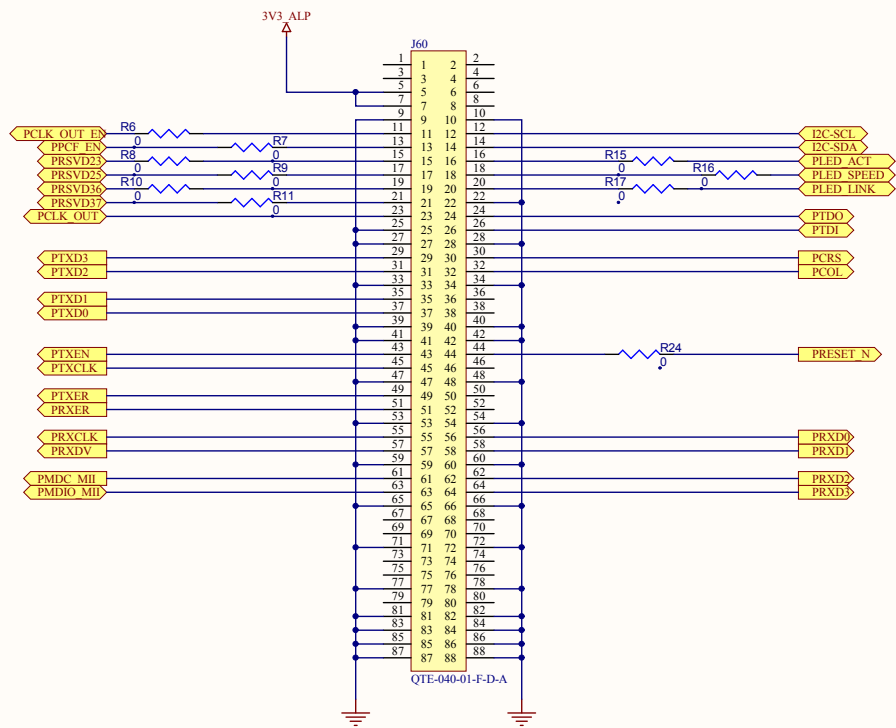
Important note:
 - R112, R115, R116, R119 are to be routed on top.
 - R113, R114, R117, R118 are to be routed on bottom.
 Stuffing option:
 For Copper Stuff: R112, R115, R116, R119
 For Fiber Stuff: R113, R114, R117, R118, R128

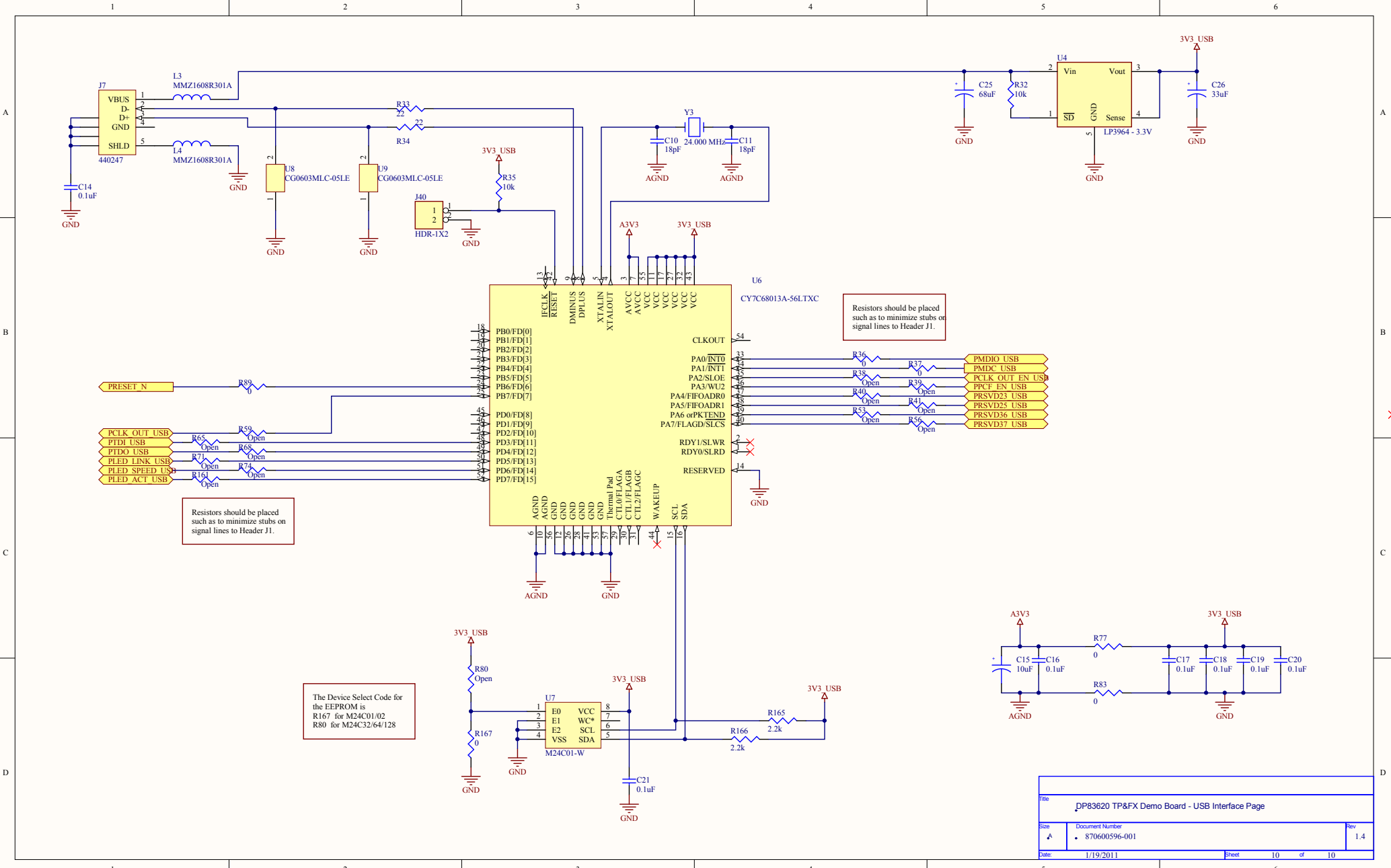
Title		
DP83620 TP&FX Demo Board - FX Page		
Size	Document Number	Rev
▲	870600596-001	1.4
Date:	1/19/2011	Sheet 7 of 10



Resistor R147, R159 and R160 should be placed close to each other.

Title		
DP83620 TP&FX Demo Board - MII Page		
Size	Document Number	Rev
1/8"	870600596-001	1.4
Date:	1/19/2011	Sheet 8 of 10





Resistors should be placed such as to minimize stubs on signal lines to Header J1.

Resistors should be placed such as to minimize stubs on signal lines to Header J1.

The Device Select Code for the EEPROM is
 R167 for M24C01/02
 R80 for M24C32/64/128

Title		
DP83620 TP&FX Demo Board - USB Interface Page		
Size	Document Number	Rev
A	870600596-001	1.4
Date:	1/19/2011	Sheet 10 of 10