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## 1.0 Introduction

This ADC12DL080 Design Kit (consisting of an Evaluation Board and this manual) is designed to ease evaluation and design-in of National Semiconductor's ADC12DL080 12-bit Analog-to-Digital Converter, which operates at speeds up to 80 Msps.

The evaluation board can be used in either of two modes. In the Manual mode suitable test equipment can be used with the board to evaluate the ADC12DL080 performance. In the Computer mode evaluation is simplified by connecting the board to the WaveVision™ Digital Interface Board (order number WAVEVSN BRD 4.0), which is connected to a personal computer through a USB port and running WaveVision™ software, operating under Microsoft Windows. The software can

perform an FFT on the captured data upon command and, in addition to a frequency domain plot, shows dynamic performance in the form of SNR, SINAD, THD and SFDR.

The signal at either of the Analog Inputs to the board is digitized and is available at J23.

## 2.0 Board Assembly

The ADC12DL080 Evaluation Board comes pre-assembled. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement and to *Section 8* for the Evaluation Board schematic.

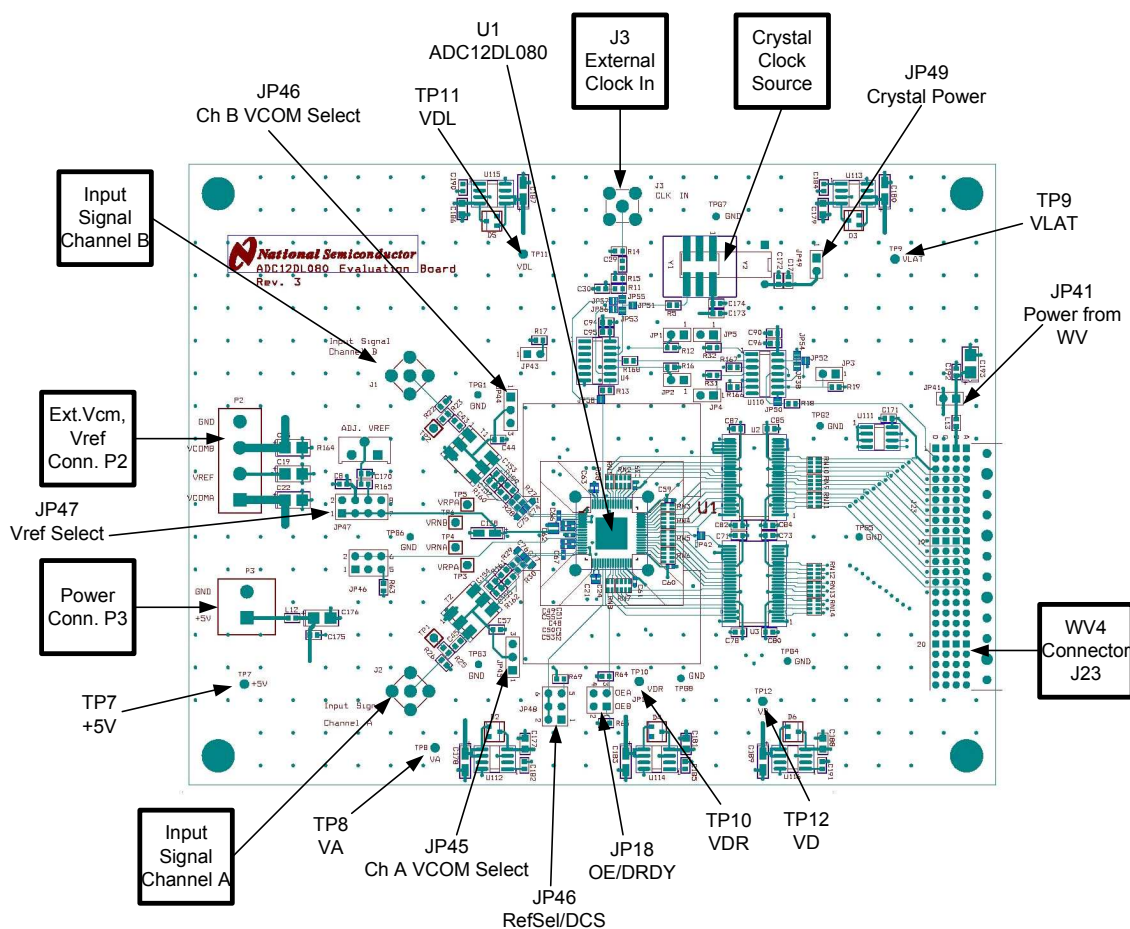


Figure 1. Component and Jumper Locations

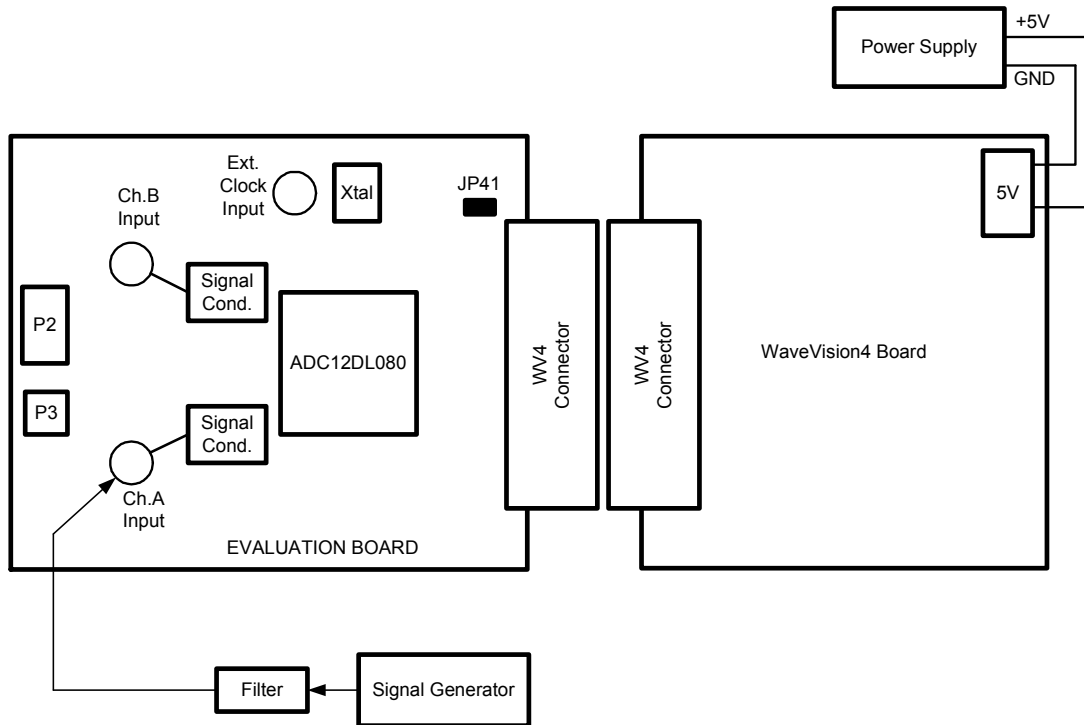


Figure 2. Test set up in Computer Mode

### 3.0 Quick Start

Refer to *Figure 1* for locations of major components. The board is configured by default to use a crystal clock source, internal 1.0V reference, and offset binary output data format. Refer to *Section 4.0* and the Appendix for more information on jumper settings.

#### For Stand-Alone operation:

1. Connect a clean +5V power supply to Power Connector P3.
2. Connect a signal from a 50-Ohm source to connector J2 (for Channel A). The ADC input signal can be observed at TP1. Because of isolation resistor R25 and the scope probe capacitance, the input signal at TP1 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
3. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data.
4. The digitized signal is available at pins B4 (MSB) through B15 (LSB) of J23. See board schematic in *Section 8*.

#### For Computer Mode operation:

You must have version 4.1.7 or later of the WaveVision™ software to properly test this board. You can download

the latest version from:

<http://www.national.com/appinfo/adc/wv4.html>

1. Connect the evaluation board to the WaveVision™ Digital Interface Board. See the WaveVision™ Board Manual for operation of that board. Connect the WaveVision™ board to the computer using a USB cable. Connect a clean +5V power supply to Power Connector J1.
2. Short jumper JP41 on the ADC12DL080 Evaluation Board. With jumper JP41 shorted, the ADC12DL080 Evaluation Board gets power from the WaveVision™ board, therefore it does not require a separate power supply. **DO NOT provide separate power supplies to the Evaluation Board and the WaveVision Board when JP41 is shorted.**
3. Connect a signal from a 50-Ohm source to connector J2 (for Channel A). The ADC input signal can be observed at TP1. Because of isolation resistor R25 and the scope probe capacitance, the input signal at TP1 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
4. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data with the WaveVision™ software.

5. Select which channel the WV4 board collects data from with the **Product Board Settings** item under the **Settings** menu. See the WaveVision™ Board Manual for instructions for gathering and analyzing data.

#### **4.0 Functional Description**

The ADC12DL080 Evaluation Board schematic is shown in *Section 8*. A list of test points and jumper settings can be found in the Appendix.

##### **4.1 Input (signal conditioning) circuitry**

The input signal to be digitized should be applied to SMA connectors J2 for Channel A or J1 for Channel B. This 50 Ohm input is intended to accept a low-noise sine wave signal of 2V peak-to-peak amplitude. To accurately evaluate the dynamic performance of this converter, the input test signal will have to be passed through a high-quality bandpass filter with at least 14-bit equivalent noise and distortion characteristics.

Signal transformers T1 and T2 provide single-ended to differential conversion. The voltage  $V_{RM}$  from the ADC, or an external voltage from connector P2 sets the common mode of the input signal by biasing the center tap of the secondary of transformer. When an external supply is used, the voltage should be set within the acceptable range of the ADC. Jumpers JP44 and JP45 select the source of the common mode voltage. Shorting pins 1-2 selects the external voltage source. The default setting is to use  $V_{RM}$  from the ADC, shorting pins 2-3.

##### **4.2 ADC Reference Circuitry**

The ADC12DL080 can use an internal 1.0V reference, or an external reference.

Shorting pins 1-2 of JP47 selects the internal 1.0V reference. This is the default setting.

Shorting pins 3-4 of jumper JP47 selects the external supply at connector P2-pin 2 as the reference source. The ADC12DL080 is specified to operate with  $V_{REF}$  in the range of 0.8 to 1.2 V, with a nominal value of 1.0V.

Shorting pins 5-6 of jumper JP47 selects the external reference from adjustable resistor R164 as the reference source.

##### **4.3 Duty Cycle Stabilizer (DCS)**

The ADC12DL080 has a clock duty cycle stabilizer that is controlled by JP46 on the Evaluation Board.

By default pins 3-4 of JP46 are shorted, and the DCS is off.

To turn on DCS, connect JP46 pins 1-2 when an external reference is used, or pins 5-6 when the internal reference is used.

##### **4.4 ADC clock circuit**

The clock circuit has a lot of options for clock source, timing, and paths. These choices are made by installing certain resistors and removing others, as well as selecting jumpers and shorting jumpers. Refer to the board schematic and Bill of Materials for more details.

By default, the board is set to use a crystal clock source to drive the ADC directly through R5.

If an external clock source is used, it should be a very low ( less than 0.5ps rms ) jitter CMOS level source.

#### **4.5 Digital Data Output**

The digitized output is available at WaveVision Connector J23. Channel A outputs are available on pins B4 (MSB) through B15 (LSB). Channel B outputs are available on pins A4 (MSB) through A15 (LSB).

#### **4.6 Power Supply Connections**

Power to this board is supplied through power connector P3. The only supply needed is +5V at pin 1 plus ground at pin 2.

When using the ADC12DL080 Evaluation Board with the the WaveVision™ Digital Interface Board, a 5V logic power supply for the interface board is passed through the WV4 connector to the Digital Interface Board when jumper JP41 is installed. **DO NOT provide separate power supplies to the Evaluation Board and the WaveVision Board when JP41 is shorted.**

#### **5.0 Installing the ADC12DL080 Evaluation Board**

The evaluation board requires power supplies as described in *Section 4.5*. When evaluating dynamic performance, an appropriate signal generator (such as the HP8644B, HP8662A or the R&S SME-03) with 50 Ohm source impedance should be connected to the Analog Input BNC J1 or J2 through an appropriate bandpass filter, as even the best signal generator available can not produce a signal pure enough to evaluate the dynamic performance of an ADC.

#### **6.0 Obtaining Best Results**

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. The layout is taken care of with the design of this evaluation board. The FFT plots shown in this section are not from an ADC14L040, however, they illustrate the points made here.

##### **6.1 Clock Jitter**

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in *Figure 3*. Compare this with the more desirable plot of *Figure 4*. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

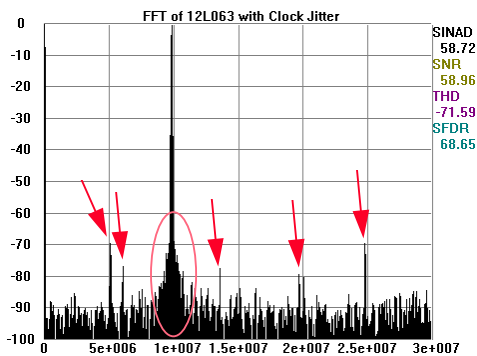


Figure 3. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

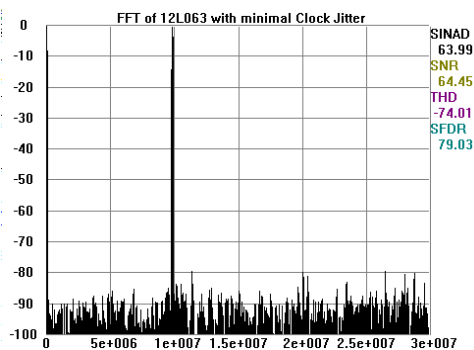


Figure 4. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

## 6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. We call this *coherent sampling*. Coherent sampling greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency ( $f_{in}$ ) and the sample rate ( $f_s$ ), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

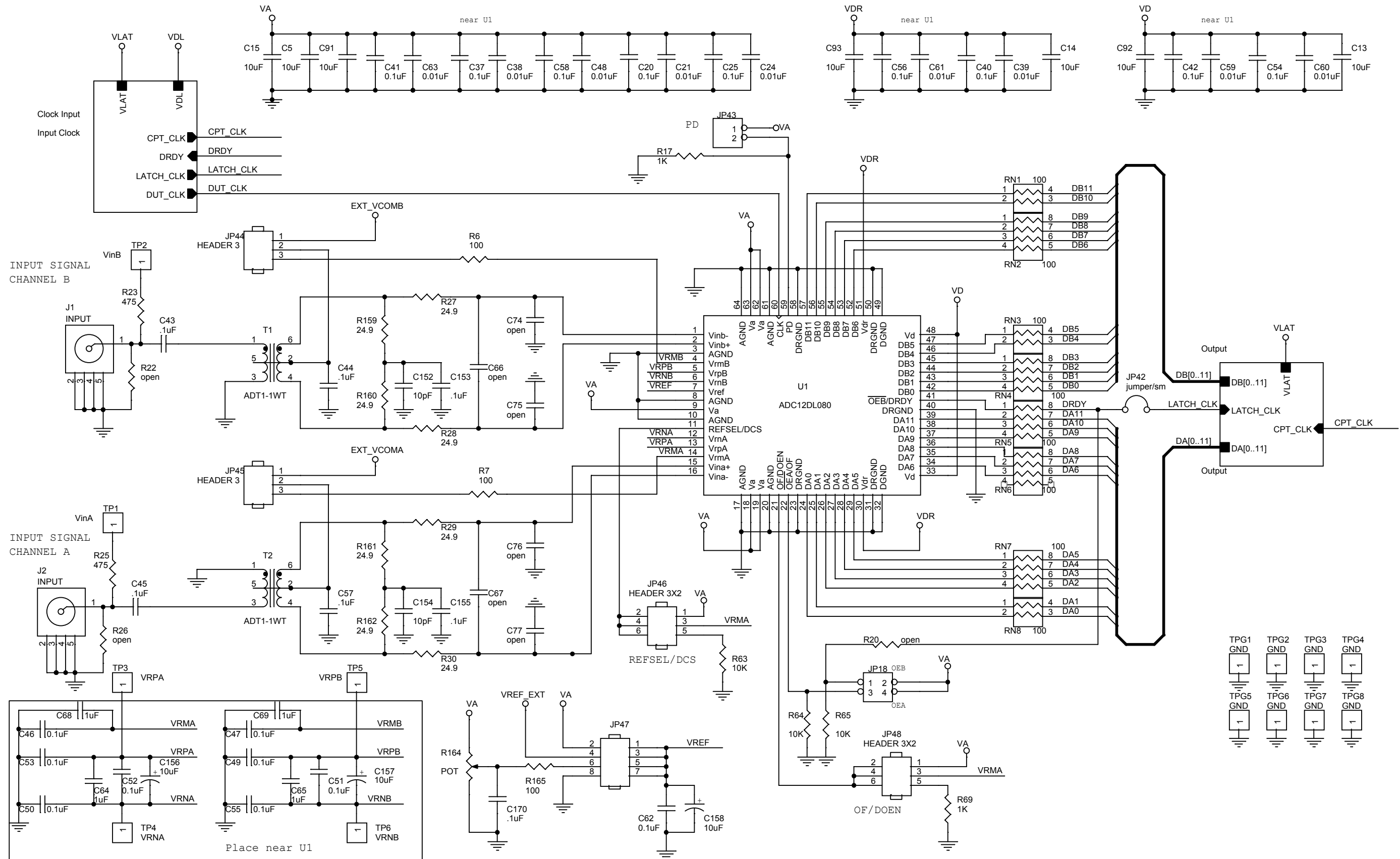
Further,  $f_{in}$  (signal input frequency) and  $f_s$  (sampling rate) should be locked to each other so that the relationship between the two frequencies is exact. Locking the two signal sources to each other also causes whatever sample-to-sample clock edge timing variation (jitter) that is present in the two signals to cancel each other.

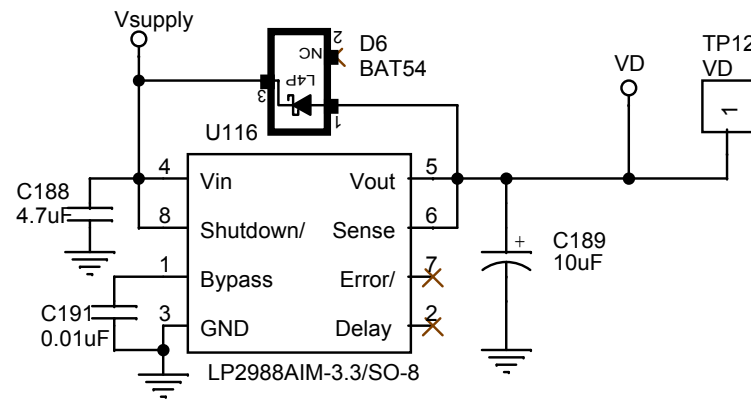
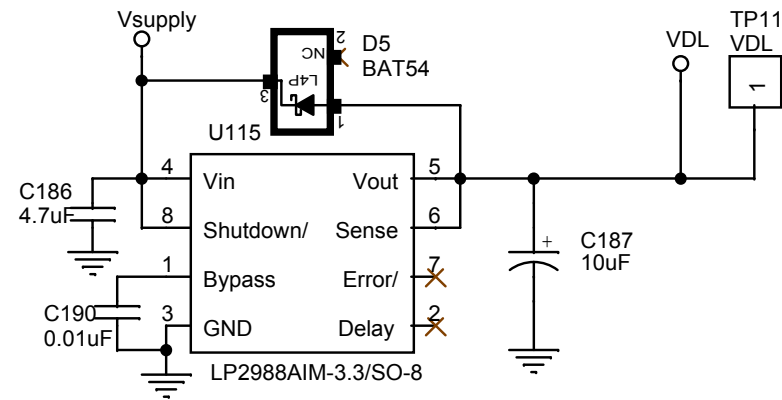
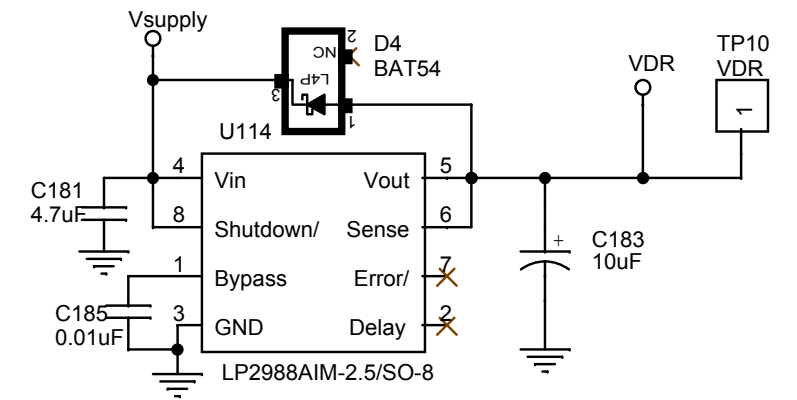
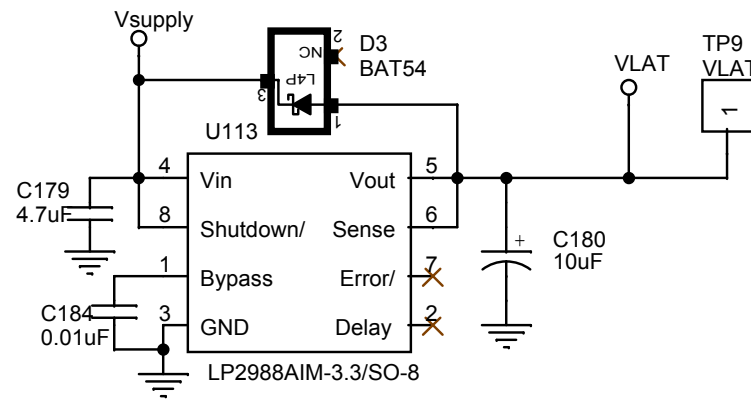
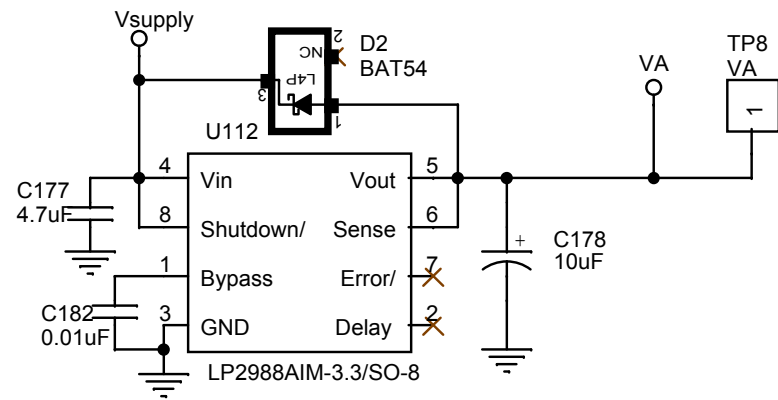
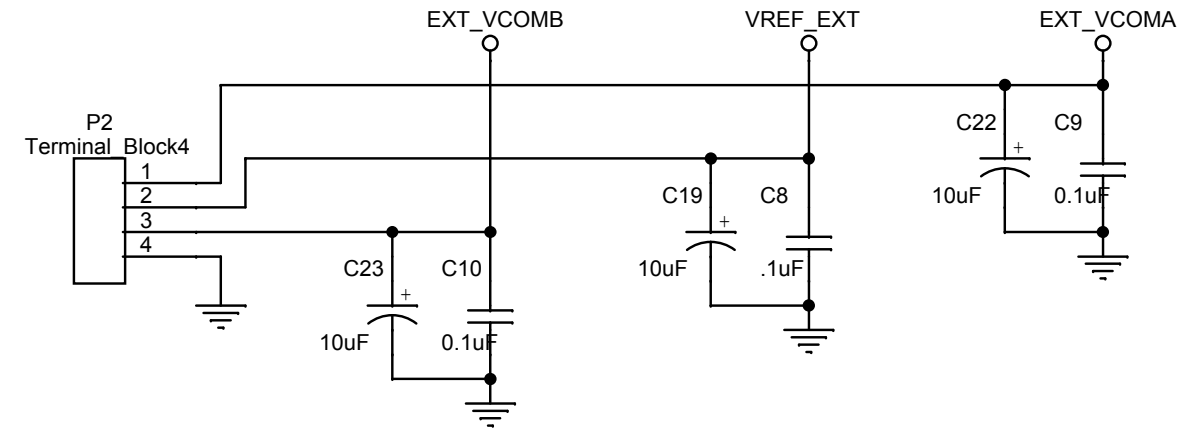
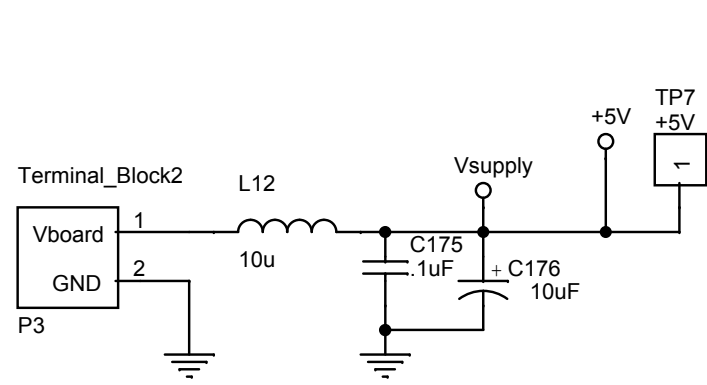
Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling.

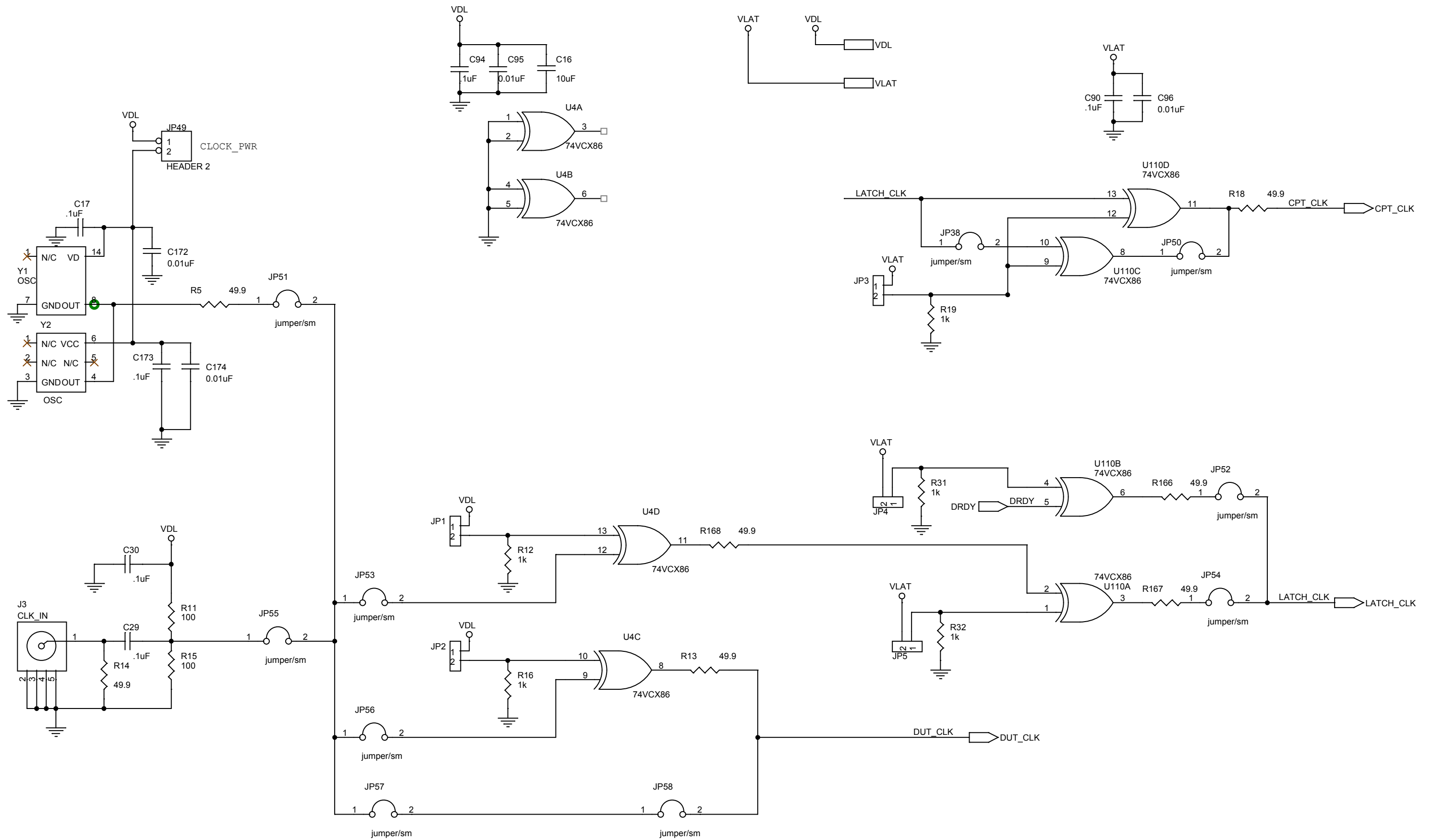
## 7.0 Evaluation Board Specifications

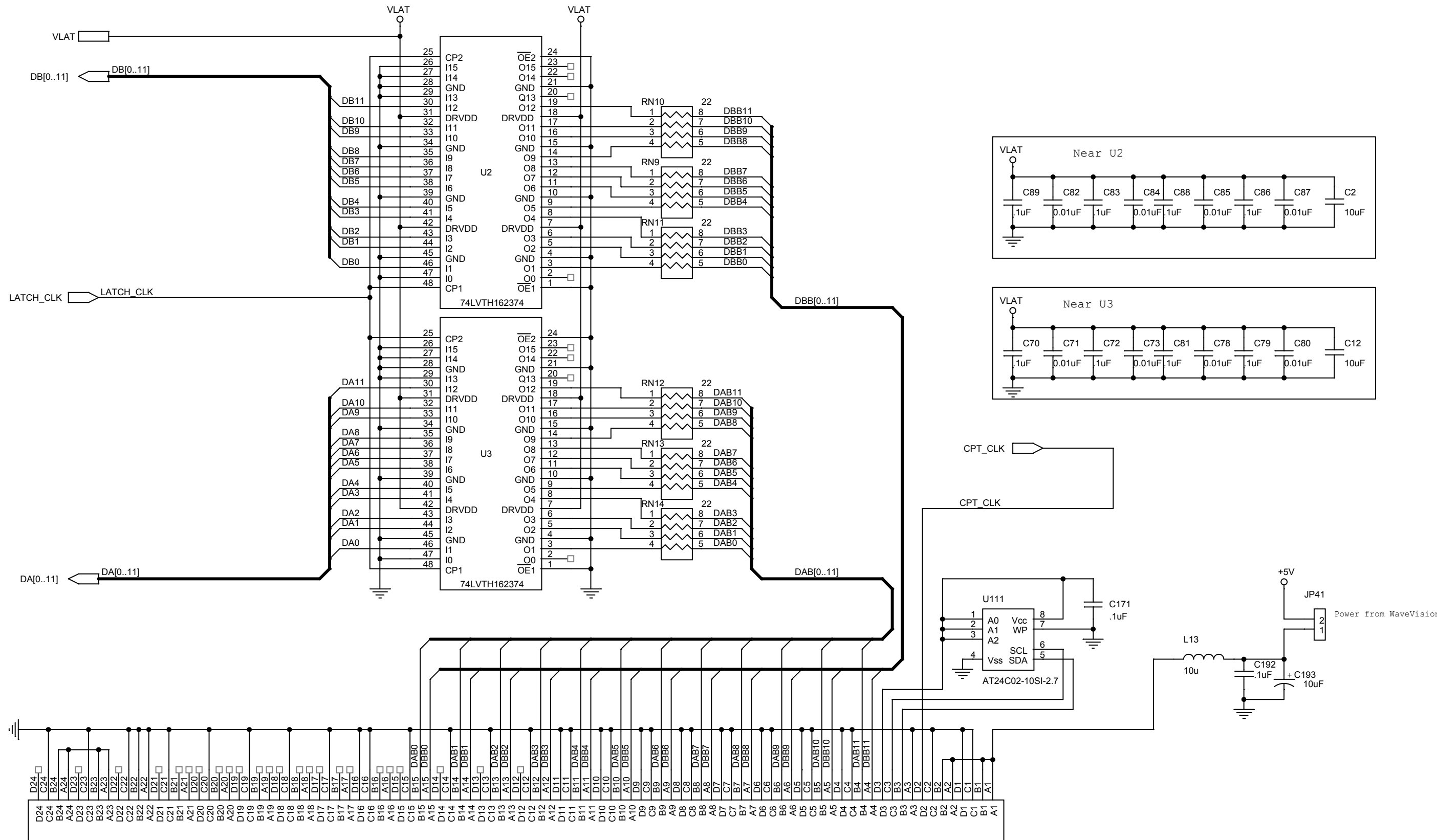
Board Size:	4.75" x 6.25"
Power Requirements:	+5.0V, 0.5 A (1A if power is shared with WaveVision Board)
Clock Frequency	80 MHz
Range:	
Analog Input	
Nominal Voltage:	2V <sub>P-P</sub>
Impedance:	50 Ohms

## 8.0 Hardware Schematic









J23  
FutureBus Connector

## 9.0 Evaluation Board Bill of Materials

Reference	Part	Part Number
C2,C5,C12,C13,C14,C15, C16,C91,C92,C93	10uF	PCC1894CT
C8,C17,C29,C30,C43,C44, C45,C57,C70,C72,C79,C81, C83,C86,C88,C89,C90,C94, C153,C155,C170,C171,C173, C175,C192	.1uF	PCC1762CT
C9,C10,C20,C25,C37,C40, C41,C42,C54,C56,C58,C62	0.1uF	PCC2188CT
C19,C22,C23,C176,C193	10uF	495-1676-1
C21,C24,C38,C39,C48,C59, C60,C61,C63	0.01uF	PCC2270CT
C46,C47,C49,C50,C51,C52, C53,C55	0.1uF	PCC2146CT
C64,C65,C68,C69	1uF	PCC2189CT
C66,C67	open	PCC150CQCT
C71,C73,C78,C80,C82,C84, C85,C87,C95,C96,C172, C174,C182,C184,C185,C190, C191	0.01uF	PCC1784CT
C74,C75,C76,C77	open	PCC100CVCT
C152,C154	10pF	PCC100CVCT
C156,C157,C158,C178,C180, C183,C187,C189	10uF	478-1751-1
C177,C179,C181,C186,C188	4.7uF	PCC1842CT
D2,D3,D4,D5,D6	BAT54	BAT54DICT
JP1,JP2,JP3,JP4,JP5,JP41	Header2	S929647-09-2
JP18	HEADER 2X2_0	S929665-09-2
JP38,JP42,JP50,JP51,JP52, JP53,JP54,JP55,JP56,JP57, JP58	jumper/sm	N/A
JP43	HEADER 2	S929647-09-2
JP44,JP45	HEADER 3	S929647-09-3
JP46,JP48	HEADER 3X2	S929665-09-3
JP47	HEADER 4X2	S929665-09-4
JP49	HEADER 2	S929647-09-2
J1,J2	INPUT	ARFX1231
J3	CLK_IN	ARFX1231
J23	FutureBus Connector	223514-1 (x4)
L12,L13	10u	0603CS-10NXJBU
P2	Terminal_Block4	277-1265
P3	Terminal_Block2	277-1263
RN1,RN3,RN8	100	Y2101CT
RN2,RN4,RN5,RN6,RN7	100	Y4101CT
RN9,RN10,RN11,RN12,RN13,	22	Y4220CT

RN14		
R5,R13,R14,R18,R166,R167, R168	49.9	P49.9HCT
R6,R7,R11,R15,R165	100	P100HCT
R12,R16,R17,R19,R31,R32, R69	1k	P1.00KHCT
R20	open	
R22,R26	open	
R23,R25	475	P475HCT
R27,R28,R29,R30,R159, R160,R161,R162	24.9	P24.9HCT
R63,R64,R65	10K	P10.0KHCT
R164	POT	3296Y-103
TPG1,TPG2,TPG3,TPG4,TPG5 ,	GND	S929647-09-1
TPG6,TPG7,TPG8		
TP1	VinA	S929647-09-1
TP2	VinB	S929647-09-1
TP3,TP5	VRPA	S929647-09-1
TP4	VRNA	S929647-09-1
TP6	VRNB	S929647-09-1
TP7	+5V	5002K
TP8	VA	5002K
TP9	VLAT	5002K
TP10	VDR	5002K
TP11	VDL	5002K
TP12	VD	5002K
T1,T2	ADT1-1WT	ADT1-1WT+
U1	ADC12DL080	ADC12DL080
U2,U3	74LVTH162374	296-14929-1
U4,U110	74VCX86	74VCX86M
U111	AT24C02-10SI-2.7	AT24C02AN-10SI-2.7
U112,U113,U115,U116	LP2988AIM-3.3/SO-8	LP2988AIM-3.3
U114	LP2988AIM-2.5/SO-8	LP2988AIM-2.5
Y1	OSC	
Y2	OSC	Pletronics SM7745DV-80.0M-Y9



## APPENDIX

### A1.0 Test Points

TP 1	Signal Input test point (Input Signal A)
TP 2	Signal Input test point (Input Signal B)
TP 3	Reference buffer VRPA
TP 4	Reference buffer VRNA
TP 5	Reference buffer VRPB
TP 6	Reference buffer VRNB
TP7	+5V
TP8	VA
TP9	VLAT
TP10	VDR
TP11	VDL
TP12	VD
TPG1 – TPG8	ADC Ground

### A1.1 Power Connectors

#### P2 Connector – External Reference and Vcm Supply Connections

P2-1	EXT_VCOMA	1.5V	External Common mode voltage for Channel A
P2-2	EXT_REF	1.0V	External reference voltage ADC
P2-3	EXT_VCOMB	1.5V	External Common mode voltage for Channel B
P2-4	GND		Power Supply Ground

#### P3 Connector - Power Supply Connections

P3-1	+5V	+5V Supply
P3-2	GND	Power Supply Ground

### A1.2 Jumper settings

Note: Default settings are in **bold**

#### Jumper JP1: Select Inverting or Non-inverting Gate

Connect 1-2	Makes the XOR gate inverting
<b>1-2 OPEN</b>	<b>Makes the XOR gate non-inverting</b>

#### Jumper JP2: Select Inverting or Non-inverting Gate

Connect 1-2	Makes the XOR gate inverting
<b>1-2 OPEN</b>	<b>Makes the XOR gate non-inverting</b>

#### Jumper JP3: Select Inverting or Non-inverting Gate

<b>Connect 1-2</b>	<b>Makes the XOR gate inverting</b>
1-2 OPEN	Makes the XOR gate non-inverting

#### Jumper JP4: Select Inverting or Non-inverting Gate

Connect 1-2	Makes the XOR gate inverting
<b>1-2 OPEN</b>	<b>Makes the XOR gate non-inverting</b>

**Jumper JP5: Select Inverting or Non-inverting Gate**

Connect 1-2	Makes the XOR gate inverting
<b>1-2 OPEN</b>	<b>Makes the XOR gate non-inverting</b>

**Jumper JP18: NOTE : JP18 is used in conjunction with JP48, see datasheet for more details**

**If DRDY output is enabled (pins 3-4 are connected on JP48) then JP18 sets the output format**

Connect 1-2	Output format is 2's complement
<b>1-2 OPEN</b>	<b>Output format is offset binary</b>

**If DRDY output is disabled (pins 1-2 or 5-6 are connected on JP48) then JP18 is the Output Enable**

Connect 1-2	Channel B outputs are disabled
1-2 Open	Channel B outputs are enabled
Connect 3-4	Channel A outputs are disabled
3-4 OPEN	Channel A outputs are Enabled

**JP41: Wavevision Power (when used with WaveVision™ 4.0 Digital Interface Board**

Connect 1-2	A +5V supply is applied to the WaveVision Board or the ADC12DL080 Board, but not both
<b>1-2 OPEN</b>	<b>Separate supplies are used for the WaveVision Board and the ADC12DL080 Board</b>

**Jumper JP43: Power Down**

Connect 1-2	Put ADC in Power Down mode
<b>1-2 OPEN</b>	<b>ADC is in normal operation</b>

**Jumper JP44: Channel B Common Mode Voltage selection jumper settings**

Connect 1-2	Use external voltage source from P2-pin3 as common mode voltage
<b>Connect 2-3</b>	<b>Use common mode voltage from ADC</b>

**Jumper JP45: Channel A Common Mode Voltage selection jumper settings**

Connect 1-2	Use external voltage source from P2-pin1 as common mode voltage
<b>Connect 2-3</b>	<b>Use common mode voltage from ADC</b>

**Jumper JP46: REFSEL/DCS – NOTE : JP46 is used in conjunction with JP47, see datasheet for more details**

Connect 1-2	External reference is used, DCS is ON (JP47 must be set to Connect 3-4 or 5-6)
<b>Connect 3-4</b>	<b>DCS is OFF</b>
Connect 5-6	Internal 1.0V Reference is selected, DCS is ON (JP47 must be set to Connect 1-2)

**Jumper JP47: VREF Select - NOTE : JP47 is used in conjunction with JP46, see datasheet for more details**

<b>Connect 1-2</b>	<b>Internal 1.0V reference is used</b>
Connect 3-4	Use external reference from P2-pin 2
Connect 5-6	Use external reference from variable resistor R164
Connect 7-8	Not used

**Jumper JP48:OF/DOEN - NOTE : JP48 is used in conjunction with JP18, see datasheet for more details**

Connect 1-2	Output format is 2's complement (DRDY output is not available)
<b>Connect 3-4</b>	<b>DRDY output is available on pin 41</b>
Connect 5-6	Output format is offset binary (DRDY output is not available)

### **Jumper JP49: Crystal power supply**

<b>Connect 1-2</b>	<b>Apply power to crystal</b>
1-2 OPEN	No power to crystal, external clock source is required

### **A1.3 Clock Circuit Solder Jumper settings**

Solder jumpers are used to select the path of the clock to the ADC, the latches, and the capture device at J23. While not as convenient as pin-type jumpers, these introduce less distortion into the clock signal.

#### **By default the following jumpers are OPEN:**

JP42, JP53, JP54, JP55, JP57, JP58

#### **By default the following jumpers are shorted:**

JP38, JP50, JP51, JP52, JP56

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2. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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