

Evaluation Board Instruction Manual

ADC10DL065, 10-Bit, 65 Mps, 3.3V A/D Converter

ADC12DL040, 12-Bit, 40 Mps, 3.0V A/D Converter

ADC12DL065, 12-Bit, 65 Mps, 3.3V A/D Converter

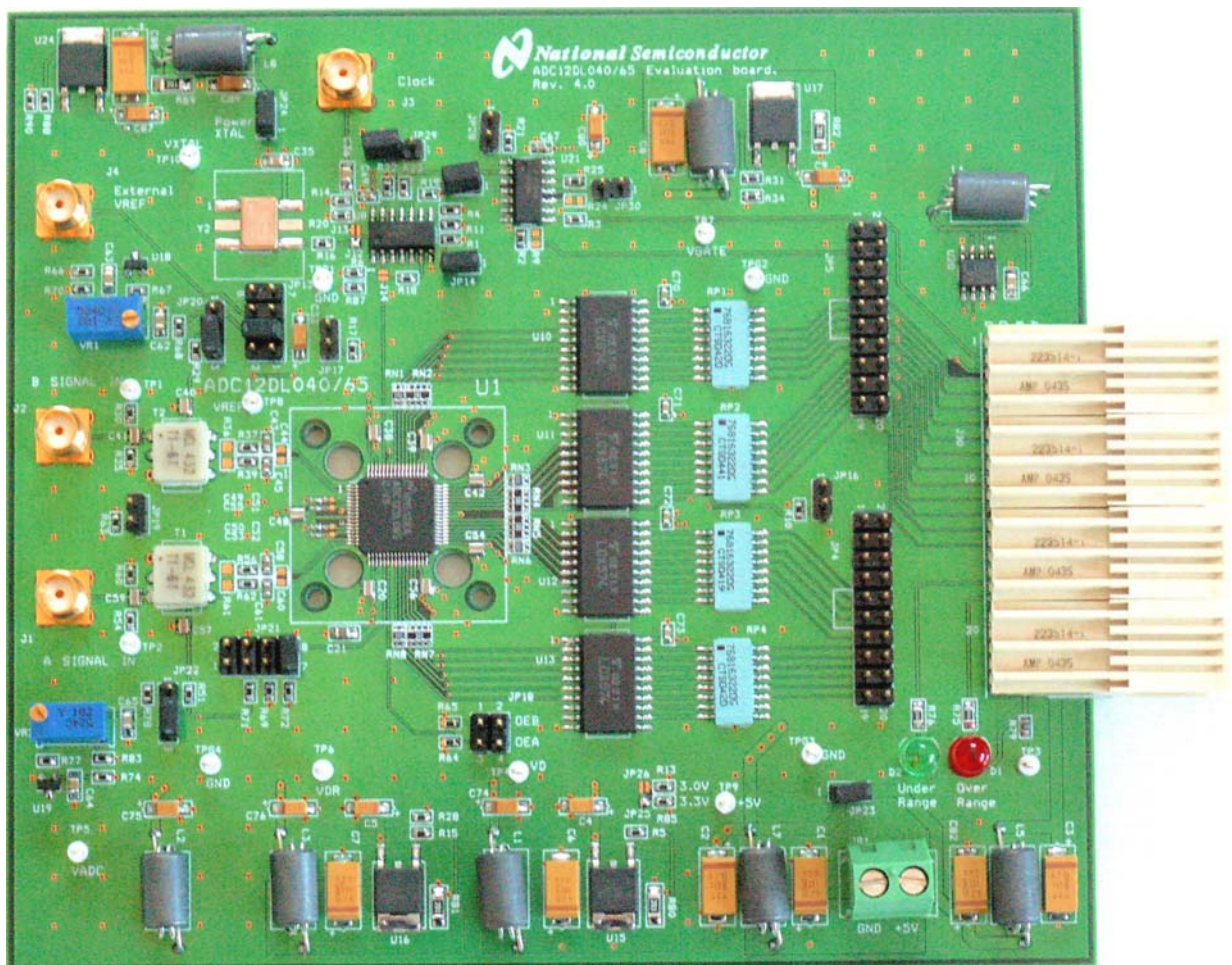


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1.0 Introduction

This Design Kit (consisting of an Evaluation Board and this manual) is designed to ease evaluation and design-in of National Semiconductor's ADC10DL065, ADC12DL040, or ADC12DL065 Analog-to-Digital Converters. Further reference in this manual to the ADC12DL040 is meant to also include the ADC10DL065 and ADC12DL065 unless otherwise specified.

The evaluation board can be used in either of two modes. In the Manual mode suitable test equipment can be used with the board to evaluate the ADC12DL040 performance. In the Computer mode evaluation is simplified by connecting the board to the WaveVision™ Digital Interface Board (order number WAVEVSN BRD 4.0), which is connected to a personal computer through a USB port and running WaveVision™ software, operating under Microsoft Windows. The software can perform an FFT on the captured data upon command and, in addition to a frequency domain plot, shows

dynamic performance in the form of SNR, SINAD, THD and SFDR.

The digital output data from Channel A of the ADC12DL040 is available at pins A4 (MSB) through A15 of the WaveVision™ (WV4) connector J10 and pins 8 (MSB) through 19 of header JP4. Channel B output data is available at pins B4 (MSB) through B15 of the WV4 connector J10 and pins 8 (MSB) through 19 of header JP5. Disregard the two LSB's for the ADC10DL065.

2.0 Board Assembly

The ADC12DL040 Evaluation Board comes pre-assembled. Refer to the Bill of Materials in Section 10 for a description of components, to Figure 1 for major component placement and to Section 8 for the Evaluation Board schematic.

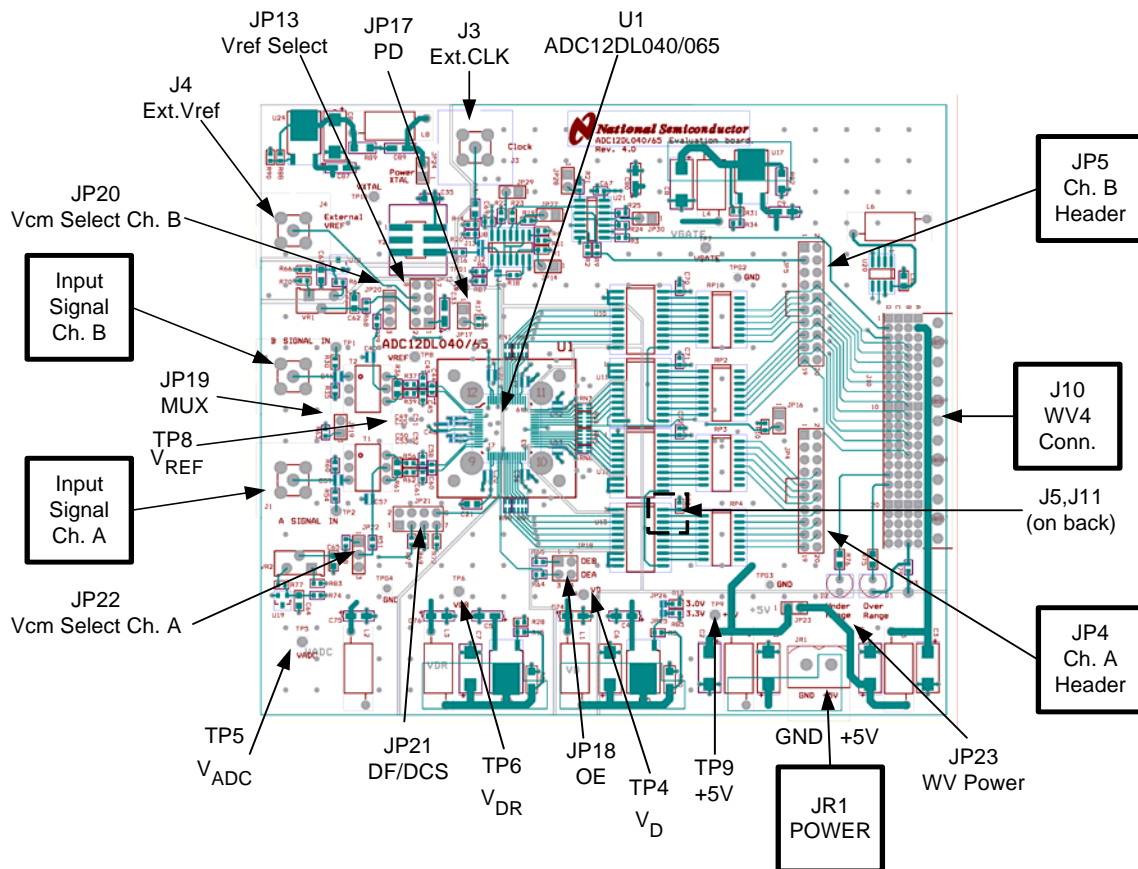


Figure 1. Major Component and Jumper Locations

3.0 Quick Start

Refer to *Figure 1* for locations of jumpers, test points and major components. The board is configured by default to use a crystal clock source, internal 1.0V reference, offset binary output data format, duty cycle stabilizer on, and parallel output mode. Refer to Section 4.0 and the Appendix for more information on jumper settings.

For Stand-Alone operation:

1. Connect a clean +5V power supply to pin 2 of Power Connector JR1. Pin 1 is ground.
2. Connect a signal from a 50-Ohm source to connector J1 (for Channel A). The ADC input signal can be observed at TP2. Because of isolation resistor R54 and the scope probe capacitance, the input signal at TP2 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
3. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data.
4. The digitized signal is available at pins 8 (MSB) through 19 (LSB) of JP4. See board schematic in *Section 8*.

For Computer Mode operation:

You must have version 4.1.7 or later of the WaveVision™ software to properly test this board. You can download the latest version from:

<http://www.national.com/appinfo/adc/wv4.html>

1. Connect the evaluation board to the WaveVision™ Digital Interface Board. See the WaveVision™ Board Manual for operation of that board. Connect the WaveVision™ board to the computer using a USB cable.
2. Connect a clean +5V power supply to pin 2 of Power Connector JR1. Pin 1 is ground. Short jumper JP23. With jumper JP23 shorted, the WaveVision™ board gets power from the ADC12DL040 Evaluation Board, therefore it does not require a separate power supply. **DO NOT provide separate power supplies to the Evaluation Board and the WaveVision Board when JP23 is shorted.**
3. Connect a clock source to connector J3. Connect a signal from a 50-Ohm source to connector J1 (for Channel A). The ADC input signal can be observed at TP2. Because of isolation resistor R54 and the scope probe capacitance, the input signal at TP2 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
4. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data with the WaveVision™ software.
5. Select which channel the WV4 board collects data from with the **Product Board Settings** item under the **Settings** menu. See the WaveVision™ Board Manual for instructions for gathering and analyzing data.

4.0 Functional Description

The ADC12DL040 Evaluation Board schematic is shown in *Section 8*. A list of test points and jumper settings can be found in the Appendix.

4.1 Input (signal conditioning) circuitry

This section describes the input circuitry for Channel A, which is the same as Channel B.

The input signal to be digitized should be applied to SMA connector J1. This 50 Ohm input is intended to accept a low-noise sine wave signal of up to 2V peak-to-peak amplitude. To accurately evaluate the dynamic performance of this converter, the input test signal will have to be passed through a high-quality bandpass filter with at least 14-bit equivalent noise and distortion characteristics.

Signal transformer T1 provides single-ended to differential conversion. The voltage V_{RMA} from the ADC, or an adjustable voltage from VR2 sets the common mode of the input signal by biasing the center tap of the secondary of T1. When VR2 is used, the voltage should be set within the acceptable range of the ADC, 0.5 to 2.0V. Jumper JP22 selects the source of the common mode voltage. Short pins 1-2 of JP22 to use VR2. The default setting is to use V_{RMA} from the ADC, with pins 2-3 shorted.

Jumper JP20 selects the source of the common mode voltage for Channel B. Short pins 1-2 of JP20 to use VR1. The default setting is to use V_{RMB} from the ADC, with pins 2-3 shorted.

4.2 ADC reference circuitry

The ADC12DL040 can use an internal 1.0V reference, an internal 0.5V reference, or an external reference. The reference is selected using jumper JP13. The default is the internal 1.0V reference, shorting pins 1-2.

An adjustable reference circuit is provided on the board. The simple circuit here is not temperature stable and is not recommended for your final design solution. The reference circuit will generate a voltage in the range of 0.5 to 2.0V. The ADC12DL040 is specified to operate with V_{REF} in the range of 0.8 to 1.2V, with a nominal value of 1.0V. The reference voltage is set with VR1. This circuit can also be used as a common mode voltage source (see section 4.1). Short pins 3-4 of JP13 to use VR1.

Short pins 7-8 of JP13 to select the internal 0.5V reference. Short pins 5-6 of JP13 to use the external reference voltage applied at connector J4.

4.3 ADC clock circuit

Solder jumpers are used to select the path of the clock to the ADC, the latches, and the output data connectors. While not as convenient as pin-type jumpers, these introduce less distortion into the clock signal.

The clock source is selected with jumper J12 or J13. By default J12 is shorted and J13 is open, which selects the crystal oscillator. To use an external clock source, connect the signal to connector J3, open J12, and short J13.

There are a number of solder jumpers which allow changes to the clock path, inversion of the clock, etc. Please refer to the schematic of *Section 8* and the Appendix for more information.

4.4 Digital Data Output

The default mode is Parallel Mode. This is set with JP19 open. In Parallel Mode the digital output data from Channel A of the ADC12DL040 is available at pins A4 (MSB) through A15 of the WV4 connector J10 and pins 8 (MSB) through 19 of header JP4. Channel B output data is available at pins B4 (MSB) through B15 of the WV4 connector J10 and pins 8 (MSB) through 19 of header JP5. When capturing data with WaveVision™ software, select which channel the WV4 board collects data from with the **Product Board Settings** item under the **Settings** menu. See the WaveVision™ Board Manual for instructions for gathering and analyzing data

Shorting JP19 puts the ADC in Multiplex Mode. In this mode the data from both channels is output on pins DA0:DA11 of the ADC. Refer to the ADC12DL040 datasheet for more detail of this function. To use Multiplex mode, open solder jumper J11, and short J5. The WaveVision™ software should be set to collect data on Channel A. The channel selected for output to WaveVision™ software is selected with JP16. With JP16 open, Channel A data is selected. Channel B is selected by shorting pins 1-2 of JP16.

4.5 Power Supply Connections

Power to this board is supplied through power connector JR1. The only supply needed is +5V at pin 2 plus ground at pin 1.

When using the ADC12DL040 Evaluation Board with the the WaveVision™ Digital Interface Board, a 5V logic power supply for the interface board is passed through the WV4 connector to the Digital Interface Board when jumper JP23 is installed. **DO NOT provide separate power supplies to the Evaluation Board and the WaveVision Board when JP23 is shorted.**

4.6 Power Requirements

Voltage and current requirements for the ADC12DL040 Evaluation Board mode are:

- +5.0V at 500 mA (1A when connected to the Digital Interface Board).

5.0 Installing the ADC12DL040 Evaluation Board

The evaluation board requires power supplies as described in *Section 4.5*. An appropriate signal source should be connected to the Signal Input SMA connector J1 or J2. When evaluating dynamic performance, an appropriate signal generator (such as the HP8644B or the R&S SME-03) with 50 Ohm source impedance should be connected to the Analog Input connector J1 and/or J2 through an appropriate bandpass filter as even the best signal generator available can not produce a signal pure enough to evaluate the dynamic performance of an ADC.

If this board is used in conjunction with the the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software, a USB must be connected

between the Digital Interface Board and the host. See the the WaveVision™ 4.0 Digital Interface Board manual for details.

6.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. The layout is taken care of with the design of this evaluation board. Note, the plots shown in *Section 6* are for illustrative purposes only. They were not taken with the ADC12DL040.

6.1 Clock Jitter

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in *Figure 2a*. Compare this with the more desirable plot of *Figure 2b*. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

Because the divided signal from the Digital Interface Board and the oscillator at Y1 are not synchronized, bad data will sometimes be taken because we are latching data when the outputs are in transition. This data might be as you see in *Figure 3* or *Figure 4*.

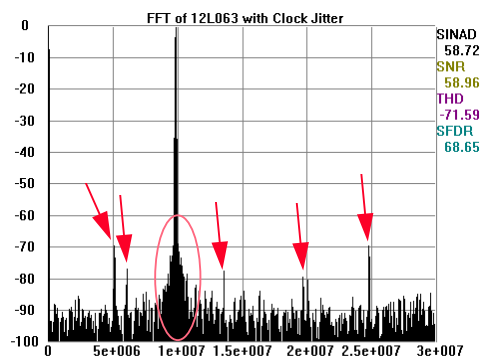


Figure 2a. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

The problem of *Figure 3* is obvious, but it is not as easy to see the problem in *Figure 4*, where the only thing we see is small excursions beyond the normal envelope. Compare *Figure 3* and *Figure 4* with *Figure 5*.

If your data capture results in something similar to what is shown here in *Figure 3* or in *Figure 4*, take another sample. It may take a few trials to get good data.

The use of WAVEVSN BRD 4.0 Digital Interface Board eliminates this problem, so that board is recommended.

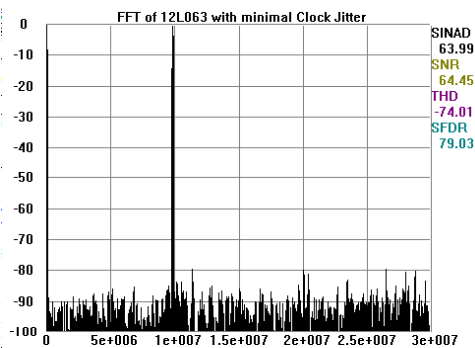


Figure 2b. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

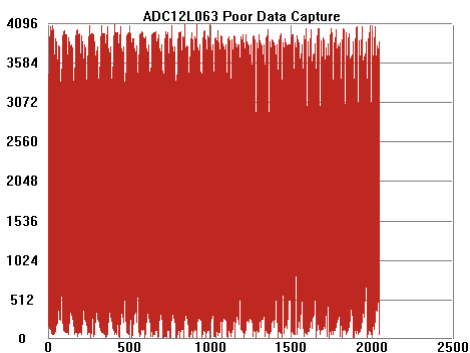


Figure 3. Poor data capture resulting from trying to capture data while the ADC outputs are in transition

6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. We call this *coherent sampling*. Coherent sampling greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (f_{in}) and the sample rate (f_s), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

Further, f_{in} (signal input frequency) and f_s (sampling rate) should be locked to each other so that the relationship between the two frequencies is exact. Locking the two signal sources to each other also causes whatever sample-to-sample clock edge timing variation (jitter) that is present in the two signals to cancel each other.

Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling.

7.0 Evaluation Board Specifications

| | |
|------------------------|---|
| Board Size: | 5" x 5.63" (12.7 cm x 14.29 cm) |
| Power Requirements: | +5.0V, 1 A (ADC12DL040EVAL and WaveVision™ 4.0 Board) |
| Clock Frequency Range: | 40/65 MHz |
| Analog Input | |
| Nominal Voltage: | 2V _{P-P} |
| Impedance: | 50 Ohms |

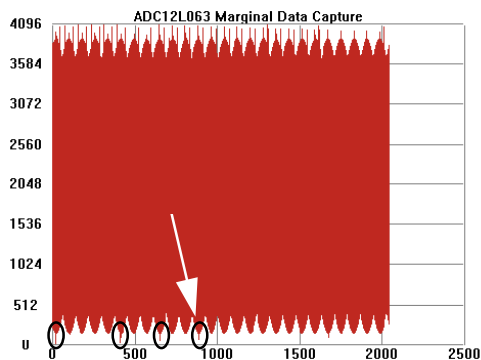


Figure 4 Marginal data capture that results from trying to capture data that is near but not right at the point where the ADC outputs are in transition.

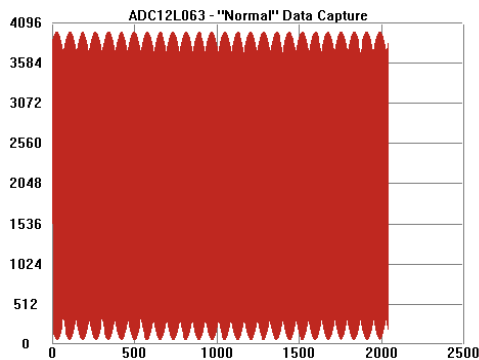
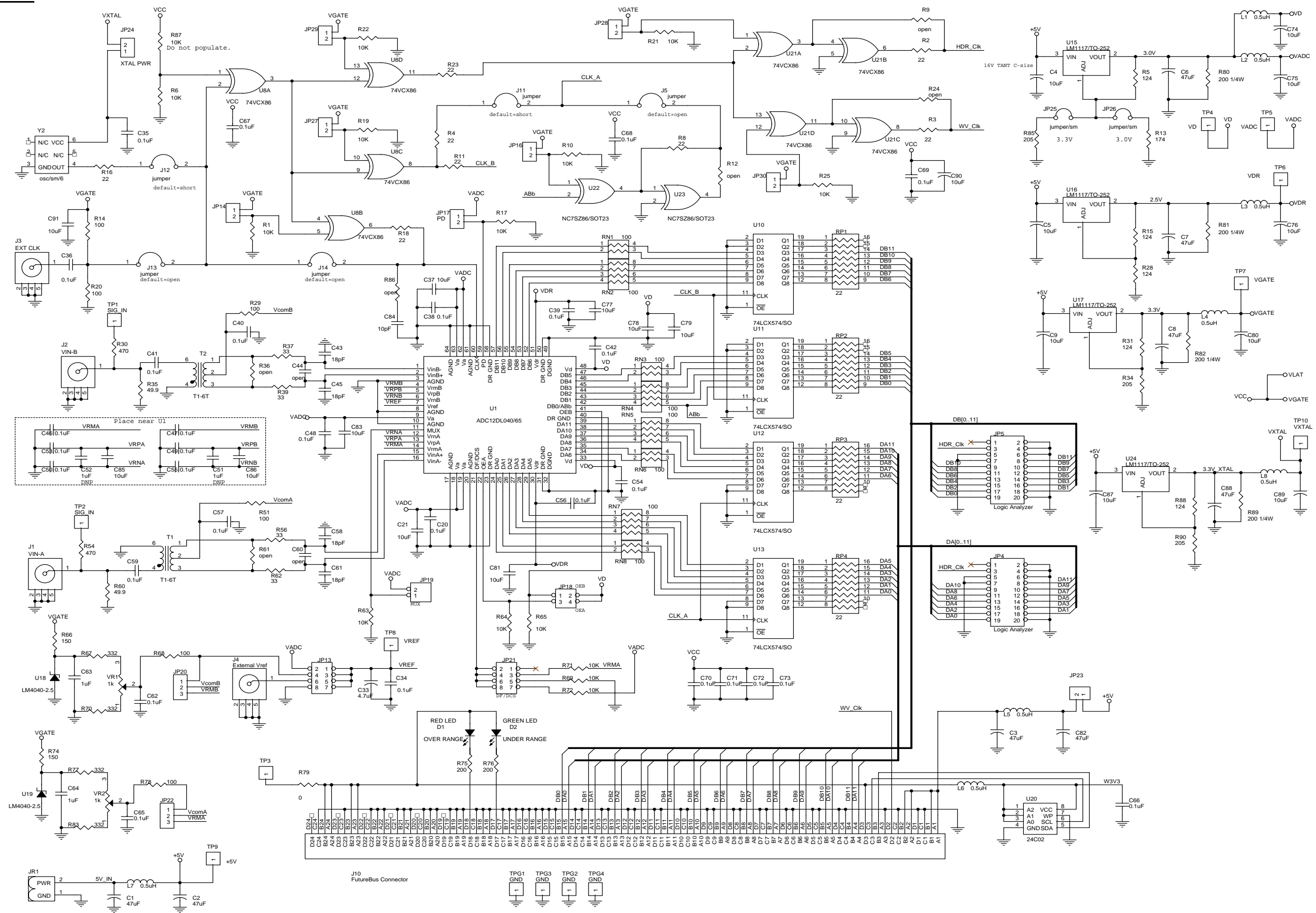
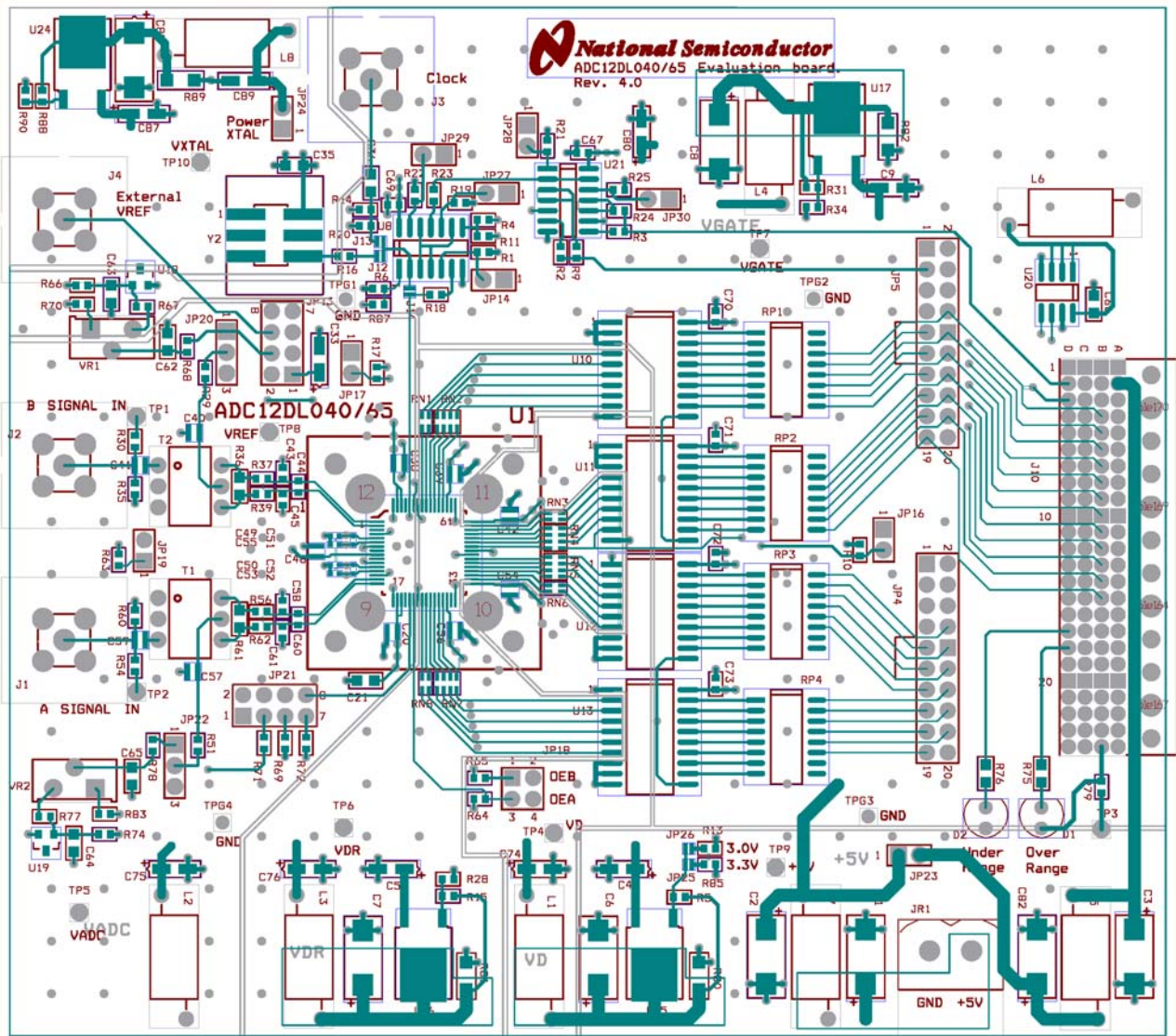


Figure 5. Normal data capture.

8.0 Hardware Schematic



9.0 Assembly Drawing



10.0 Evaluation Board Bill of Materials

| QTY | REFERENCE | DESCRIPTION | VALUE | Package | Manufacturer | Manufacturer P/N |
|-----|---|---------------|---------------|----------------------|------------------|------------------|
| 8 | C1,C2,C3,C6,C7,C8,C82, C88 | CAP TANT | 47uF | SMD 7343 | KEMET | T491D476K010AS |
| 10 | C4,C5,C9,C74,C75,C76,C80, C87,C89,C90 | CAP TANT | 10uF | SMD 3216 | KEMET | T491A106K006AS |
| 13 | C20,C38,C39,C40,C41,C42, C46,C47,C48,C54,C56,C57, C59 | CAP CER | 0.1uF | SMD 0508 | Panasonic | ECY-29RE104KV |
| 10 | C21,C37,C77,C78,C79,C81, C83,C85,C86,C91 | CAP CER | 10uF | SMD 0805 | Panasonic | ECJ-2FF0J106Z |
| 1 | C33 | CAP TANT | 4.7uF | SMD 3216 | Kemet | T491A475K010AS |
| 8 | C34,C67,C68,C69,C70,C71, C72,C73 | CAP CER | 0.1uF | SMD 0603 | Panasonic | ECJ-1VB1C104K |
| 5 | C35,C36,C62,C65,C66 | CAP CER | 0.1uF | SMD 0805 | Panasonic | ECJ-2VB1E104K |
| 4 | C43,C45,C58,C61 | CAP CER | 18pF | SMD 0603 | Panasonic | ECJ-1VC1H180J |
| 2 | C44,C60 | CAP | open | | | N/A |
| 4 | C49,C50,C53,C55 | CAP CER | 0.1uF | SMD 0402 | Panasonic | ECJ-0EB1A104K |
| 2 | C51,C52 | CAP CER | open | SMD 402 | Panasonic | ECJ-0EF0J105Z |
| 2 | C63,C64 | CAP CER | 1uF | SMD 805 | Panasonic | ECJ-2YB1A105K |
| 1 | C84 | CAP CER. | 10pF | SMD 0603 | Panasonic | ECJ-1VC1H100D |
| 1 | D1 | LED RED | OVER RANGE | 5MM | Lumex OPTO/COMP | SSL-LX5093IT |
| 1 | D2 | LED GREEN | UNDER RANGE | 5MM | Lumex OPTO/COMP | SSL-LX5093GT |
| 2 | JP4,JP5 | CON | HDR 2X10 | .100 DUAL STR 60POS | Sullins Elect | PBC30DADN |
| 2 | JP13,JP21 | CON | HDR 4X2 | .100 DUAL STR 60POS | Sullins Elect | PBC30DADN |
| 8 | JP14,JP16,JP17,JP23,JP27, JP28,JP29,JP30 | CON | HDR 1X2 | .100 SINGL STR 36POS | Sullins Elect | PBC36SAAN |
| 1 | JP18 | CON | HDR 2X2 | .100 DUAL STR 60POS | Sullins Elect | PBC30DADN |
| 1 | JP19 | CON | HDR 1X2 | .100 SINGL STR 36POS | Sullins Elect | PBC36SAAN |
| 2 | JP20,JP22 | CON | HDR 1X3 | .100 SINGL STR 36POS | Sullins Elect | PBC36SAAN |
| 1 | JP24 | CON | HDR 1X2 | .100 SINGL STR 36POS | Sullins Elect | PBC36SAAN |
| 2 | JP25,JP26 | JUMPER | jumper/sm | | | |
| 1 | JR1 | CONN | ECL power | 2 Pos 5.08MM | Phoenix Contacts | 1755736 |
| 1 | J1 | CON | VIN-A | SMA RECEPTACLE | Amphenol | 901-144-8RFX |
| 1 | J2 | CON | VIN-B | SMA RECEPTACLE | Amphenol | 901-144-8RFX |
| 1 | J3 | CON | EXT CLK | SMA RECEPTACLE | Amphenol | 901-144-8RFX |
| 1 | J4 | CON | External Vref | SMA RECEPTACLE | Amphenol | 901-144-8RFX |
| 5 | J5,J11,J12,J13,J14 | JUMPER | jumper | N/A | N/A | N/A |
| 1 | J10 | CONN RECEPT | FutureBus Con | RT/A 2MM 96POS 30AU | Tyco | 5536511-3 |
| 8 | L1,L2,L3,L4,L5,L6,L7,L8 | FERRITE_CHOKE | 2.5 TURNS | | JW MILLER MAG. | FB20020-4B-RC |
| 4 | RN1,RN3,RN6,RN8 | RES ARRAY | 100 | 2 RES SMD | PANASONIC | EXB-V4V101JV |
| 4 | RN2,RN4,RN5,RN7 | RES ARRAY | 100 | 0603 x 4 | PANASONIC | EXB-V8V101JV |
| 4 | RP1,RP2,RP3,RP4 | RES-NET | 22 | 16-PIN SMD | CTS CORP. | 768163220G |
| 14 | R1,R6,R10,R17,R19,R21, R22,R25,R63,R64,R65,R69, R71,R72 | RES | 10K | SMD 0603 | PANASONIC | ERJ-3EKF1002V |
| 7 | R2,R3,R4,R11,R16,R18,R23 | RES | 22.1 | SMD 0603 | PANASONIC | ERJ-3EKF22R1V |
| 5 | R5,R15,R28,R31,R88 | RES | 124 | SMD 0603 | PANASONIC | ERJ-3EKF1240V |

| | | | | | | |
|---|---------------------|------|-------------------------|----------------------|------------------|--|
| 1 | R8 | RES | 22 | SMD 0603 | PANASONIC | ERJ-3EKF22R1V |
| 3 | R9,R12,R87 | RES | open | N/A | | N/A |
| 1 | R13 | RES | 174 | SMD 0603 | PANASONIC | ERJ-3EKF1740V |
| 4 | R14,R20,R68,R78 | RES | 100 | SMD 0603 | PANASONIC | ERJ-3EKF1000V |
| 2 | R24,R86 | RES | open | N/A | | N/A |
| 2 | R29,R51 | RES | 100 | SMD 0603 | PANASONIC | ERJ-3EKF1000V |
| 2 | R30,R54 | RES | 475 | SMD 0603 | PANASONIC | ERJ-3EKF4750V |
| 3 | R34,R85,R90 | RES | 205 | SMD 0603 | PANASONIC | ERJ-3EKF2050V |
| 2 | R35,R60 | RES | 49.9 | SMD 0603 | PANASONIC | ERJ-3EKF49R9V |
| 2 | R36,R61 | RES | open | N/A | | N/A |
| 4 | R37,R39,R56,R62 | RES | 33.2 | SMD 0603 | PANASONIC | P33.2HCT |
| 2 | R66,R74 | RES | 150 | SMD 0603 | PANASONIC | ERJ-3EKF1500V |
| 4 | R67,R70,R77,R83 | RES | 332 | SMD 0603 | PANASONIC | ERJ-3EKF3320V |
| 2 | R75,R76 | RES | 200 | SMD 0805 | PANASONIC | P200CCT |
| 1 | R79 | RES | 0 | SMD 0603 | PANASONIC | RC0603JR-070RL |
| 4 | R80,R81,R82,R89 | RES | 200 | SMD 1206 | PANASONIC | ERJ-8GEYJ201V |
| 4 | TPG1,TPG2,TPG3,TPG4 | Hdr. | HDR 1X1 | .100 SINGL STR 36POS | Sullins Elect | PBC36SAAN |
| 2 | TP1,TP2 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP3 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP4 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP5 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP6 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP7 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP8 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP9 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 1 | TP10 | TP | .040"D | MINI .040"D | Keystone Elec. | 5002 |
| 2 | T1,T2 | XFMR | .015-300MHZ | SM | MINI-CIRCUITS | T1-6T X65 |
| 1 | U1 | IC | DUAL ADC | 64-TQFP | NATIONAL | |
| 2 | U8,U21 | IC | EXCL-OR QUAD | 14SOIC | FAIRCHILD | 74VCX86M |
| 4 | U10,U11,U12,U13 | IC | FLIP FLOP OCT | 20SOIC | FAIRCHILD | 4LCX574WMX |
| 4 | U15,U16,U17,U24 | IC | LM1117/TO-252 | TO252 | NATIONAL | LM1117DT-ADJ |
| 2 | U18,U19 | IC | LM4040-2.5 | SOT-23-5 | NATIONAL | LM4040CIM3-2.5CT |
| 1 | U20 | IC | EEPROM 2K | 8SOIC | ATMEL | AT24C02BN-10SU-1.8 |
| 2 | U22,U23 | IC | EX-OR GATE 2-IN | SOT-23-5 | Texas Instrument | SN74LVC1G86DBVR |
| 2 | VR1,VR2 | POT | 1k | 3/8" SQ CERM SL MT | BOURNS INC | 3296Y-1-102 |
| 1 | Y2 | OSC | 40.00MHz or 66.00MHZ | 5X7MM CERAMIC | PLETRONICS | SM7745HV-66.0M-Y9 or SM7745HV-40.00M-Y9 |

APPENDIX

A1.0 Operating in the Computer Mode

The ADC12DL040 Evaluation Board is compatible with the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software. You must have version 4.1.7 or later of the WaveVision™ software to properly test this board. You can download the latest version from: <http://www.national.com/appinfo/adc/wv4.html>

When connected to the Digital Interface Board, data capture is easily controlled from a personal computer operating in the Windows environment. The data samples that are captured can be observed on the PC video monitor in the time and frequency domains. The FFT analysis of the captured data yields insight into system noise and distortion sources and estimates of ADC dynamic performance such as SINAD, SNR and THD. Select which channel the WV4 board collects data from with the **Product Board Settings** item under the **Settings** menu. See the Digital Interface Board manual for more information.

A2.0 Summary Tables of Test Points, Connectors, and Jumper Settings

A2.1 Test Points

Test Points on the ADC12DL040 Evaluation Board

| | |
|-------------|----------------------------|
| TP 1 | Input Signal Channel B |
| TP 2 | Input Signal Channel A |
| TP3 | 3.3V from WaveVision Board |
| TP4 | ADC Digital Supply |
| TP5 | ADC Analog Supply |
| TP6 | ADC Output Driver Supply |
| TP7 | Logic Supply |
| TP8 | VREF |
| TP9 | +5V |
| TPG1 – TPG4 | Ground |

A2.2 Connectors

JR1 Connector - Power Supply Connections

| | | |
|------|-----|---------------------|
| P1-1 | GND | Power Supply Ground |
| P1-2 | +5V | +5V Power Supply |

A2.3 Jumper settings

Note: Default settings are in **bold**

JP13 : VREF selection jumper settings

| | |
|--------------------|---|
| Connect 1-2 | Use internal 1.0V reference |
| Connect 3-4 | Use voltage from VR1 as reference voltage |
| Connect 5-6 | Use external voltage from J4 as reference voltage |
| Connect 7-8 | Use internal 0.5V reference |

JP14 : Latch Invert

| | |
|--------------------|---------------------------------|
| Connect 1-2 | Invert clock for latches |
| 1-2 OPEN | Do not invert clock |

JP16 : Latch Invert in Multiplex Mode with ABb as clock

| | |
|-----------------|-----------------------------------|
| Connect 1-2 | Channel B data is selected |
| 1-2 OPEN | Channel A data is selected |

JP17 : Power Down

| | |
|-----------------|-----------------------------------|
| Connect 1-2 | Put ADC in Power Down mode |
| 1-2 OPEN | ADC is in normal operation |

JP18 : Output Enable

| | |
|-----------------|---|
| Connect 1-2 | Channel B outputs are in high impedance state |
| Connect 3-4 | Channel A outputs are in high impedance state |
| 1-2 OPEN | Channel B outputs are enabled |
| 3-4 OPEN | Channel A outputs are enabled |

JP19 : Multiplex/Parallel Mode

| | |
|-----------------|--|
| Connect 1-2 | Outputs are in Multiplex Mode on Channel A outputs |
| 1-2 OPEN | Outputs are in parallel mode |

JP20 : Channel B Vcm selection

| | |
|--------------------|---|
| Connect 1-2 | Use voltage from VR1 as common mode voltage for Channel B |
| Connect 2-3 | Use common mode voltage from ADC for Channel B |

JP21 : Data Format / Duty Cycle Stabilizer

| | |
|--------------------|---|
| Connect 1-2 | Select Output format of Offset Binary, Duty Cycle Stabilizer is OFF |
| Connect 3-4 | Select Output format of 2's complement, Duty Cycle Stabilizer is OFF |
| Connect 5-6 | Select Output format of 2's complement, Duty Cycle Stabilizer is ON |
| Connect 7-8 | Select Output format of Offset Binary, Duty Cycle Stabilizer is ON |

JP22 : Channel A Vcm selection

| | |
|--------------------|---|
| Connect 1-2 | Use voltage from VR2 as common mode voltage for Channel A |
| Connect 2-3 | Use common mode voltage from ADC for Channel A |

JP23 : Wavevision Power (when used with WaveVision™ 4.0 Digital Interface Board)

| | |
|-----------------|---|
| Connect 1-2 | A +5V supply is applied to the WaveVision Board or the ADC12DL040 Board, but not both |
| 1-2 OPEN | Separate supplies are used for the WaveVision Board and the ADC12DL040 Board |

JP24 : Power for Crystal Oscillator

| | |
|--------------------|--|
| Connect 1-2 | Power is applied to the crystal |
| 1-2 OPEN | No power for the crystal |

JP27 : Latch Invert

| | |
|--------------------|---------------------------------|
| Connect 1-2 | Invert clock for latches |
| 1-2 OPEN | Do not invert clock |

JP28 : Latch Invert

| | |
|-----------------|----------------------------|
| Connect 1-2 | Invert clock for latches |
| 1-2 OPEN | Do not invert clock |

JP29 : Latch Invert

| | |
|-----------------|----------------------------|
| Connect 1-2 | Invert clock for latches |
| 1-2 OPEN | Do not invert clock |

JP30 : Latch Invert

| | |
|-----------------|----------------------------|
| Connect 1-2 | Invert clock for latches |
| 1-2 OPEN | Do not invert clock |

A2.4 Clock Circuit Solder Jumper settings

Solder jumpers are used to select the path of the clock to the ADC, the latches, and the capture device at J7. While not as convenient as pin-type jumpers, these introduce less distortion into the clock signal.

By default the following jumpers are OPEN:

J5, J13, J14

By default the following jumpers are shorted:

J11, J12

A2.5 VADC/VD Solder Jumper settings

Either J25 or J26 is shorted to set the voltage for the ADC's analog (VADC) and digital (VD) supplies.

J26 is shorted to produce a VADC and VD of 3.0V, which is the default value for the ADC12DL040.

J25 is shorted to produce a VADC and VD of 3.3V, which is the default value for the ADC12DL065.

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