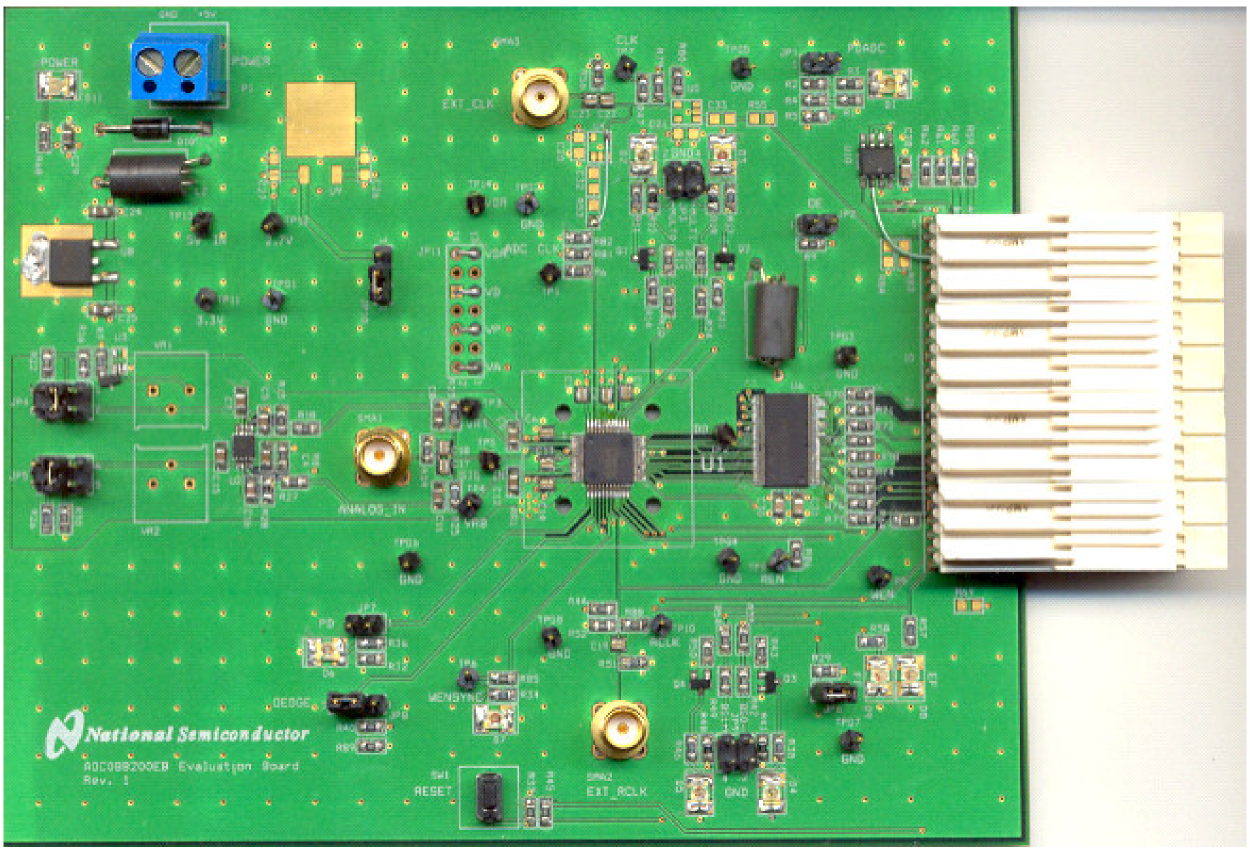
National Semiconductor

July 2007
Rev -

Evaluation Board Users' Guide

ADC08B200 8-Bit Analog-to-Digital Converter with Capture Buffer



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1.0 Introduction

The ADC08B200EB Design Kit (consisting of the ADC08B200 Evaluation Board, National's WaveVision software and this Users' Guide) is designed to ease evaluation and design-in of National Semiconductor's ADC08B200 8-bit Analog-to-Digital Converter, which operates at sample rates up to 210 MSPS.

The WaveVision software operates under Microsoft Windows. The signal at the Analog Input is digitized and can be captured and displayed on the computer monitor as dynamic waveforms. The digitized output is also available at FutureBus connector J1.

The software can perform an FFT on the captured data upon command. The frequency domain (FFT) display also shows dynamic performance in the form of SNR, SINAD, THD, SINAD and ENOB.

While this evaluation board can be used in a stand-alone mode, evaluation with this system is simplified by connecting the board to the WaveVision Data Capture Board (order number WAVEVSN BRD 5.1), which is connected to a personal computer through a USB port and running WaveVision software operating under Microsoft Windows. Use the WaveVision 4.3.19a program provided with the board (and not yet available on the web).

The reference voltages are set with jumpers, but provision is made for adjustment of Reference Voltages V_{RT} and V_{RB} with potentiometers VR1 and VR2, respectively, which must be added to the board if this fine adjustment is desired. The reference source is not temperature compensated, but drift is minimal.

2.0 Board Assembly

The ADC08B200 Evaluation Board comes pre-assembled. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement and to *Figure 2* for the Evaluation Board schematic.

3.0 Quick Start

Refer to *Figure 1* for locations of test points and major components.

1. Start (run) the WaveVision software.
2. Connect the evaluation board to the WaveVision5 Data Capture Board. See the Data Capture Board Users' Guide for operation of that board.
3. Connect a clean power supply to the terminals of connector P1. Adjust power supply to voltage of +4.5V to +5.5V before connecting it to the board. Turn on the power and confirm that there is about +5 Volts at TP13.
4. Be sure that jumpers on the board are in their default positions per the "Jumper Connections" in the Appendix. Check for approximate top and bottom references of 1.9V at TP3 and 0.3V at TP4.
5. Connect a signal of about 1.55V_{P-P} amplitude from a 50-Ohm source to Analog Input connector SMA1 through an appropriate band pass filter. The ADC input signal can be observed at TP4, but nothing should be connected to TP4 during data capture.
6. Gather data by pressing the F1 key on the computer keyboard. Observe the frequency domain (FFT) plot by selecting the FFT tab within the WaveVision window. Note that an appropriate band pass filter should be used at the signal input to the board.
7. See the WaveVision Data Capture Board Users' Guide for complete data gathering instructions.

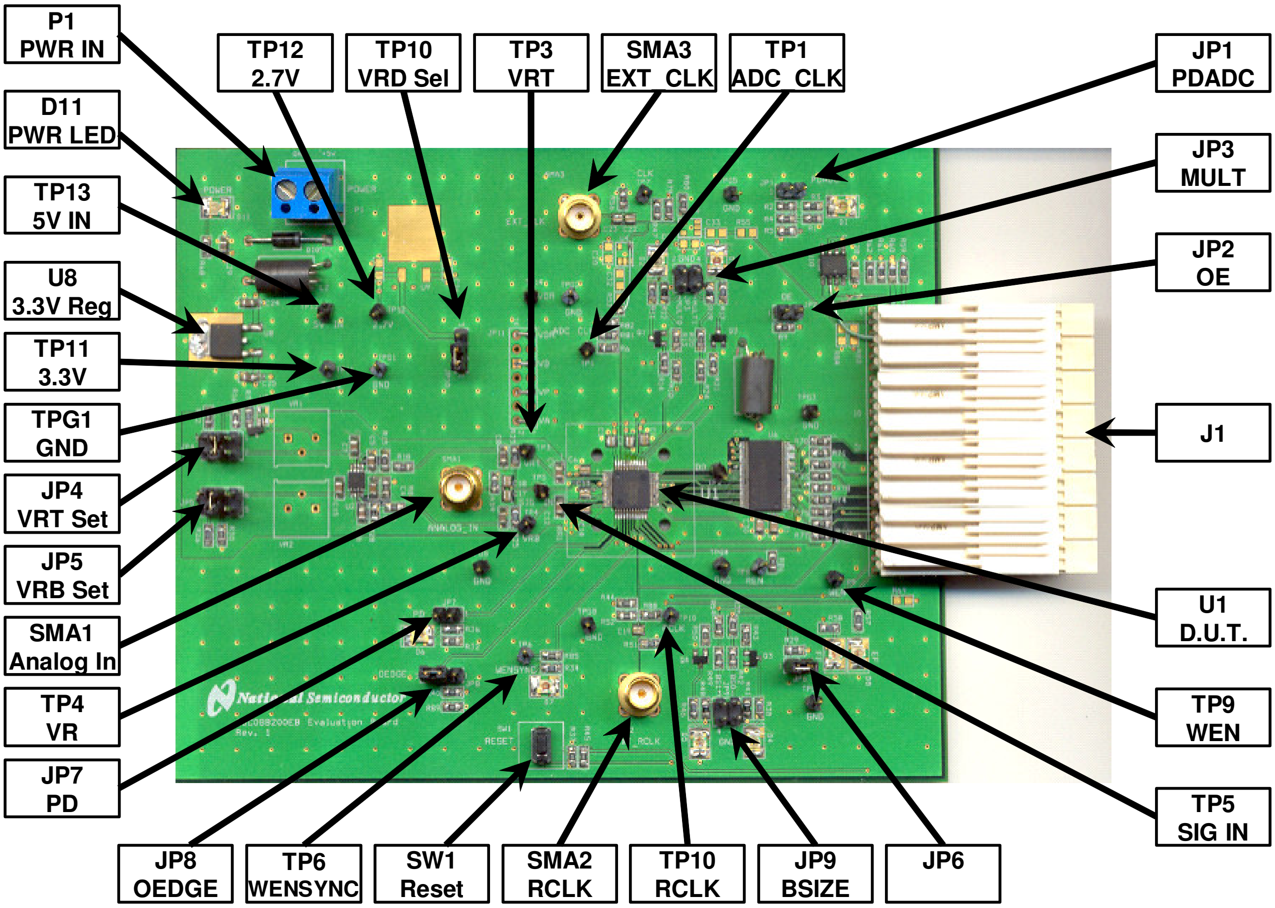

Figure 1. Component and Test Point Locations

4.0 Functional Description

The ADC08B200 Evaluation Board component and test point locations are shown in *Figure 1*. The board schematic is shown in *Figure 2*.

4.1 Input (signal conditioning) circuitry

The input signal to be digitized should be applied to connector SMA1 through an appropriate band pass filter. The 50 Ohm boar input is intended to accept a low-noise sine wave signal of amplitudes up to 2.5V peak-to-peak. To accurately evaluate the ADC08B200 dynamic performance, the input test signal should be a single frequency passed through a high-quality band pass filter.

Resistors R23 and R25 provide the needed input bias to the ADC08B200 with a sine wave input. Complex waveforms might not be properly centered within the active input range of the ADC08B200.

Resistor R39, in parallel with R23 and R25, provide a 50-Ohm board input termination.

If DC. coupling to the ADC analog input is desired, it may be done by shorting across capacitor C17. Use care not to drive the ADC08B200 inputs beyond the limits of the power supply.

4.2 ADC reference circuitry

The reference circuitry will provide nominal reference voltages of 2.5V, 1.9V or 1.0V for V_{RT} and 0V, 0.3V or 1.0V for V_{RB}. This means that the full-scale range may be set as low as 0V peak-to-peak and as high as 2.5V peak-to-peak, which is beyond the specified 1.0 to 2.3V range of the ADC08B200.

The reference voltages for the ADC08B200 can be monitored at test point TP3 and TP4 and are set with JP4 and JP5. The user may populate VR1 and VR2, if desired. If this is done, There should be no jumpers on JP4 or JP5.

4.3 ADC clock circuit

The clock signal applied to the ADC08B200 is supplied from an external signal generator via connector SMA3. Clock amplitude should be at least $600mV_{P-P}$.

4.5 Digital Data Output.

The digital output data from the ADC08B200 is latched by digital buffer U6 to minimize loading on the ADC08B200 outputs and is available at the 96-pin FutureBus connector J1. The series resistors after U6 isolate the buffer from the capacitive load of the WaveVision Data Capture board, reducing the noise produced on the ADC08B200 evaluation board.

4.6 Operational Controls

Virtually all of the controls of the ADC08B200 can be exercised with this evaluation board. While using this evaluation board in a Stand Alone fashion is possible, evaluation is simplified by controlling this board with a WaveVision5 Data Capture Board.

The operational controls of this board are split between Basic Controls and Buffer Controls. The ADC08B200 data sheet should be consulted for more information on the use of these controls.

4.6.1 Basic Controls

The Basic Controls of this board consist of PDADC, PD, OEDGE, MULT, VDR Select, OE, Reference Voltage and DRDY.

6.6.1.1 PDADC

Raising the PDADC pin of the ADC08B200 high puts only the A/D converter (ADC) block within the device into a power down mode. The buffer and bias circuitry remain active so that the buffer can be read while the ADC is powered down, minimizing overall power consumption. On this board, this function is controlled with jumper JP1 only and can not be controlled through the WaveVision Data Capture Board. RED LED D1 is illuminated when the device is in the PDADC mode.

4.6.1.2 PD

Raising the PD pin of the ADC08B200 high puts the entire chip into the power down mode. It will not convert and its buffer can not be read while in this mode. On this board, this function is controlled with jumper JP7 only and can not be controlled through the WaveVision Data Capture Board. RED LED D6 is illuminated when the device is in the PD mode.

4.6.1.3 OEDGE

The OEDGE input to the ADC08B200 causes the output data (conversion results) to transition at the rising edge of DRDY if OEDGE is high, or to transition at the falling edge of DRDY if OEDGE is low.

When this board is used with a WaveVision Data Capture Board, good data capture is possible with either setting of this pin because of the way the FPGA on the WaveVision Data Capture Board is programmed.

Allowing the OEDGE pin to float puts the ADC08B200 into its test mode, where a repeating 00h - FFh - 00h - FFh - 00h sequence is sent on the data outputs.

The jumper at JP8 is used to control the OEDGE input of the ADC08B200. This function can not be controlled by the WaveVision Data Capture Board.

4.6.1.4 MULT

These pins are used to select the CLK input as the conversion clock or to multiply that input frequency by 2, 4 or 8 to produce a higher frequency conversion clock. Note that the range of input frequencies allowed with any given setting of the clock multiplier is given in the product data sheet. The jumper settings of JP3 are used in the stand alone mode of this board, but are ignored when using the WaveVision Data Capture Board.

4.6.1.5 VDR Select

This jumper (JP10) is not populated on this evaluation board as shipped, but is used to select a lower ADC08B200 output driver voltage (VDR) if U9 and is associated components are populated. Positions 1 and 2 of this header are shorted together on the board as shipped. If desired, the user may remove the short at this header position, install a 3-pin header at JP10, an LM38690DC-2.5 and capacitors C26 and C27 to enable this function. Alternatively, it is possible to remove the short At JP10 and provide the desired output driver voltage at pin 3 of JP10 position or at TP12 position.

4.6.1.6 OE

The OE pin of the ADC08B200, when high, enables the data and DRDY outputs. When this pin is low, the data and DRDY outputs are in a high impedance state. On this board, this pin is controlled by JP2 and can not be controlled by the WaveVision Data Capture Board.

4.6.1.7 Reference Voltage

The ADC08B200 has both an upper reference voltage (VRT) and a lower reference voltage (VRB). These voltages are controlled on this board by three position headers JP4 and JP5, respectively. Each of these headers must have a jumper in place or the reference voltages for the ADC08B200 will be at undetermined potentials.

The board is fabricated for the possibility of using potentiometers (VR1 and VR2) to set the upper and lower reference voltages, but these potentiometers are not populated on the board as shipped. If these potentiometers are installed, the jumpers on headers JP4 and JP5 should be removed.

4.6.1.8 DRDY

The DRDY output of the ADC08B200 indicates when the conversion data transitions. (The OEDGE pin is used to determine on what edge of DRDY the data transitions.) The DRDY output simplifies capture of the conversion results data. Since DRDY has a 50% duty cycle, the opposite edge falls at the center of the data valid time.

The DRDY signal is present only when both BSIZE pins are low, or when either BSIZE pin is high **and** there is an RCLK signal **and** REN is high.

4.6.2 Buffer Controls

The conversion buffer of the ADC08B200 can be configured to hold 256, 512 or 1024 bytes of data. The buffer must be completely filled before it can be read.

The Buffer Controls of this board consist of BSIZE, WEN, ASW, REN, RCLK and RESET.

4.6.2.1 BSIZE

The BSIZE inputs (B0:B1) determine the size of the buffer. Setting these two bits low will cause the data to be streamed out at the sample rate without the use of the buffer. The BSIZE bits cause the buffer size to be as indicated here:

B1	B0	Buffer Size
0	0	0 (straight through)
0	1	256 bytes
1	0	512 bytes
1	1	1024 bytes

The jumper settings of JP9 are used in the stand alone mode of this board, but are ignored when using the WaveVision Data Capture Board.

4.6.2.2 WEN

This Write Enable input, when high, enables writing of conversion data to the buffer when at least one of the BSIZE bits is high. The WENSYNC output is not used on this board, but indicates when data capture begins so that timing of the captured data is known.

The WEN input is not controlled by a jumper, but only through the FutureBus connector. The signal here may be monitored at TP9.

The WENSYNC output is not sent to the FutureBus connector, but may be monitored at TP6.

4.6.2.3 ASW

This Auto Stop Write pin, when high, causes the writing of new conversion data to the buffer once it has been filled with the number of bytes set by the BSIZE bits. This is to prevent over writing of unread data with new data. JP6 controls the input to this pin of the ADC08B200, which can not be controlled with the WaveVison Data Capture Board.

4.6.2.4 REN

The REN input, when high, enables reading of the on-chip buffer with RCLK. The REN input is not controlled by a jumper, but only through the FutureBus connector. This signal may be monitored at TP8.

4.6.2.5 RCLK

The RCLK input, along with the REN input, is used to read the contents of the buffer.

4.6.2.6 RESET

Generally, the on-chip buffer must be completely read out before it can be written to again. Should it be necessary to write to a buffer that has been at least partially written to or has not been completely read, a pulse to this RESET pin will reset the buffer so that it may be written to.

4.7 The Power Supply

Power to this board is supplied through power connector P1. The only Voltage needed for this board are +5V, as described in *Section 4.8*, below.

When using the ADC08B200 Evaluation Board with the WaveVision Data Capture Board, the 5V power supplied to either that board or to the ADC08B200 evaluation board is passed from one board to the other through the FutureBus connector J1. The supply voltage is protected against reverse polarity with shunt diode D10. The +3.3 Volts needed for the ADC08B200 is provided with voltage regulator U8.

While U9 and JP10 can be used to select 2.5V for the ADC08B200 output drivers, U9, JP10, C26 and C27 are not populated on this board. The user may add these components if they are desired.

4.8 Power Requirements

Voltage and current requirements for the ADC08B200 Evaluation Board are as indicated in *Section 6.0*.

In addition, the power supply must provide about power required by the WaveVision Data Capture Board.

5.0 Installing and Using the ADC08B200 Evaluation Board

The evaluation board requires power as described in *Sections 4.7* and *4.8*, above. An appropriate signal generator with 50 Ohm source impedance should be connected to the Analog Input, SMA1. A bandpass filter should be inserted between the generator output and the input to the ADC08B200 evaluatoin board when evaluating sinusoidal signals to be sure there are no unwanted frequencies (harmonics and noise) presented to the ADC. A USB cable must be connected between the WaveVision Data Capture Board and the host computer for use in the computer mode. See the WaveVision Data Capture Board Users' Guide for details.

5.1 WaveVision Software

The WaveVision software runs under Windows. The WaveVision Data Capture Board comes with a CDROM that has the WaveVision software, but the required version for this board is different from that version. Use WaveVision 4.3.19a supplied with this board.

5.2 Setting up the ADC08B200 Evaluation Board

This evaluation package was designed to be easy and simple to use, and to provide a quick and simple way to evaluate the ADC08B200. The procedures given here will help you to properly set up the board.

5.2.1 Board Set-up

Refer to *Figure 1* for locations of connectors, test points and jumpers on the board and to *Figure 2* for the board schematic.

1. Connect The ADC08B200 evaluation board to a WaveVision5 Data Capture Board.
2. Connect power to either board per requirements of *Sections 4.7* and *4.8*. Confirm that Red LED D10 on the ADC08B200 evaluation board is on, indicating power is applied to that board, and that at least one LED on the WaveVision Data Capture Board is on, indicating presence of power on that board.
3. Be sure an appropriate clock signal is applied to connector SMA3.
4. Connect an appropriate test signal source to SMA1 of the ADC08B200 evaluation board through an appropriate filter.
5. Connect a USB cable between the WaveVision Data Capture Board and your computer.

5.2.2 Check of Analog Functions

Refer to *Figure 1* for locations of connectors, test points and jumpers on the board. If at any time the expected response is not obtained, see *Section 5.2.5* on Troubleshooting.

1. Perform steps 1 through 5 of Section 5.2.1.
2. Put a jumper in across pins 3 and 4 of JP4 and check for a voltage of about 1.9V at TP3.
3. Put a jumper in across pins 3 and 4 of JP5 and check for a voltage of about 0.3V at TP4.
4. Scope TP5 to be sure the input signal is present then remove the scope probe.

This completes the check of the analog portion of the evaluation board.

5.2.3 Quick Check of Software and Computer Interface Operation

1. Perform steps of Paragraph 5.2.2, above.
2. RUN the WaveVision program. While it is loading, perform the next three steps, below.
3. Install a USB cable between the WaveVision Data Capture Board and a USB port on your computer.
4. Provide +5V power to either of the boards.
5. Supply a 1.5 Vp-p sine wave of about 5 MHz at Analog Input SMA1.
6. After the WaveVison software comes up, acquire data by pressing the F1 key on the computer keyboard. Data transfer can take a few seconds. When transfer is complete, the data window should show many sine waves. The display may show a nearly solid area of red, which is O.K.
7. With the mouse, you may click on the magnifying icon, then click and drag to select a small portion of the displayed waveform for better examination of portions of the waveform.
8. Click on the FFT tab to run an FFT on the data and display a frequency domain plot.

The FFT data will provide a measurement of SINAD, SNR, THD SFDR and ENOB, easing the performance verification of the ADC08B200.

Note: Be sure to use a bandpass filter between the signal source and this board for accurate dynamic performance measurement.

5.2.4 Getting Consistent Readings

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than our measurements would indicate. Windowing is a common method of improving FFT results of finite data.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies, forcing the data to cleanly "wrap around" itself, providing coherent sampling. This eliminates the distortion that would otherwise be present in an FFT and greatly increases its spectral resolution. This, in turn, allows us to more accurately evaluate the spectral response of the A/D converter.

When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when an integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (f_{in}) and the sample rate (f_s), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the record, must be a power of 2 integer.

Further, f_{in} (signal input frequency) and f_s (sampling rate) should be locked to each other to provide an exact frequency relationship between the two frequencies (f_{in} and f_s).

"No Windowing" (an FFT Option under WaveVision) should be selected for coherent sampling.

5.2.5 Troubleshooting

PWR LED (D11) is not lit:

- Be sure that the proper voltage is supplied to either board and that the FutureBus connectors of the ADC08B200 evaluation board and of the WaveVison Data Capture Board are properly aligned with each other and are completely seated.
- Be sure the polarity of the power supplied is correct.
- Check for the presence and integrity of resistors R59, R60, R61 and R62.

There is no output (or flat line) from the ADC08B200:

- Be sure there is a signal input and that the input filter will pass the frequency of the signal source. Check signal presence at TP5.
- The device may be in one of its power down modes. Be sure there is no shorting jumper on JP1 (PDADC) or on JP7 (PD). LEDs D1 and D6 should be off.
- Be sure that the proper voltage and polarity is present at Power Connector P1. If power is coming from the WaveVision Data Capture Board, 5V should still be present at P1 and at TP13.
- Be sure there is a voltage of 2.4V or greater on L1.
- Be sure there is a clock signal present at ADC08B200 pin 46.

Dynamic performance is very bad.

- Be sure to insert an adequate band pass filter between the signal source and the ADC08B200 board.
- Try changing the position of the OEDGE jumper (JP8).

Output is distorted

- Be sure the input signal is not over range
- Be sure the clock signal is between 600mVp-p and 2.5Vp-p.

The only output codes from the ADC08B200 are 00h and FFh and they can only be seen when there is an RCLK signal:

- The device may be in the test mode. Be sure there is a shorting jumper on JP8 (OEDGE).
- VRT and VRB may be the same voltage. Avoid having the shorting jumper on JP5 pins 1 & 2 at the same time that there is a shorting jumper on JP4 pins 5 & 6.
- Be sure that the input signal is not grossly over range.

The reference voltages are not as expected:

- Be sure that the jumpers are at the correct positions of JP4 and JP5.
- Realize that there is a voltage drop across resistors R28 and R27.
- An incorrect voltage at the connection between R7 and U3 could indicate a faulty U3 or incorrect R7 value.

6.0 Evaluation Board Specifications

Board Size:	4.5" x 5.65" (11.4 cm x 14.3 cm)
Power Requirements:	+ 5V ±5% @ 250 mA
Clock Frequency Range:	1 MHz to 200 MHz
Clock Amplitude	600mVp-p to 2.5Vp-p
Analog Input	
Nominal Voltage:	$1.6V_{P-P}$
Frequency Range	100 kHz to 150 MHz
Impedance:	50 Ohms

7.0 Hardware Schematic

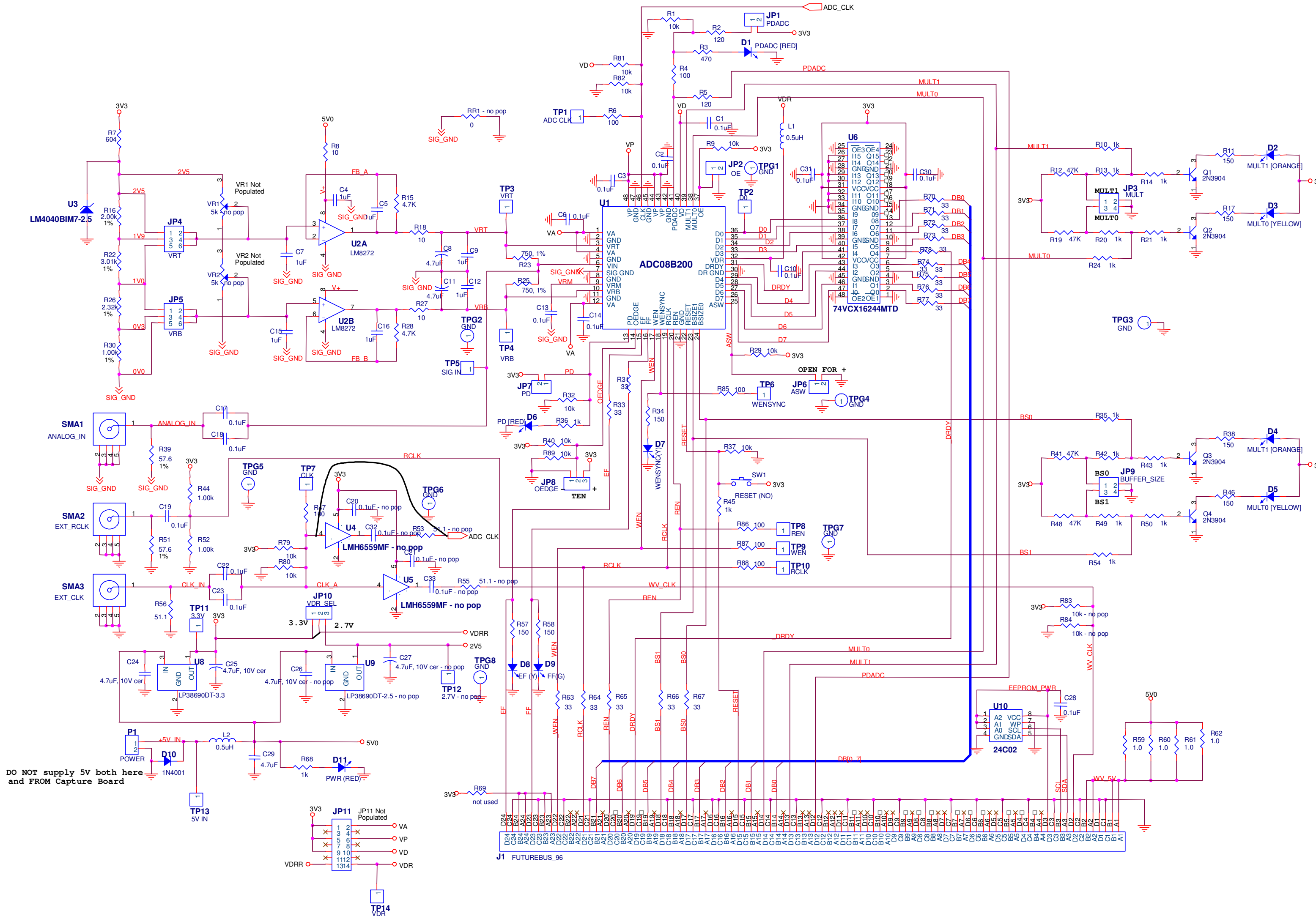

Figure 2. ADC 08B200 Evaluation Board Schematic

8.0 ADC08B200 Evaluation Board Bill of Materials

Item	Qty	Reference	Part	Source
1	4	C10, C28, C30, C31	0.1uF	**AVX #0805ZC104MAT2A**
2	11	C1, C2, C3, C6, C13, C14, C17, C18, C19, C22, C23	0.1uF, Low ESL	AVX #0508ZC104MAT2S
3	7	C4, C5, C7, C9, C12, C15, C16	1uF	**AVX #0805ZC105MAT2A**
4	7	C8, C11, C24, C25, C29	4.7uF, 10V cer	**AVX #0805ZG475ZAT2A**
5	-	C20, C21, C26, C27, C32, C33	Not Populated	Not Populated
6	3	D1, D6, D11	RED LED	LITE-ON #LTST-C930KAKT
7	2	D2, D4	ORANGE LED	LITE-ON #LTST-C930EKT
8	2	D3, D5, D7, D8	YELLOW LED	LITE-ON #LTST-C930YKT
9	1	D9	GREEN LED	LITE-ON #LTST-C930GKT
10	1	D10	1N4001	Various - axial leads
11	4	JP1, JP2, JP6, JP7	1 x 2 Header	Molex#22-28-4133
12	1	JP8	1 x 3 Header	
13	2	JP3, JP9	2 x 2 Header	Molex#10-89-2321
14	2	JP4, JP5	2 x 3 Header	
15	-	JP10	Hard Wired	Hard Wired
16	-	JP11	Hard Wired	Hard Wired
17	1	J1	FutureBus Connector	AMP/Tyco 5223514-3
18	1	L1, L2	0.5uH Choke	JW Miller #FB20010-3B-RC
19	1	P1	Terminal Block	On Shore Technology #ED120/2DS
20	4	Q1, Q2, Q3, Q4	MMBTN3904	Fairchild Semiconductor
21	11	R1, R9, R29, R32, R37, R40, R79, R80, R81, R82, R89	10kΩ, 5%, 1/10W, 0805	Rohm #MCR10EZPJ103
22	2	R2, R5	120Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ121
23	1	R3	470Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ471
24	7	R4, R6, R47, R85, R86, R87, R88	100Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ101
25	1	R7	604Ω, 5%, 1/10W, 0805	Panasonic #ERJ-S06F6040V
26	3	R8, R18, R27	10Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ100
27	15	R10, R13, R14, R20, R21, R24, R35, R36, R42, R43, R45, R49, R50, R54, R68	1kΩ, 5%, 1/10W, 0805	Rohm #MCR10EZPJ102
28	7	R11, R17, R34, R38, R46, R57, R58	150Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ151
29	4	R12, R19, R41, R48	47kΩ, 5%, 1/10W, 0805	Rohm #MCR10EZPJ473
30	2	R15, R28	4.7kΩ, 5%, 1/10W, 0805	Rohm #MCR10EZPJ472
31	1	R16	2.00kΩ, 1%, 1/10W, 0805	Rohm #MCR10EZPF2001
32	1	R22	3.01kΩ, 1%, 1/10W, 0805	Yageo #RC0805FR-073K01L
33	2	R23, R25	750Ω, 1%, 1/10W, 0805	Rohm #MCR10EZPF7500
34	1	R26	2.32kΩ, 1%, 1/10W, 0805	Rohm #MCR10EZPF2321
35	3	R30, R44, R52	1.00kΩ, 1%, 1/10W, 0805	
36	16	R31, R33, R63, R64, R65, R66, R67, R70, R71, R72, R73, R74, R75, R76, R77, R78	33Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPF33R0
37	2	R39, R51	57.6Ω, 1%, 1/10W, 0805	Rohm #MCR10EZHF57R6
38	1	R56	51.1Ω, 1%, 1/10W, 0805	Rohm #MCR10EZHF51R1
39	4	R59, R60, R61, R62	1.0Ω, 5%, 1/10W, 0805	Rohm #MCR10EZPJ1R0
40	-	R53, R55, R69, R83, R84	Not Populated	Not Populated
41	3	SMA1, SMA2, SMA3	SMA connectors	Amphenol #901-144-8RFX or Johnson #142-0701-201
42	1	SW1	Switch, NO	E-Switch #TL59CF160Q
43	21	TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11, TP13, TP14, TPG1, TPG2, TPG3, TPG4, TPG5, TPG6, TPG7, TPG8	Test Points	Molex #22-28-4323
44	-	TP12	Not Populated	Not Populated
45	1	U1	ADC08B200CIVS/NOPB	National Semiconductor
46	1	U2	LM8272MM/NOPB	National Semiconductor
47	1	U3	LM4040BIM7-2.5/NOPB	National Semiconductor
48	1	U6	74VCX16244MTD	Fairchild Semiconductor
49	1	U8	LP38690DT-3.3/NOPB	National Semiconductor
50	1	U10	AT24C02N-10SA-2.7C	Atmel
51	-	U4, U5, U7, U9	Not Populated	Not Populated
52	-	VR1, VR2	Not Populated	Not Populated
53	9	2-Pin Shorts	Shorting Jumpers	3M #929957-08

APPENDIX

Summary Tables of Test Points and Connectors

Test Points on the ADC08B200 Evaluation Board

TP 1	ADC CLK Signal
TP 2	D0 - ADC LSB Output
TP 3	VRT - Upper Reference Voltage
TP 4	VRB - Lower Reference Voltage
TP 5	Analog Signal input
TP 6	WENSYNC
TP 7	Does not exist
TP 8	REN Signal
TP 9	WEN Signal
TP 10	RCLK Signal
TP 11	3.3V
TP 12	2.7V (if U9 populated)
TP 13	5V Input to board
TP 14	VDR

SMA Connectors

SMA1	ADC Analog Input
SMA2	External RCLK Input
SMA3	External CLK Input

P1 Connector - Power Supply Connections

J1-1	+5V	Positive Power Supply
J1-2	GND	Power Supply Ground

J1 Connector - ADC Data Outputs - Connection to WaveVision Data Capture Board

Signal	J1 Pin Number
ADC output D0	B14
ADC output D1	B15
ADC output D2	B16
ADC output D3	B17
ADC output D4	B18
ADC output D5	B19
ADC output D6	B20
ADC output D7	B21

Jumper Connections

Jumper	Pins Shorted	Action
JP1 - PDADC	none	ADC active if PD active
	1 - 2	ADC Powered down; Buffer & outputs Active
JP2 - OE	none	Enable Digital Outputs
	1 - 2	Disable Digital Outputs (Hi-Z)
JP3 - MULT	none	ADC CLK is sample rate
	1 - 2	Sample clock is 4 x CLK frequency
	3 - 4	Sample clock is 2 x CLK frequency
	1 - 2 & 3 - 4	Sample clock is 8 x CLK frequency
JP4 - VRT	none	not allowed - do not leave jumper complete off
	1 - 2	VRT set to 2.5V
	3 - 4	VRT set to 1.9V
	5 - 6	VRT set to 1.0V
JP5 - VRB	none	not allowed - do not leave jumper complete off
	1 - 2	VRB set to 1.0V
	3 - 4	VRB set to 0.3V
	5 - 6	VRB set to 0V [U2 saturation will limit minimum voltage]
JP6 - ASW	none	Autostop Write enabled
	1 - 2	Autostop Write disabled
JP7 - PD	none	Device active
	1 - 2	Entire chip powered down
JP8 - OEDGE	none	Device in Test Mode
	1 - 2	Data transitions at fall of DRDY
	2 - 3	Data transitions at rise of DRDY
JP9 - Buffer Size	none	Buffer not used - output rate is ADC sample rate
	1 - 2	256 byte buffer used - output rate is RCLK
	3 - 4	512 byte buffer used - output rate is RCLK
	1 - 2 & 3 - 4	1024 byte buffer used - output rate is RCLK
JP10 - VDR Select	-	Not populated
JP11 -		Not populated

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The ADC08B200 Evaluation Board is intended for product evaluation purposes only and is not intended for resale to end consumers, is not authorized for such use and is not designed for compliance with European EMC Directive 89/336/EEC.

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