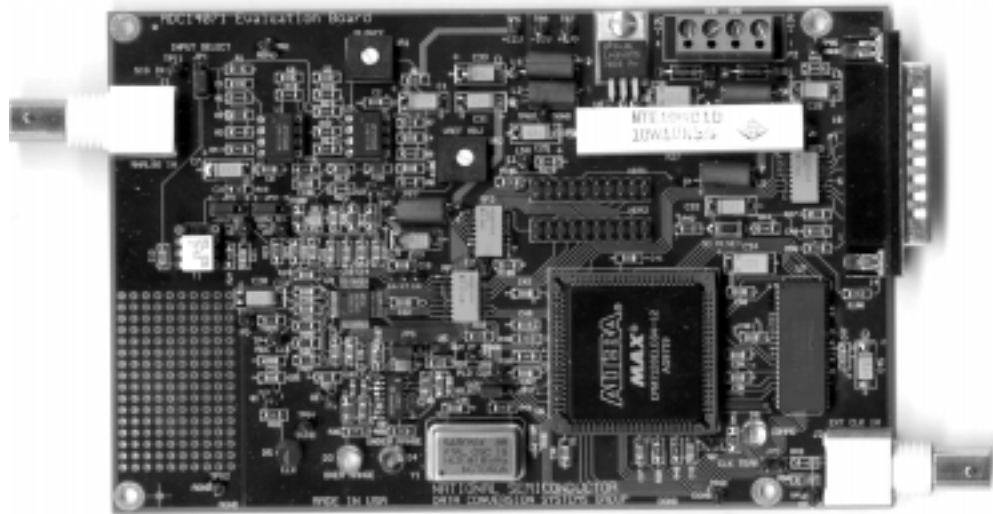


# Evaluation Board Instruction Manual

## ADC14071 14-Bit, 7 MSPS, 390mW Analog-to-Digital Converter



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# Table of Contents

1.0 Introduction.....	5
2.0 Quick Start .....	5
3.0 Functional Description .....	5
3.1 Input signal conditioning.....	5
3.2 ADC reference circuitry.....	5
3.3 Board Outputs.....	6
3.4 Board Control.....	6
3.5 Data Memory.....	6
3.6 Computer Interface.....	6
3.7 Power requirements.....	6
4.0 Installing and using the ADC14071 Evaluation Board and WaveVision Software.....	6
4.1 Software Installation .....	7
4.2 Setting up the ADC14071 Evaluation Board .....	7
4.2.1 Board Set-up.....	7
4.2.2 Quick Check of Analog Functions .....	7
4.2.3 Quick Check of Software and Computer Interface Operation .....	7
4.2.4 Getting Consistent Readings.....	8
4.2.5 Jumper Information.....	8
4.2.6 Troubleshooting.....	8
5.0 Exploring the Waveform.....	9
5.1 Signal Purity .....	9
5.1.1 Evaluating a Sine Wave.....	9
5.1.2 Low Frequency Triangle Wave Input.....	9
5.1.2.1 Monotonicity and Uncertainty.....	9
5.1.2.2 Rising / Falling Symmetry .....	10
5.2 The FFT Plot .....	10
5.2.1 Dynamic Performance Estimates .....	10
5.2.2 Bandwidth Estimation .....	10
6.0 Computer-Board Communications .....	10
7.0 Circuit Description and Hardware Schematics.....	10
7.1 Input, Reference and Test Device Section.....	10
7.2 Control, Memory, Communications and Power Supply Section .....	10
7.3 The Reset Button .....	10
7.4 Hardware Schematics.....	12
8.0 Bill of Materials.....	14
9.0 Saving and Retrieving Files .....	15
9.1 Binary Files.....	15
9.1 ASCII Files.....	15
10.0 Evaluation Board Specifications .....	15
APPENDIX - WaveVision Screens .....	16

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## 1.0 Introduction

The ADC14071EVAL Design Kit (consisting of the ADC14071 Evaluation Board, National's WaveVision software and this manual) is designed to ease evaluation and design-in of National's ADC14071 14-bit, 7MSPS Analog-to-Digital Converter.

With the WaveVision software operating under Microsoft Windows 3.1 or later, the signal at the Analog Input is digitized and can be captured and displayed on the computer monitor as a dynamic waveform. The digitized output is also available at a pair of headers, HDR1 and HDR2, for easy connection with ribbon cables.

The software can perform an FFT on the captured data upon command and display a spectral plot. This spectral plot also shows dynamic performance in the form of SNR, SINAD, THD and SFDR.

Both a socketed transformer and an op-amp-based single-ended to differential conversion circuit are available with jumpers to select which is used. A prototype area is available for building customized input conditioning circuitry.

The on-board clock oscillator is stated as being 14MHz in this manual, but the popular 14.31818MHz crystal is quite acceptable and provided with the assembled board.

Because this board uses software that is also used for the 2.5 MSPS ADC16061, you will see references in this manual to the ADC16061.EXE software. For the ADC14071, be sure to use Version 2.1 or later of the ADC16061.EXE software with the ADC14071 choice in the Configuration Menu.

## 2.0 Quick Start

1. Unless the ADC14071 Evaluation Board has been pre-assembled, it needs to be assembled before operation. Refer to *Figure 1* for the location of major components on the board. Refer to section 8.0 for the bill of materials.
2. Connect a cable with DB-25 connectors between connector P1 on the board and an available parallel port on your PC.
3. Position jumpers JP4 and JP5 to their default position as indicated in *Figure 1*. Position jumpers JP1, JP2 and JP3 opposite to their default positions.
4. Connect voltage sources ( $\pm 12V$  to  $\pm 15V$ ) and ground to Power Connector P2 and turn on the power.
5. Press the RESET button (S1).
6. Adjust VR2 for 2.0V at TP1. This sets the ADC14071 reference voltage.
7. Adjust VR1 (Balance) for equal dc voltages at TP12 and TP13 (near JP2 and JP3).
8. Copy Version 1.1 or later of the WaveVision software (ADC16061.EXE) to the desired computer hard drive directory and RUN it.
9. Connect a 50 Ohm signal generator to BNC J1 and adjust its output for a signal excursion between the limits of -0.5V and +0.5V. **Be careful not to overdrive the ADC14071 input.**
10. To use the op-amp-based single ended to differential conversion circuit, place jumpers JP1, JP2 and JP3

opposite to their default positions. To use the transformer T1, place jumpers JP1, JP2 and JP3 to their default positions. When using the transformer, the signal level at BNC J1 should be about  $2V_{p-p}$ .

11. Adjust the signal level so that LEDs D34 and D4 are not on.
12. With the WaveVision software, select the parallel port (under the Options menu) that is to be used.
13. Capture data by pressing CTRL-X.
14. Perform an FFT on the data that was acquired by pressing CTRL-F.

Note that earlier versions of the ADC16061 software may be used with the ADC14071 evaluation board. However, the following exceptions/changes should be noted. The default oscillator divider (Board to ADC Clock Ratio) shown when CTRL+P is pressed is "8", which really causes a divide by 4 for the ADC14071 board. So with a 14.31818MHz crystal in place, the ADC clock frequency would be 3.579545MHz. The divide by ratio should be changed to "4", which will yield a divider of 2 and an ADC clock frequency of 7.15909MHz. When performing an FFT on the captured waveform, it will be necessary to change the indicated Sampling Rate for the data if the horizontal axis of the display is changed to frequency. You can make this change by double clicking the left mouse button with the cursor over the FFT display.

## 3.0 Functional Description

*Figure 7* shows the block diagram of the ADC14071 evaluation board, while *Figures 8* and *9* show the board schematic. U4 is the ADC14071 under test.

### 3.1 Input signal conditioning.

The board contains a breadboard area to be used as needed. The input signal to be digitized should be applied to BNC connector J1. For sinusoidal input signals you should include an appropriate bandpass filter in the input circuitry because the signal from any generator will usually contain more distortion than that produced by a 14-bit ADC. Without the input filter, the measured performance will not be as good as the ADC14071 capability.

Note that the input signal to the ADC14071 should not swing below ground, or go above the ADC14071 analog supply,  $V_A$ , to avoid damage to the device. To avoid signal clipping at the ADC output, the signal at the ADC input pins should have a peak-to-peak value less than  $V_{REF}$ , centered around  $V_{REF}/2$ .

To get the correct differential  $4V_{p-p}$  centered at  $V_{REF}/2$  at the ADC14071 input, the transformer requires a  $2 V_{p-p}$  signal at J1, while the op-amp circuit requires a  $1 V_{p-p}$  signal centered at 0V to be applied at J1.

### 3.2 ADC reference circuitry.

The ADC14071 operates with a nominal reference voltage of 2.0V. The acceptable reference voltage range is

$$1.0V \leq V_{REF} \leq 2.7V.$$

This board, if assembled, comes with a LM4041-ADJ adjustable reference. The nominal range of adjustment in this circuit is 1.3V to 2.8V.

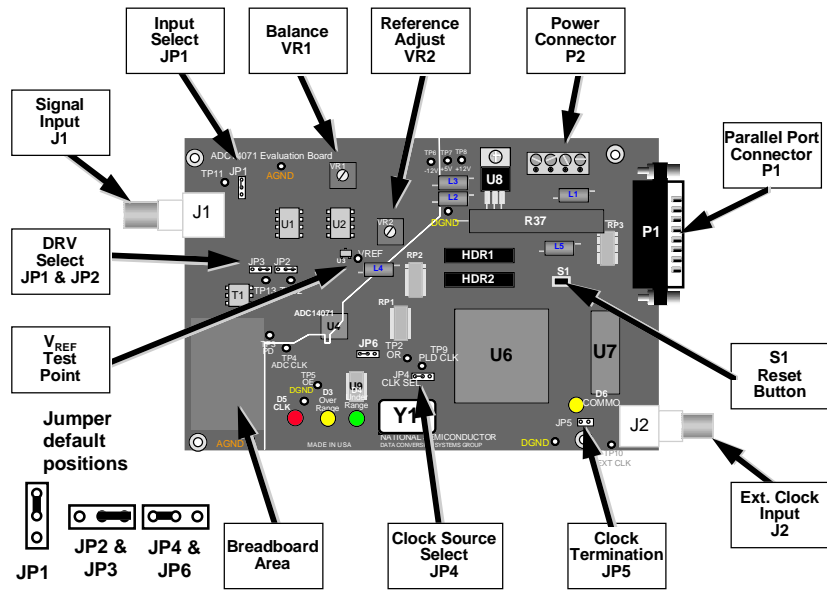


Figure 1. Component and Test Point Locations

### 3.3 Board Outputs.

Uploading of data to a PC running WaveVision is accomplished through Parallel Port connector P1.

The buffered digital data from the ADC14071 output, as well as a clock signal for this data, is available at 20 pin headers HDR1 and HDR2. These connectors have all the even numbered pins grounded and are suitable for connecting ribbon cables to the board.

LEDs provide visual indication of the condition of the board. Red LED D5, when lit, indicates that a clock signal is present at the clock input to the ADC14071. Yellow LED D6 indicates the status of board-PC communications. The board is sending data to the computer when this LED is on.

Two LEDs are provided as an indicator that the input to the ADC is beyond the ADC's range. Yellow LED D3 indicates when the input is beyond the maximum positive range, while Green LED D4 indicates when the input is beyond the lowest negative value allowable to avoid signal clipping. Input signal levels that just prevent these LEDs from coming on will provide maximum SNR performance.

### 3.4 Board Control.

PLD U6 is a state machine that performs the control functions of the board. It also contains registers and logic used to move data. The functions of this device are:

- Write acquired data to RAM.
- Accept and interpret commands from the computer.
- Divide the clock input frequency per command.
- Upload data in RAM to PC via parallel port.

### 3.5 Data Memory.

The data memory consists of a single 64k x 16 RAM chip, U7. Data is written to RAM from the ADC14071 by way of PLD

U6. During data acquisition, the RAM address is incremented by U6. After the data is gathered and loaded into RAM, it is read from RAM by U6 and sent over the computer-board cable. The number of words sent is determined by the instructions from the host computer.

### 3.6 Computer Interface.

The board communicates with a host computer through a parallel interface. The data path is through the DB-25 connector P1, located at the right side of the board. The parallel interface uses a PC parallel port that must support either EPP mode or ECP mode.

### 3.7 Power requirements.

Power is supplied to this board through power connector P2 at the top right of the board. The board requires 1 Amp at +12V to +15V and 10mA at -12V to -15V. The board is protected from accidental polarity reversal with series diodes in both the positive and negative supply lines.

### 4.0 Installing and using the ADC14071 Evaluation Board and WaveVision Software

The evaluation board requires power as described in paragraph 3.7. No input signals for evaluation are generated on the board. An appropriate signal generator (such as HP8662A) with a 50- to 75-Ohm source impedance should be used to evaluate the performance of the ADC14071. The generator output should be filtered by a bandpass filter when evaluating sinusoidal signals to eliminate unwanted frequencies (harmonics and noise) from the generator. This will provide dynamic readings that are a more accurate assessment of the converter performance than you would obtain without the filter. This is because even the best signal

generators can not provide a level of distortion low enough to evaluate high resolution ADCs.

#### 4.1 Software Installation

The WaveVision software provided requires 300k bytes of hard drive space and will run under Windows 3.1 or later.

1. Insert the disk into a 3.5" floppy drive.
2. Copy the program ADC16061.EXE to the desired subdirectory on your computer's hard disk and RUN it.

#### 4.2 Setting up the ADC14071 Evaluation Board

This evaluation package was designed to be easy and simple to use, and to provide a quick and simple way to evaluate the ADC14071. The procedures given here will help you to properly set up the board.

##### 4.2.1 Board Set-up

Refer to *Figure 1* for locations of connectors, test points and jumpers on the board.

1. Set jumpers to their default position, or as desired. *Table 1* explains the function of the jumpers. Jumpers JP1, JP2 and JP3 should all be moved together. That is all of these should be either in their default positions or all not in their default positions.
2. Connect power to the board per requirements of paragraph 3.7.
3. Connect a cable with DB-25 connector between board connector P1 and a parallel port on your computer.
4. Be sure a 14MHz (14.31818MHz is fine) clock oscillator (Y1) is in place, or connect an external clock source to BNC J2, at the lower right corner of the board.
5. Be sure jumper JP4 is set to select the clock source used. The default position selects the on-board oscillator, Y1.
6. If using an external clock source, place a shorting bar across the pins of JP5 to terminate the clock input, if needed and connect a clock source to BNC J2.
7. Connect an appropriate signal source to J1.
8. Turn on the power and press reset button (S1). Confirm that Red LED D5 is on, indicating the clock presence.

##### 4.2.2 Quick Check of Analog Functions

Refer to *Figure 1* for locations of connectors, test points and jumpers on the board. If at any time the expected response is not obtained, see section 4.2.6 on Troubleshooting.

1. Perform steps 1 through 8 of Section 4.2.1. Adjust the input signal at J1 for 1V<sub>p-p</sub>.
2. JP4 - Short left two pins to select the on-board clock oscillator (Default position).
3. JP1 - Short upper two pins of JP1 and the right two pins of JP2 and JP3 to use the op-amp circuitry (Default positions).
4. Turn on the power to the board.
5. Adjust VR2 for a voltage of 2.0V at TP1.
6. Scope TP4 to confirm the presence of an ADC clock.
7. Scope the signals at TP12 and TP13 to be sure they are present at a 2V<sub>p-p</sub> level.
8. JP1 - Remove the short on the upper two pins of JP1 and the right two pins of JP2 and JP3. Short lower two pins of JP1 and the left two pins of JP2 and JP3 to use the transformer T1.

9. Adjust the signal source at Analog Input J1 for a signal amplitude of approximately 2V<sub>p-p</sub>, centered at ground.
  10. Scope the signals at TP12 and TP13 to be sure they are present at a 2V<sub>p-p</sub> level between ground and +2V.
  11. Short right two pins of JP4 to select an external clock source. Connect a clock source to BNC J2.
  12. Scope TP4 to confirm the presence of an ADC clock.
- This completes the testing of the analog portion of the evaluation board.

##### 4.2.3 Quick Check of Software and Computer Interface Operation

1. Perform steps 1 through 5 of Paragraph 4.2.2, above.
2. Turn on the power to the board and press reset button (S1).
3. Supply a 1V<sub>p-p</sub> sine wave of about 1MHz at Analog Input BNC J1 and adjust it so that yellow and green LEDs D3 and D4 are not on.
4. If only one of these LEDs is on, adjust VR2 until they are both off or both on, then go back to step 3.
5. Be sure there is an interconnecting cable between the board and your computer parallel port.
6. Run program ADC16061.EXE.
7. Acquire data by clicking on the ACQUIRE icon or by pressing ALT, E, X or CTRL-X. Data transfer and calculations can take a few seconds.
8. When transfer is complete, the data window should show many sine waves. The display may show a nearly solid area of red, which is O.K.

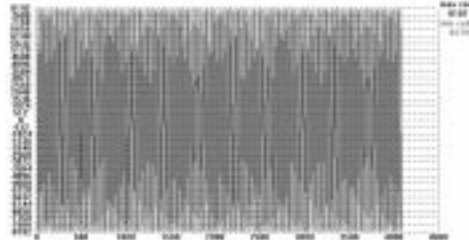


Figure 2. The WaveVision captured display of a 1MHz sine wave at 7MSPS. The input signal should be filtered to remove harmonic distortion and should be stable to prevent averaging of the data in the FFT process.

9. Note the max and min codes at the upper right of the data window. These should be within the limits of  $\pm 8190$ . If the signal is outside of these limits, the signal may be clipped (and distorted). If this is the case, lower the input level to the board and go back to step 7.
10. With the mouse, you may click and drag to select a small portion of the displayed waveform for better examination.
11. Click on the FFT icon or type ALT, E, E or CTRL-F.

The FFT data will provide a measurement of SINAD, SNR, THD and SFDR (See *Figure 3*), easing the performance verification of the ADC14071.

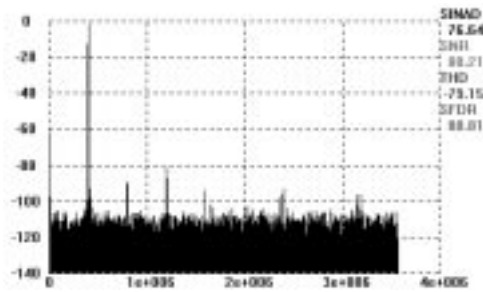


Figure 3. FFT display of the signal in Figure 2 showing performance of the ADC14071. From this display, the noise floor can be estimated and spurious signals can be identified. Note the display of SINAD, SNR, THD and SFDR to the right of the plot.

#### 4.2.4 Getting Consistent Readings

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than our measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. This greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter. Coherent sampling of a periodic waveform occurs when an integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency ( $f_{in}$ ) and the sample rate ( $f_s$ ), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be an integer number and SS, the number of samples in the record, must be a factor of 2 integer. For optimum results, CY should also be a prime number.

Further,  $f_{in}$  (signal input frequency) and  $f_s$  (sampling rate) should be locked to each other. If they come from the same generator, whatever frequency instability (jitter) is present in the two signals will cancel each other.

Windowing (an FFT Option under WaveVision) should be turned off for coherent sampling.

#### 4.2.5 Jumper Information

Table 1 indicates the function and use of the jumpers on the ADC14071 evaluation board.

JUMPER	FUNCTION	PINS 1 & 2 SHORTED	PINS 2 & 3 SHORTED
JP1	Input Select	Select Transformer	Select Op-Amp Circuit
JP2 & JP3	Select Input to drive ADC	Select Transformer	Select Op-Amp Circuit
JP4	Select Clock Source	External Clock	On-Board Clock
JP5	Ext. Clock Termination	50-Ohm Termination	No Termination

Table 1. Jumper settings.

#### 4.2.6 Troubleshooting

"Error Transmitting", "Parallel Port Time Out Error" and/or "Failed to communicate with the board on LPT1" errors mean communication was unsuccessful. Try the following:

- Be sure that the ADC14071 board is connected to a parallel printer port supporting ECP or EPP modes and has power.
- Be sure that a jumper is present on J4.
- Ascertain that a 14MHz clock oscillator is properly inserted into the socket at Y1, or that a TTL-level clock signal is present at J2. Check to see that LED D5 is on.
- Be sure cable connections are solid.
- Be sure that the board to computer cable is one with all wires present
- Be sure the correct parallel port is selected.
- Reset the evaluation board by pressing button S1 and try again.
- Be sure that the parallel port jumper within the computer or BIOS settings is set to enable bi-directional EPP or ECP modes.

If there is no output from the ADC14071, perform the following:

- Be sure proper voltages and polarities are at the correct pins of power connector P2. Check for correct voltages at TP6, TP7 and TP8 at the top center of the board.
- Look at the min/max code note at the upper right of the data window. If the signal level is very low and does not cross zero, it will be off the screen. If this is the case, press ALT,-V, A and set the Y-axis min and max so that the plot may be viewed. If you set the min higher than the max, the program will abort.
- Be sure clock signal is present at TP4.
- Check for presence of jumpers on JP1, JP2 and JP3.
- Reset the evaluation board by pressing button S1 and try again.

If the displayed waveform appears to be garbage, or if the FFT plot shows nothing but noise with no apparent signal, reset the evaluation board by pressing button S1 and try again.

If the performance is significantly better with the op-amp circuit than it is with the transformer, the transformer may need to be replaced. We have found that only one out of 10 of these transformers perform satisfactorily.

### 5.0 Exploring the Waveform

WaveVision software and the ADC14071 Evaluation Board add a new tool to the designer's toolbox. The software and evaluation board can be used to capture a signal. The captured data can then be displayed on a computer monitor and performance parameters can be estimated.

After the ADC14071 Evaluation Board has uploaded a captured waveform to the PC, WaveVision displays this waveform on the computer monitor. You should realize that any amplifier used before the ADC14071 can affect the apparent performance of the ADC because most available amplifiers exhibit more distortion than does the ADC14071. The characteristics of any transformer you may use can also affect the overall circuit performance.

See the Appendix for WaveVision screen drawings of software operation.

### 5.1 Signal Purity

Most sine wave generators can not produce a signal pure enough to adequately evaluate a 14-bit ADC. Since the SINAD of a perfect 14 bit ADC is 86dB, any input signal should be at least 6dB better than this, or have a SINAD of 92dB or better! Even very expensive, high-performance signal generators, generally, can not produce such a clean signal.

To ensure that the input signal is clean, you should insert a low pass filter in series with the signal input. Comparing the dynamic response with and without this filter is an education in itself.

The elliptic filter of Figure 4 is an example of a suitable filter. It has attenuation of about 3dB at 800 kHz, 32dB at 1MHz and 64 dB at 1.5 MHz.

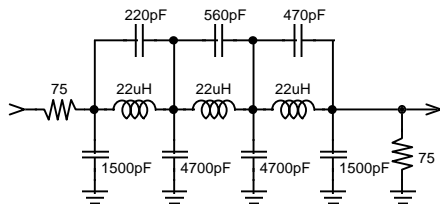


Figure 4. This elliptic filter should be driven by a generator of 50 to 75 Ohms source impedance and terminated with 50 to 75 Ohms. The input resistor shown here is normally included in the generator.

### 5.1.1 Evaluating a Sine Wave

Set the ADC clock frequency to 7MSPS as follows:

1. Be sure that a 14MHz oscillator (Y1) is in its socket, or use an external frequency source.
2. Select the Procedures pull-down menu and the Configure Board sub menu, or type CTRL P.
3. Be sure that the lower left of the dialog box indicates your oscillator frequency. Check this each time you enter this dialog box.
4. Set the clock divide by number to 2 by typing CTRL-P and changing the "Board to ADC Clock Ratio" to 2 (choices are 2 and 4 for the ADC14071).
5. Select the number of samples you wish to take. It takes longer for the computer to operate on a very large number samples, but FFT accuracy is better with more samples. If you are performing an FFT on the data, take at least 4096 samples.
6. Click on OK.
7. Connect a signal generator to input BNC J1.
8. Adjust the generator to provide a 5kHz to 6kHz output. Adjust the level so LEDs D3 and D4 do not come on.
9. Capture the signal (Procedure Execute or CTRL X) and wait for it to be displayed on your monitor.

You may select a small portion of the waveform by clicking and dragging across it.

### 5.1.2 Low Frequency Triangle Wave Input

A low frequency (about 1KHz) triangle wave will provide general information on ADC performance. If you are looking for triangle wave symmetry, compare the ADC output symmetry with that of the generator output. Many triangle wave generators do not produce a symmetrical output.

#### 5.1.2.1 Monotonicity and Uncertainty

When a voltage ramp is digitized, the code sequence shows increasing codes up to the peak level, or decreasing codes to the minimum level, depending upon whether the slope is positive or negative. A monotonic condition is one where the code sequence does not show any reversals, as in Figure 5a.

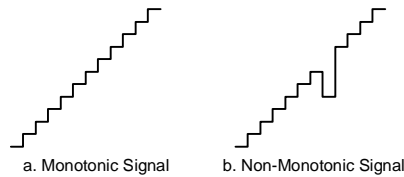


Figure 5. Monotonicity means codes are continually increasing or decreasing.

A converter that has one or more instances of codes going in the wrong direction, *always at the same point(s)*, is said to be non-monotonic. Code progression reversal at sporadic points in the waveform indicates noise in the system and not a non-monotonic condition.

When digitizing signals with rise and fall times slow enough to result in more than one conversion of the same code in sequence, it is normal to have some code uncertainty when the input is at a code transition point. See Figure 6.

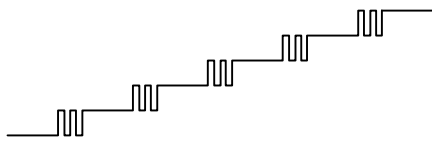


Figure 6. Code uncertainty when the ADC input voltage is near a code transition point.

#### 5.1.2.2 Rising / Falling Symmetry

The ideal analog-to-digital converter will give the same code when digitizing a given input voltage whether that voltage is approached from a lower voltage or from a higher voltage. If a triangle wave is presented to the ADC, the falling side of the waveform should be a mirror image of the rising side at the input and at the output. In practice, however, this may not be the case. Noise anywhere in the system may cause the rising and falling slopes to differ, as can the signal source itself. Looking at the WaveVision data display of a digitized triangle wave will show how symmetrical the two slopes are with respect to each other *provided the input signal has symmetrical slopes*. Choose your generator with care as many triangle wave signal generators have non-symmetrical slopes.

### 5.2 The FFT Plot

The readings of SINAD, SNR, THD and SFDR (Spurious-Free Dynamic Range) are only meaningful for a single frequency sine wave input to the ADC and are only accurate to the extent that the input waveform to the ADC14071 is clean (contains a single frequency) and is stable.

#### 5.2.1 Dynamic Performance Estimates

The dynamic performance as indicated by SINAD, SNR, THD and SFDR are estimates rather than absolute figures because their accuracy depends upon how much of the ADC14071's dynamic input range is used, how many samples are taken and at what point in the waveform the first and last samples are taken.

If the input is reduced below a full scale swing such that the minimum and maximum codes obtained at the output are  $\pm 6500$  rather than the full scale values of zero and  $-8192$  and  $+8191$ , only about 80% of the code range is used. The result is an apparent degradation of SNR. On the other hand, if the input exceeds the input dynamic range such that the top or bottom (or both) of the input signal is clipped at the ADC14071's input, THD, SFDR and SINAD will be degraded.

Furthermore, apparent performance may be limited by the purity of the input signal used, or by the non-linearities of any op-amp, transformer, or other component(s) in the signal conditioning circuitry.

#### 5.2.2 Bandwidth Estimation

If a constant amplitude frequency sweep is applied at the Analog Input (J1) and the signal at the ADC input is digitized and displayed, the data display on your computer monitor will show any frequency dependent amplitude variation. If you then perform an FFT on this data, you can effectively see the amplitude response in the form of a Bode plot.

## 6.0 Computer-Board Communications

Communication between the board and computer is through a parallel port connection at connector P1. The board responds to commands from the computer and uploads data requested by the computer.

The RAM address is incremented by PLD U6, which clocks the ADC14071 output data into RAM. The PLD counts the number of words it clocks into RAM. Once the requested number of words has been acquired and loaded into RAM, the board uploads the data to the host computer.

## 7.0 Circuit Description and Hardware Schematics

Figure 7 shows the block diagram of the ADC14071 evaluation board. U6 (a programmable logic device) controls I/O and interprets instructions from a host PC that is operating under WaveVision control. After receiving a command from the host PC, the U6 interprets it, performs the operation requested and returns the results. The board operates from supplies of  $\pm 12V$  to  $\pm 15V$ .

The hardware schematic is divided into two sections: The Input, Reference and Test Device Section, and the Control, Memory, Communications and Power Supply Section.

### 7.1 Input, Reference and Test Device Section

Figure 8 shows the input processing, reference and test device circuitry. The Analog Input at J2 will be presented to the converter through any signal conditioning circuitry that you may build or use. No anti-aliasing filter is included with the board. You should add such a filter, if needed.

Note that this board allows selection of a transformer or operational amplifiers for single-ended to differential conversion of the input signal to drive the ADC14071. Because the transformer is a high frequency one and not designed for low frequency operation, we recommend that the transformer be used only for input frequencies above 500kHz.

### 7.2 Control, Memory, Communications and Power Supply Section

The Control, Memory, Communications and Power Supply Section is shown in Figure 9. The PLD controls the functions of the evaluation board.

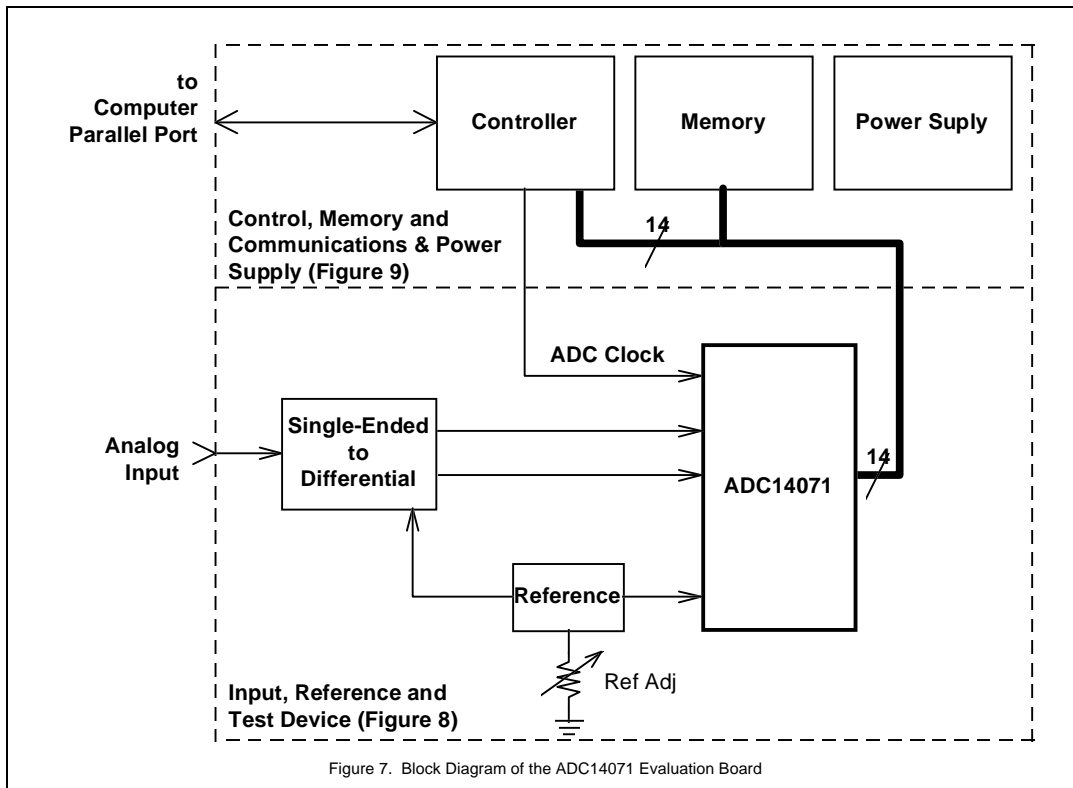
Output data from the ADC14071 is clocked directly into RAM (U7). The stored data is read from RAM and sent to the host computer by U6.

Power is brought to the board at P2. The board is protected with series diodes in the power supply lines.

The ADC14071 will operate with clock frequencies of 25kHz to 8MHz. U6 will divide the on-board clock oscillator by either 2 or 4. For a board clock rate of 14MHz, U6 provides ADC clock rates of 7MHz or 3.5MHz. The board will function with clock oscillators in the range of 50kHz to 32MHz, as long as the ADC14071 clock frequency is in the range of 25kHz to 8MHz. The ADC14071 is specified only for 7MSPS.

### 7.3 The Reset Button

The Reset button (S1) is used to reset U6. This button should be pressed after applying power to the board and any time the system does not appear to be working properly.



## 7.4 Hardware Schematics

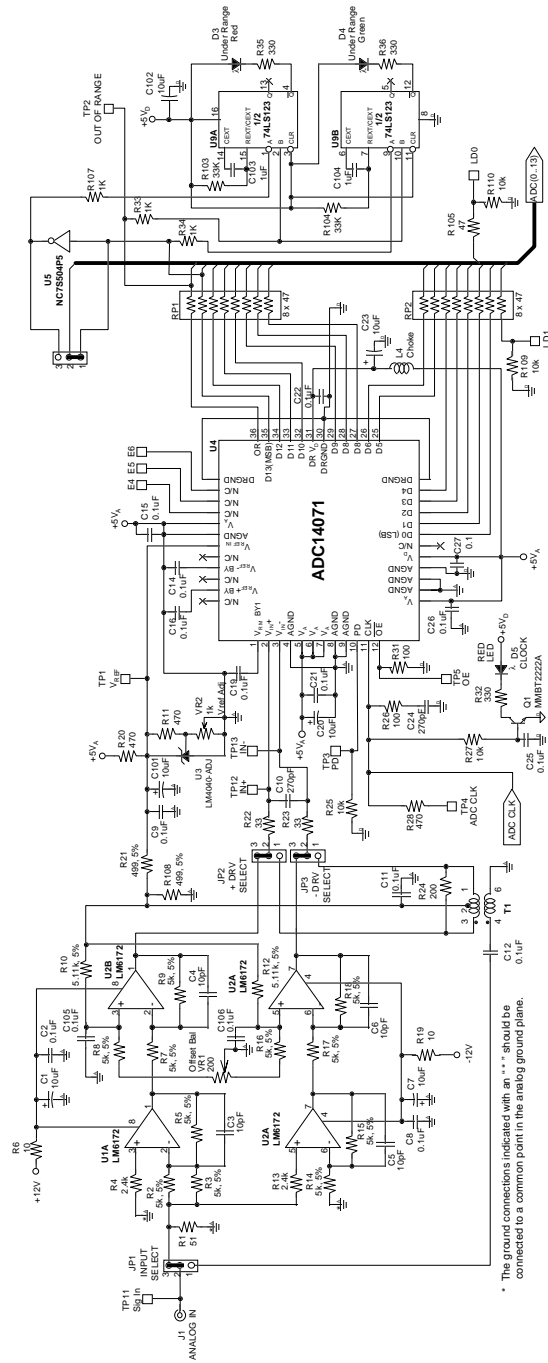


Figure 8. Input Processing, Reference and Test Device Section of the ADC14071 Evaluation Board

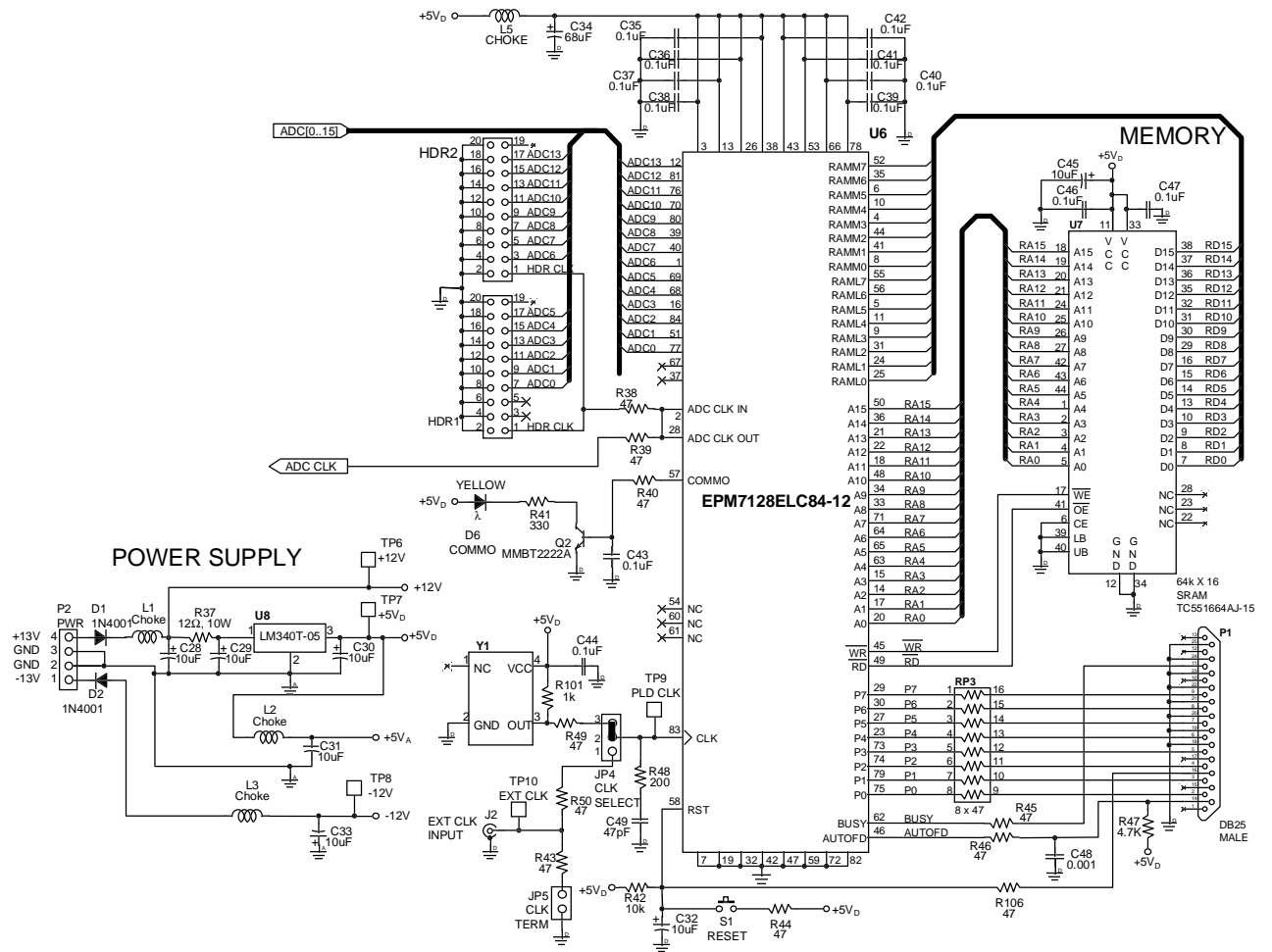


Figure 9. Control, Memory, Communications and Power Supply Section of the ADC14071 Evaluation Board

## 8.0 Bill of Materials

Item	Qty	Reference	Part	Source
1	12	C1, C7, C20, C23, C28, C29, C31, C32, C33, C45, C101, C102	10uF, 6.3V	Type 1206
2	31	C2, C8, C9, C11, C12, C13, C14, C15, C16, C17, C18, C19, C21, C22, C25, C26, C27, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C46, C47, C105, C106	0.1uF	Type 1206
3	4	C3, C4, C5, C6	10pF	Type 1206
4	2	C10, C24	270pF	Type 1206
5	2	C30, C34	68uF, 6.3V	Type 1206
6	1	C48	0.001uF	Type 1206
7	1	C49	47pF	Type 1206
8	2	C104, C103	1uF	Type 1206
9	2	D1, D2	1N4001	Various
10	2	D3, D5	RED LEDs	DigiKey # 160-1124-ND
11	1	D4	GREEN LED	DigiKey # 160-1130-ND
12	1	D6	YELLOW LED	DigiKey # 160-1133-ND
13	6	E1, E2, E3, E4, E5, E6	Future use	n/a
14	2	HDR1 HDR2	10 x 2 Headers	DigiKey # 2011-36-ND
15	5	JP1, JP2, JP3, JP4, JP6	3-Pin Post Headers	DigiKey # A19351-ND
16	1	JP5	2-Pin Post Headers	DigiKey # A19350-ND
17	6	--	Shorting Jumpers	DigiKey #S9001-ND
18	2	J1, J2	BNC Connectors	DigiKey # ARF1177-ND
19	5	L1, L2, L3, L4, L5	CHOKES	DigiKey # M2204-ND
20	1	P1	Male Connector - DB25	DigiKey # A2098-ND
21	1	P2	Terminal Block	DigiKey # ED1609-ND
22	2	Q1, Q2	MMBT2222A	Various
23	3	RP1, RP2, RP3	Resistor Pack - 8x47	DigiKey # 766-163-R47-ND
24	1	R1	51	Type 1206
25	10	R2, R3, R5, R7, R8, R14, R15, R16, R17, R18	4.99k, 1%	Type 1206
26	2	R4, R13	2.4k	Type 1206
27	2	R6, R19	10	Type 1206
28	1	R9	5k, 1%	Type 1206
29	2	R12, R10	5.11k, 1%	Type 1206
30	3	R11, R20, R28	470	Type 1206
31	1	R21	464, 1%	Type 1206
32	2	R22, R23	33	Type 1206
33	2	R24, R48	200	Type 1206
34	5	R25, R27, R42, R109, R110	10k	Type 1206
35	2	R26, R31	100	Type 1206
36	4	R32, R35, R36, R41	330	Type 1206
37	4	R33, R34, R101, R107	1k	Type 1206
38	1	R37	10, 10W	DigiKey # ALSR1J-12-ND
39	10	R38, R39, R40, R43, R44, R45, R46, R49, R50, R105	47	Type 1206
40	1	R47	4.7k	Type 1206
41	2	R103, R104	33k	Type 1206
42	1	R108	511, 1%	Type 1206
43	0	R106	not populated	n/a
44	1	S1	Push Button Switch, SPST-N.O.	DigiKey # CKN9016-ND or CKN9017-ND
45	13	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13	Breakable Headers	DigiKey # S1012-36-ND
46	1	T1	Signal Transformer	MiniCircuits type T4-6T
47	2	U1, U2	LM6172	National Semiconductor
48	1	U3	LM4041-ADJ	National Semiconductor
49	1	U4	ADC14071	National Semiconductor
50	1	U5	NC7S04P5	Fairchild Semiconductor
51	1	U6	EPM7128ELC84-15 (Needs programming)	Altera
52	1	U7	TC551664BJ-15	Toshiba
53	1	U8	LM340AT-5.0	National Semiconductor
54	1	U9	74LS123	Fairchild Semiconductor
55	1	VR1	200	DigiKey # 3386F-201-ND
56	1	VR2	1k	DigiKey # 3386F-102-ND
57	1	Y1	14.31818MHz Oscillator	DigiKey # CTX115-ND
58	1	--	6-pin Socket for Transformer	DigiKey # AE8906-ND
59	1	--	4-Pin full-size oscillator socket	DigiKey # A462-ND

## **9.0 Saving and Retrieving Files**

WaveVision allows you to save data in two formats. One is a binary file, the other is an ASCII file.

### **9.1 Binary Files**

A binary file is intended for use only by WaveVision and contains information as to program settings as well as the raw waveform data.

To save a binary file for use later by WaveVision, you can click on the Save icon, enter ALT, E, S or enter CTRL-S. You will be prompted for a file name the first time you save a given set of data.

To save a file that has already been saved, but to save it under a different file name, enter ALT, E, A. You will be prompted to enter the new file name.

To retrieve a binary file in WaveVision, you may click on the Open File icon, enter ALT, E, O or enter CTRL-O. You will be prompted for the name of the file you wish to retrieve.

### **9.1 ASCII Files**

To export (save) an ASCII file for use later by another program, such as a spreadsheet, you must enter ALT, E, D. You will be prompted for a file name. The ASCII file will contain only raw data with one data point per line.

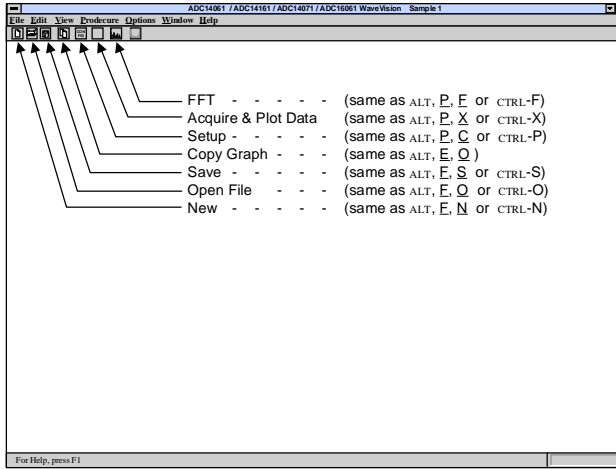
To import (retrieve) an ASCII file, whether created with WaveVision or with any other program or utility, enter ALT, E, I. You will be prompted for the name of the file you wish to retrieve. Remember that imported files must have one data point per line.

## **10.0 Evaluation Board Specifications**

Board Size:	4.5" x 6.5" (11.4 x 16.5 cm)
Power Requirements:	+12V @ 1 Amp & -12V @ 10mA
Communications:	Parallel Port
Modes Supported:	Bi-Directional EPP & ECP
Board Clock Frequency:	50kHz to 32MHz
Analog Input	
Nominal Voltage:	1 V <sub>p-p</sub> (Amps), 2 V <sub>p-p</sub> Xfmr
Minimum Excursion:	0V
Maximum Excursion:	2.7V
Memory:	64k Words by 16 bits
Reference Voltage:	2.0V, nominal

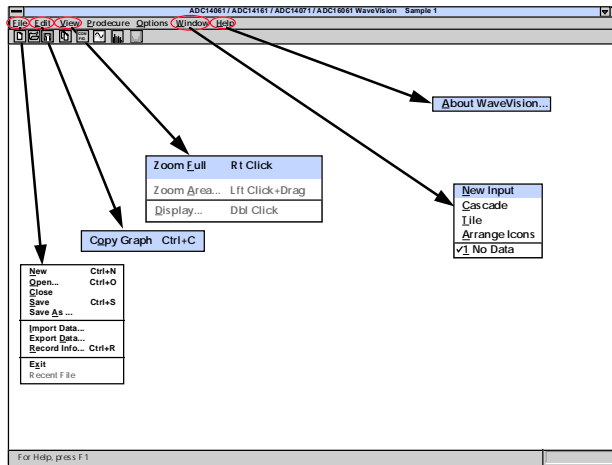
# ADC14071

## WaveVision Menu & Icon Description



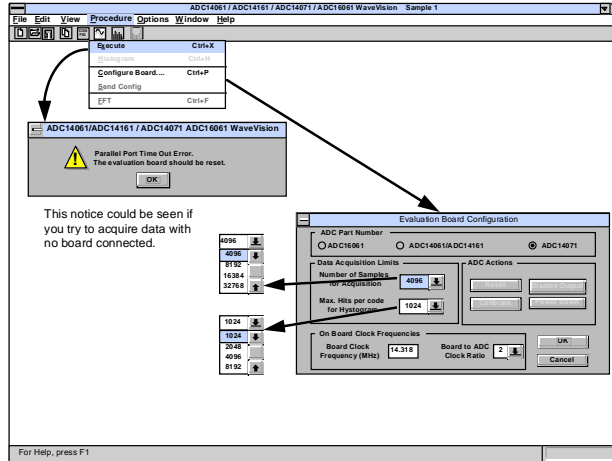
# ADC14071

## WaveVision Menu



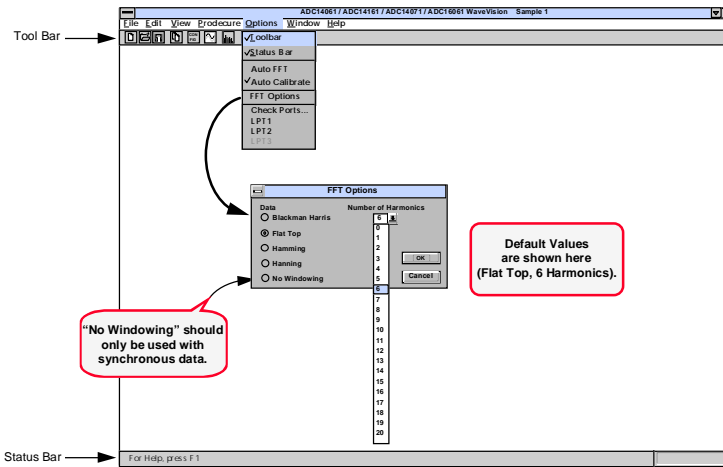
# ADC14071

## WaveVision Procedure Menu



# ADC14071

## WaveVision Options Menu



# ADC14071

## Sampled Data and FFT Data Display Options

**Sampled Data display**

Title: \_\_\_\_\_

X Axis Units:  Samples  Seconds

Y Axis Units:  Converter Codes  Volts

Sampling Rate of this data (Hz):

Vmax:  V

Vmin:  V

OK Cancel

This dialog box is obtained by double clicking on the sampled data plot.

It allows you to set a title for the displayed waveform, to set X Axis and Y Axis units and to set min and max voltage levels.

**FFT Data display**

Title: \_\_\_\_\_

X Axis Units:  Bin Numbers  Frequency

Sampling Rate of this data (Hz):

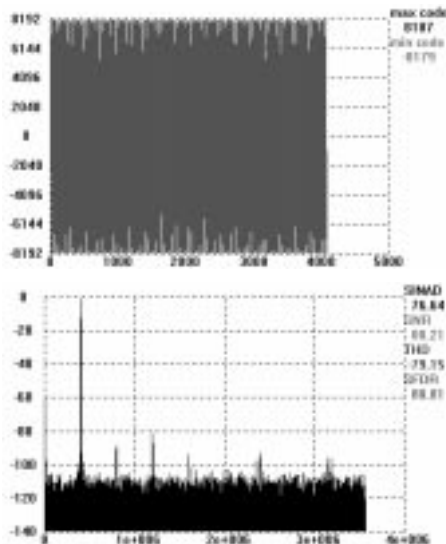
OK Cancel

This dialog box is obtained by double clicking on the FFT plot.

It allows you to set a title for the FFT and to set X Axis units

# ADC14071

## WaveVision Data Display Examples



[Blank]

The ADC14071 Evaluation Board is intended for product evaluation purposes only and is not intended for resale to end consumers, is not authorized for such use and is not designed for compliance with European EMC Directive 89/336/EEC.

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2. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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