

Video Circuit Clamps Under All Conditions

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Many video-circuit clamps operate well in the presence of a composite-video signal but cannot achieve a clamp level with signals other than composite video or in the absence of an input signal. The circuit in *Figure 1*, developed for the ADC1175 (a popular and inexpensive, high-performance, 8-bit, 20M-sample/sec ADC), provides the normal back-porch clamp function to the input of the ADC in the presence of a composite-video signal. The circuit further ensures that the voltage presented to the ADC is within its correct operating range in the absence of an input signal and forces any signal other than composite video to be within the ADC's input common-mode range.

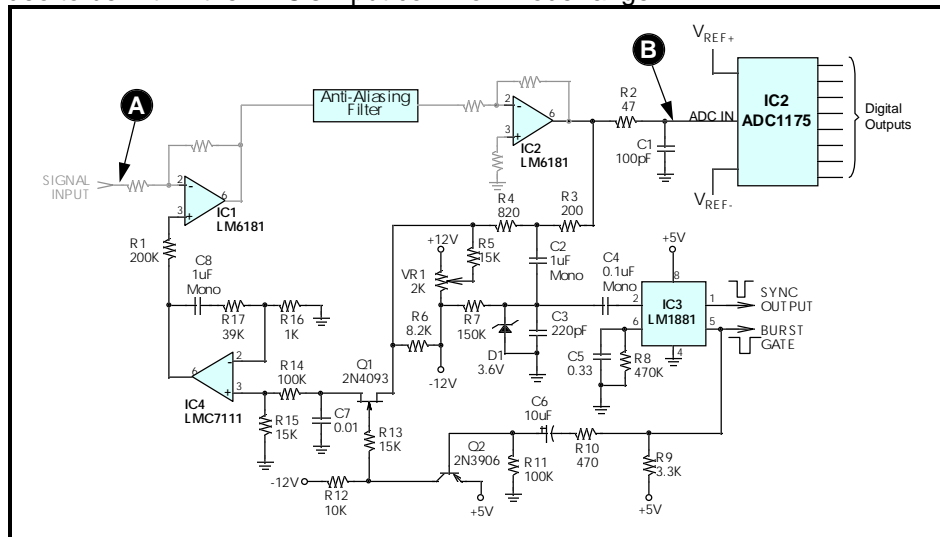


Figure 1. Video Clamp Circuit. The clamp level at "B" is independent of the average level at "A".

The circuit accomplishes video clamping by building a control loop that forces the dc voltage at IC2's output to a desired level during the blanking period. This level, approximately 25% of full scale for a composite-video signal, forces the ADC's output-pedestal (blanking) level to an 8-bit code of approximately 64. The simple filter comprising R3 and C3 bandlimits the signal at the output of IC2. This high-frequency attenuation is necessary to prevent noise spikes from upsetting the operation of the LM1881. The LM1881 is a video sync-separator chip that produces burst-gate pulses at its Pin 5 when a composite-video signal is present at Pin 2.

The burst-gate output of the LM1881 serves to sample the blanking level of the video signal. Potentiometer VR1 and R5 produce an adjustable offset in the signal path when Q1 gates on. During the blanking period, the ac-coupled burst-gate signal pulls Q2's base low (to approximately 4V), thus pulling Q1's gate high, thereby sampling and storing the sum of the video-blanking level and the dc offset from VR1 onto C7. At times other than the back-porch interval, Pin 5 of the LM1881 is high, and Q2 is off, thereby turning Q1 off. Divider R14-R15 attenuates the voltage on C7 to ensure sufficient phase margin in the clamp loop. IC4 is an integrator that averages the attenuated dc value over many samples. This average sums with the input signal in IC1.

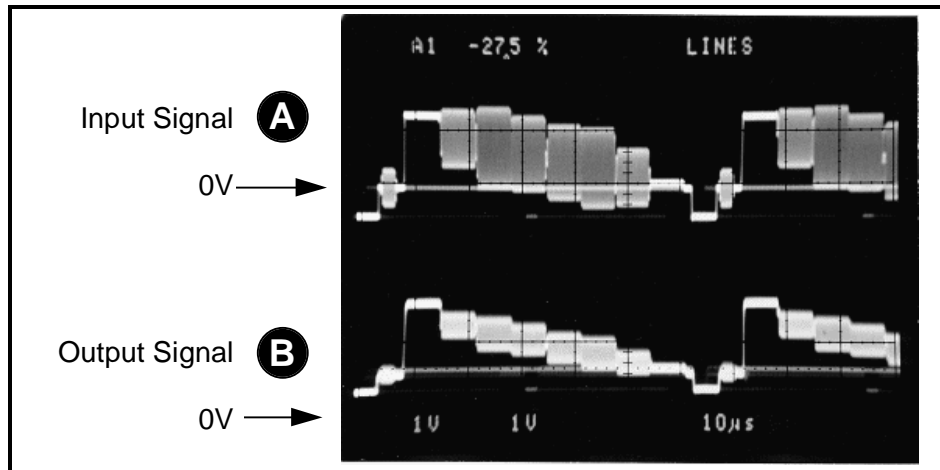


Figure 2 Oscilloscope showing offset produced at point "B" relative to point "A". Note also the gain provided.

If the integration time is too small, the result could be shading across the display. A long integration results in slow, perceptible adjustments when switching between fields with large differences in average brightness. The dc feedback path for IC4 is through IC1 and IC2. If no video signal exists or if the input signal has no sync, R11 holds Q2 on, thus holding the video output of the circuit within the ADC's operating range. With VR1 centered, the level halfway between the positive and negative peaks of the input signal clamps at approximately 1.6V, or approximately halfway between the high and low reference voltages (2.6 and 0.6V, respectively) of the ADC1175. The circuit achieves an effective number of bits of 7.5, corresponding to a signal-to-noise and distortion of 47 dB. *Figure 2* shows the offset at Point B in *Figure 1*, relative to the voltage at Point A.