

POWER | designer

Expert tips, tricks, and techniques for powerful designs

No. 103

Feature article.....1-7

DC-DC digital core and I/O power management2

Inductorless core and I/O power management4

Innovative RF signal-path power management.....6

Power design tools.....8

Understanding Portable Applications Requirements to Improve System Performance

— By Mark Davidson, Marketing Director

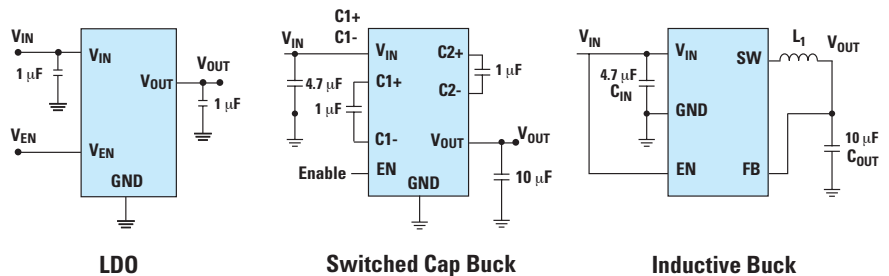


Figure 1: Common topologies for digital core power management

Until recently, power supplies were not considered an integral part of the system design. It wasn't until the last design stage that the power supply was shoved into a corner with power “rails” braided across the board. Modern techniques involve point of load where regulators are sprinkled close to their loads. But these days, especially in portable devices, neither of these techniques is acceptable. The need for longer battery life and reduced power consumption has become so important that even the digital processors themselves are being developed with power management in mind. Either implementing different power domains which can be switched on and off independently, or including voltage scaling of V_{CC} to provide the minimum allowable power for a given set of instructions prove the importance that power management plays in any system design.

When developing a highly effective power management system, designers must first start by understanding the characteristics of the source. The most common battery technology today is Li-Ion. Driven by the volume of the cell phone industry, this chemistry provides the best combination of power density and cost. The typical operating range of Li-Ion batteries is 3.0V to 4.2V. Note that many of the points which will be made in this article are also relevant to systems with fixed 3.3V rails where size and efficiency are equally important.

When it comes to selecting power management devices, many engineers simply consider input voltage, output voltage, and current requirements.

NEXT ISSUE:

Managing Power-over-Ethernet

 **National
Semiconductor**
The Sight & Sound of Information



DC-DC digital core and I/O power management

High-performing LM3670/71 synchronous buck regulators

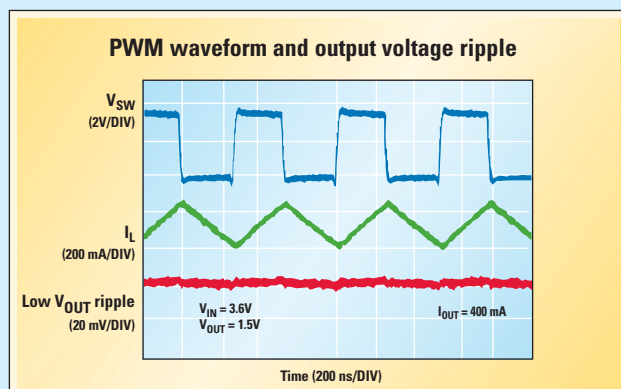
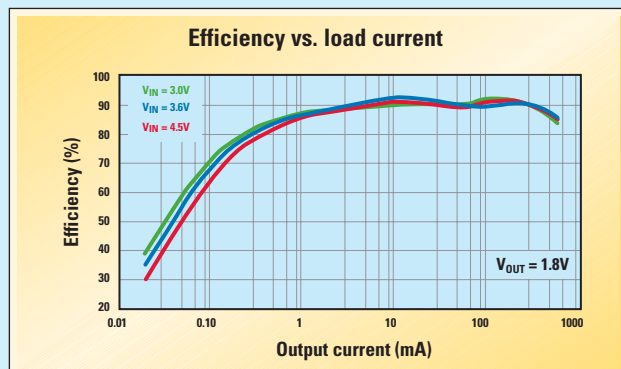
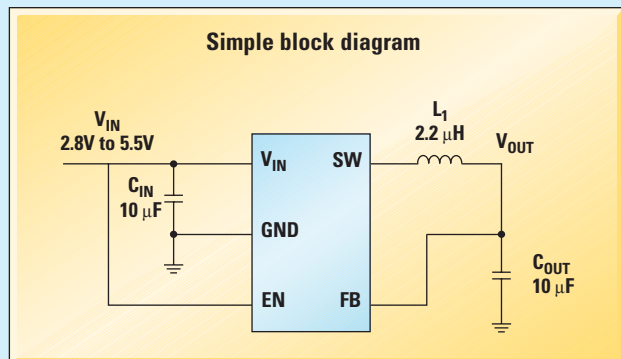
Features

- High switching frequency, ceramic capacitors, and SOT23-5 package enables an extremely small solution with industry standard components
- High load current (300 mA to 600 mA) allows flexibility in system design by supporting multiple applications
- Automatic PFM-PWM mode switching enables longer battery life and extended stand-by times
- High-output voltage accuracy, low-output voltage ripple in PFM mode, and fast transient response allow the processor to obtain peak MIPS at the lowest possible power level
- 2 MHz, 600 mA output current (LM3671) or 1 MHz, 300 mA output current (LM3670)
- Available in SOT23-5 packaging

Ideal for powering digital processors in portable systems where size and efficiency are at a premium

Product Highlight:

LM3671 achieves 95% efficiency with 2.2 μH inductor while enabling peak processors MIPS



Understanding Portable Applications Requirements

Effective power management techniques require knowledge of the type of load. In any electronic system, there are two common applications requiring power management: the digital subsystem (core and I/O) and the signal path (analog or RF). Both require a different set of trade-offs to ensure optimal performance of the system. *Figure 1* highlights the common topologies and *Table 1* highlights the priorities for digital subsystem and signal-path power.

Designing Core and I/O Power Management

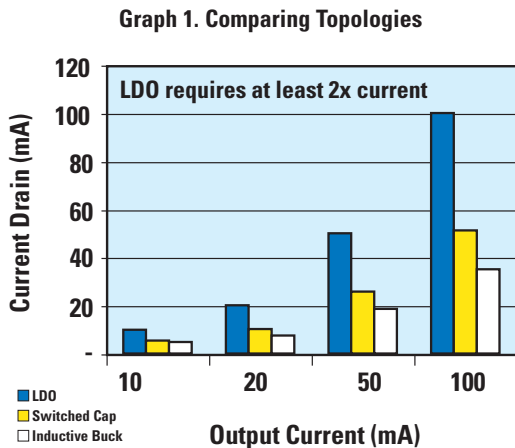
In most portable devices, the digital subsystem (processor plus digital I/O) consumes a large percentage of the total power, and in many of these systems the processor must remain on—even in a stand-by state. This need for high efficiency is further complicated by today’s digital subsystems requiring V_{CC} ’s much lower than the input source—as low as 1V. The combination of these requirements is driving the need for highly sophisticated inductive synchronous buck regulators. *Graph 1* highlights the input current drain for each of the three topologies which could be considered and highlights the

overwhelming benefit of the DC-DC converter.

The inductive DC-DC converter uses a half-bridge output stage followed by an LC filter. Its main advantage is that it can regulate a voltage with extremely high efficiency, regardless of the V_{OUT}/V_{IN} ratio. However, there are trade-offs associated with this technology, and most of these trade-offs start with the inductor. This requires careful consideration of all of the external components chosen for the circuit. The smaller the inductance value, the larger the ripple currents, so while the form factor of the system demands ultra-small components, the design engineer must understand the trade-offs. While pushing the switching frequency higher allows the use of less inductance, switching losses increase (efficiency decreases) due to the latency of turning MOSFETs on and off and the power required to charge the gate capacitance at a faster rate. FETs have capacitance between Gate and Source, so while this capacitance is “charging”, the FET is not completely in the saturation range. [The Drain-to-Source resistance (R_{DS-ON}) is not at its lowest.] For integrated DC-DC converters where the half-bridge is integrated, it is up to the IC manufacturer to minimize this effect. For controllers requiring external FETs, it is imperative to select FETs with minimal gate capacitance for a given R_{DS-ON} . The device datasheet should elaborate on this selection process.

The DC-DC converter generates an output voltage ripple proportional to the inductor current ripple multiplied by the ESR of the output capacitor.

$$\text{where } I_{\text{RIPPLE}} = \left(\frac{V_{\text{IN}} - V_{\text{OUT}}}{2 + L} \right) + \left(\frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) + \left(\frac{1}{f} \right)$$



Power Type	Voltage Range	Current Range	Performance Requirements	Predominant Topology
Digital Core	Output voltages between 1V to 2.5V	Up to 1A, but efficiency < 1 mA also important	Load-transient response, efficiency	DC-DC step-down regulator
Signal Path	Output voltages between 2.5V to 3.3V	Less than 500 mA	Noise, Power Supply Rejection Ratio (PSRR)	Low drop-out regulator

Table 1: Digital core and signal path priorities

Inductorless core and I/O power management

New LM2770/88/98 DC-DC converters provide optimal solution size and efficiency

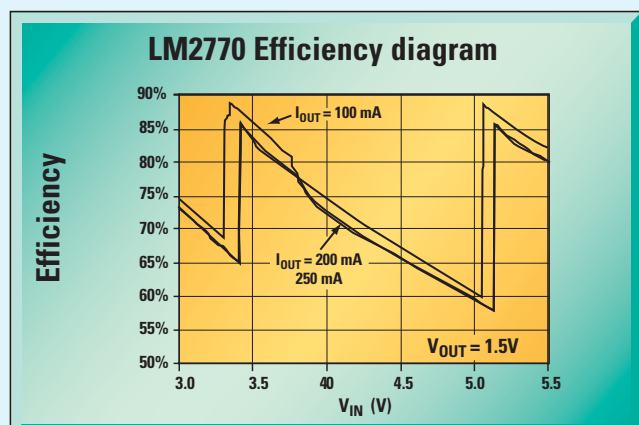
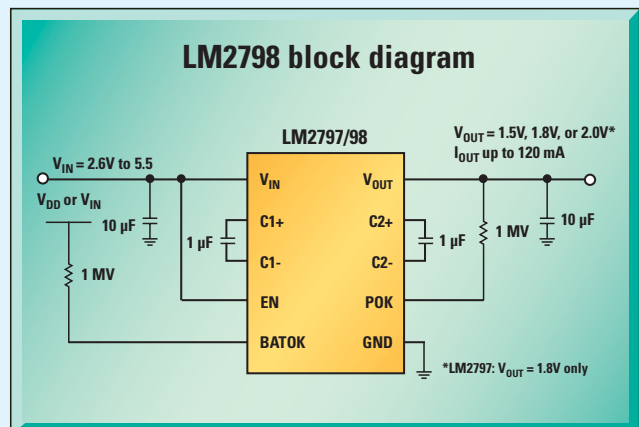
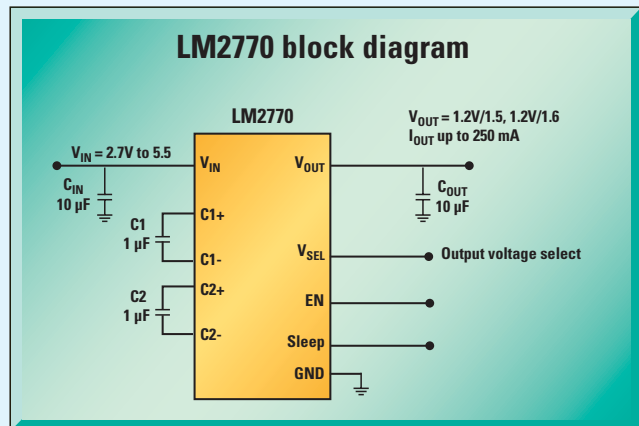
Features

- Multi-gain, gain-hopping architecture and low I_q sleep mode provide efficiency as high as 90%
- Input and output voltage monitoring helps prevent unexpected power loss and instability issues in the application
- No inductor, small capacitors, and miniature MSOP-8 and LLP-10 packages provide a small solution size and reduced BOM for application

Ideal for portable systems powered by Li-Ion or 3-cell NiMH/NiCd batteries as well as input voltage rails between 2.8V to 5.5V

Product Highlight:

New buck regulators provide up to 90% efficiency and reduce component count



Understanding Portable Applications Requirements

The ESR of the output capacitor is obtained from the capacitor datasheet, and f is the frequency of the DC-DC converter (the datasheet will specify an acceptable range of inductance values). Ceramic capacitors have the lowest ESR and should be considered whenever possible; however, the DC-DC converter must allow for their use.

While the fixed-frequency DC-DC converter is ideal for systems where the frequency range of the Di/Dt noise generated needs to be known, the efficiency at light loads suffers greatly. This is not important if the load is either “full power” or off, but when considering a digital processor or volatile memory which must remain powered during stand-by states, it is important to find a device which switches to a pulse-skipping or Pulse Frequency Modulation (PFM) scheme. In the PFM scheme, the top FET of the half-bridge is only turned on when the output voltage drops below a comparator threshold. At this time, the P-FET is turned on and the output filter is recharged. This scheme continues until the output current is detected to rise above a certain threshold and PWM operation is again required. There are two main advantages of this PFM scheme: the supply current of the DC-DC converter is greatly reduced as much of the internal circuitry is turned off and the switching losses of the output stage are minimized by only being turned on/off when required (rather than at the beginning of each time period).

As with all power management design, there is a subsequent disadvantage to this scheme. Now that the frequency is variable, the Di/Dt noise is no longer predictable. However, the optimal PFM scheme keeps the switching at or near the nominal fixed frequency during the recharge. While there is a

much slower ripple observed at the output, this is simply the charge/discharge of the output capacitor, so EMI is negligible.

Another design priority is the need for load-transient response. This is the ability of the DC-DC converter to respond to an instantaneous increase in output power (current to the load). Most modern DC-DC converters have control loops optimized for load-transient response, but once again, the external components are critical to the system performance. This characteristic still drives the need for the smallest inductor, but in this case it also drives the need for a larger output capacitor.

When the highest possible efficiency is not required, the switched capacitor buck regulator is a perfect selection. This topology achieves higher efficiency than an LDO without the use of an inductor. On average, it can achieve 70-80% efficiency for loads up to 200 mA. Modern switched capacitor bucks use a control scheme where the gains of the charge pump are changed on the fly depending on the V_{OUT}/V_{IN} ratio. By automatically changing gains, this power management device will ensure the highest possible efficiency for the given set of conditions.

Signal-Path Power

Power management for signal path devices is quite different from that of digital subsystems. Signal path devices are working with a “real-world” analog signal, so it is imperative not to lose data integrity. Thus, the top priorities for signal-path power management design are different.

The most common topology for signal-path power involves the use of a Low Drop-Out (LDO) regulator. Since the required output voltages tend to be higher

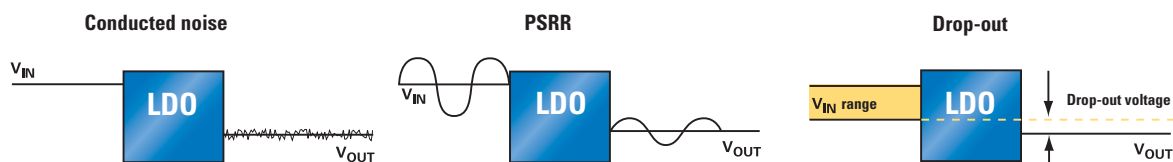


Figure 2: Important signal path parameters for portable power management

Innovative RF signal-path power management

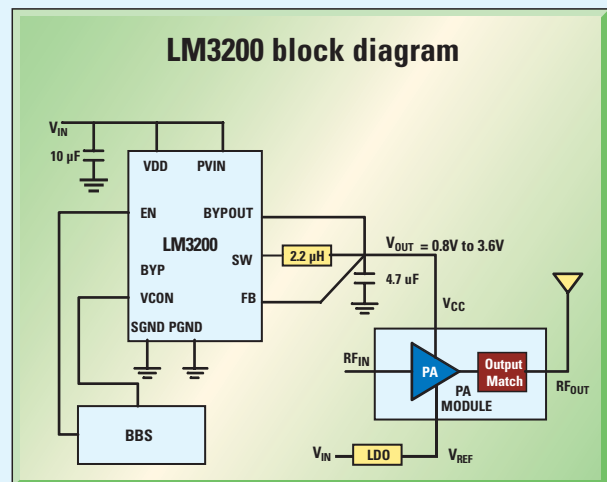
RF power amplifiers optimized for portable RF applications to increase battery life

LM3200 Features

- Dynamically adjustable output voltage maintains low RF PA power levels to optimize PA efficiency for increased battery life
- Bypass mode maintains maximum output power regardless of battery voltage.
- Small micro-SMD package and 2 MHz switching frequency minimizes size impact to RF subsystem

Product Highlight:

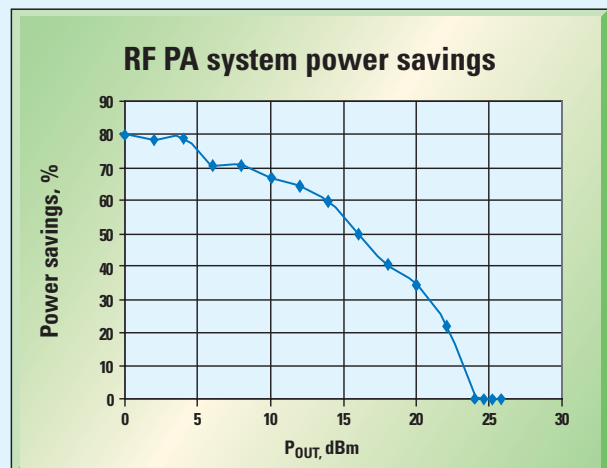
DC-DC converter delivers up to 5X transmit time in RF PAs



LP3985/95/99 Features

- Low-noise high PSRR for powering signal-path devices
- RF/analog regulators with ultra-low noise
- High power supply rejection enables clean analog signals

Ideal for powering RF power amplifiers in portable systems where solution size and efficiency are crucial



Product ID	Output Noise/Ripple	PSRR at 1kHz	Dropout at Full Load	Output Voltage	Output Current	Packages
DC-DC converter for RF PA V_{CC} supply						
LM3200	<10 mV	n/a	50 mV	0.8V to 3.6V	500 mA	micro SMD
Low-noise LDOs for RF PA V_{REF} and other RF signal path devices						
LP3985	30 µV rms	70 dB	60 mV	2.5V to 4.7V	150 mA	micro SMD, SOT-23
LP3995	25 µV rms	70 dB	60 mV	1.8V to 3.3V	150 mA	micro SMD
LP3999	25 µV rms	70 dB	60 mV	1.8V to 3.3V	150 mA	micro SMD, LLP

Understanding Portable Applications Requirements

and the output currents tend to be relatively low, the power loss of this linear device has minimal impact on overall system efficiency. The load profiles of these devices are much more steady-state, so optimization is focused more on conducted noise, Power Supply Rejection, and drop-out.

Conducted noise is the spurious, non-predictable noise that is either passed through or generated by the power management device itself. If this noise is too high, it can be passed into the signal, thus corrupting the data or reducing the system's ability to read the data. This is a very difficult parameter to understand from a datasheet as there is no common method for this specification. Unfortunately, bench analysis is the most effective way of understanding the quality of this parameter to the total system.

Power Supply Rejection is the power management device's ability to attenuate a perturbation from the input. It is measured as a ratio of a fixed-frequency sine wave at the input versus its amplitude at the output. This parameter is defined as PSR Ratio and certainly needs to be considered in conjunction with noise as the two are additive.

Drop-out is the head-room required by the LDO to generate an output from a low input. Drop-out is effectively the R_{DS-ON} of the PMOS device multiplied by the output current. As output current increases, the drop-out requirement becomes more difficult. *Figure 2* highlights the definition of each of these parameters.

Within the realm of signal-path power, there is a new emerging technology. Its application is specific to RF Power Amplifiers (PA), and it involves the use of a specialized DC-DC converter to provide the V_{CC} to the PA. So far, this application has been limited to mobile phones; however, it is starting to migrate to WLAN and other wireless protocols. *Figures 3 and 4* illustrate the PA subsystem and the placement of the DC-DC converter.

Modern PAs can maintain linearity with a V_{CC} much lower than the traditional 3V or higher and because PAs are effectively fixed impedance loads,

Figure 3: Standard PA power control

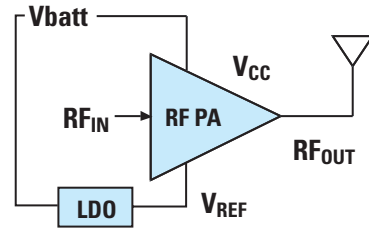
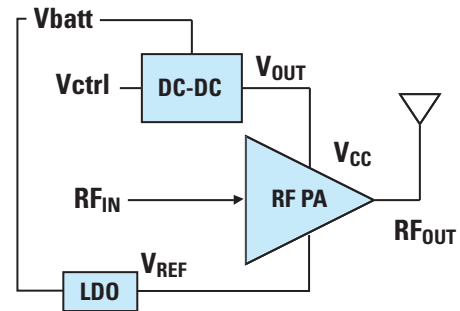


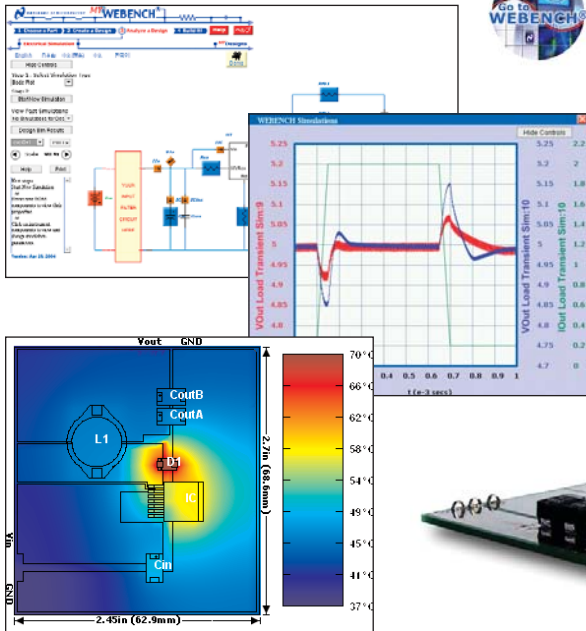
Figure 4: New PA + DC-DC converter power control



reducing the V_{CC} also reduces the current consumption. When applied to mobile phones, power consumption is reduced by 80% plus, depending on the profile of the RF transmission. The V_{CC} is changed by applying a control signal to the DC-DC converter proportional to the detected power. As less transmission power is required, the V_{CC} can be reduced, saving valuable amounts of current drain. When designing with an RF PA, designers must understand the minimum V_{CC} possible. If the PA maintains linearity down to 1.5V or lower, consider the use of these specialized DC-DC converters.

Understanding the priorities for power management design and including these decisions early in the system architecture allows engineers to optimize their system designs. And obtaining world-class features and performance while maintaining longer battery life enables OEMs to differentiate their products from their competition. ■

Power design tools

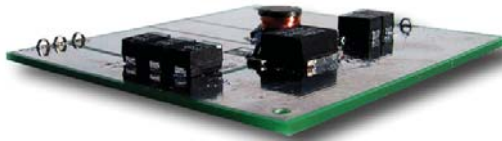


WEBENCH® online design environment

Our design and prototyping environment simplifies and expedites the entire design process.

1. Choose a part
2. Create a design
3. Analyze a power supply design
 - Perform electrical simulation
 - Simulate thermal behavior
4. Build it
 - Receive your custom prototype kit 24 hours later

www.webench.national.com



On-Demand Online Seminars

Visit our library of online seminars for pertinent design topics including:

"Practical Aspects of Magnetic Buck Converters for Portable Applications"

www.national.com/onlineSeminar

National Semiconductor

2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052
1 800 272 9959

Visit our website at:
power.national.com

For more information,
send email to:
new.feedback@nsc.com

Don't miss a single issue!



Subscribe now to receive email alerts when new issues are available:

power.national.com/designer

