BusLVDS Expands Applications for Low Voltage Differential Signaling (LVDS)

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ABSTRACT

The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is analog Low-Voltage Differential Signaling (LVDS) that designers are choosing to drive these high-speed transmission lines. LVDS's proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecom, datacom, and displays. Now, a new generation of LVDS, BusLVDS, is filling the high-speed requirements of many more applications.

This paper begins with an introduction to LVDS that covers all the basics such as what, when, and how it has become such a popular interface standard. Examples of real world applications demonstrate the key points. The paper then describes the advantages that BLVDS brings to a wider range of applications. Technical details are the focus of this section with examples used to clearly make the points. An example is Bus-LVDS enabling high-speed multipoint backplanes in Tele-communications switches. The conclusion covers why LVDS, and all it's derivatives, are the I/O technology for the twenty-first Century.

BIOGRAPHY

Stephen Kempainen

Current Activities

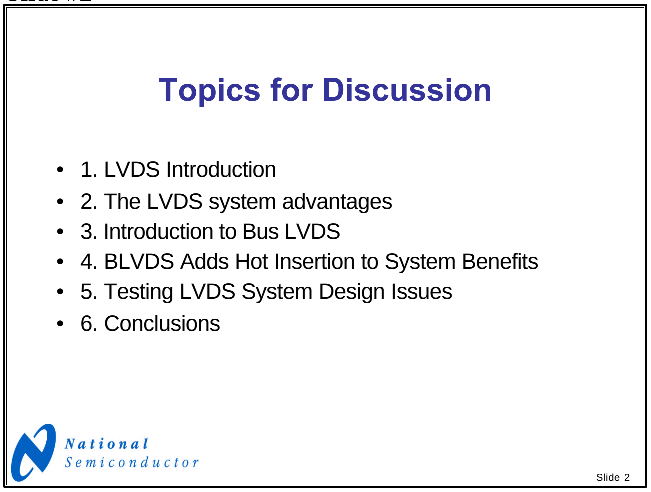
Stephen Kempainen is a Member of the Technical Staff at National Semiconductor. He serves as the system architect for new LVDS (Low-Voltage Differential Signals) products.

Background

Stephen worked for more than 2 years as a Technical Editor at EDN Magazine. His editorial responsibilities included digital design with emphasis in Communications and Networking topics. He has had 19 articles published in multiple trade journals. He is active in industry standard work and was the working group chair for the IEEE 1596.3-1996 LVDS for Scalable Coherent Interface (SCI) industry standard.

Slide #1
INTRODUCTION

Slide #2

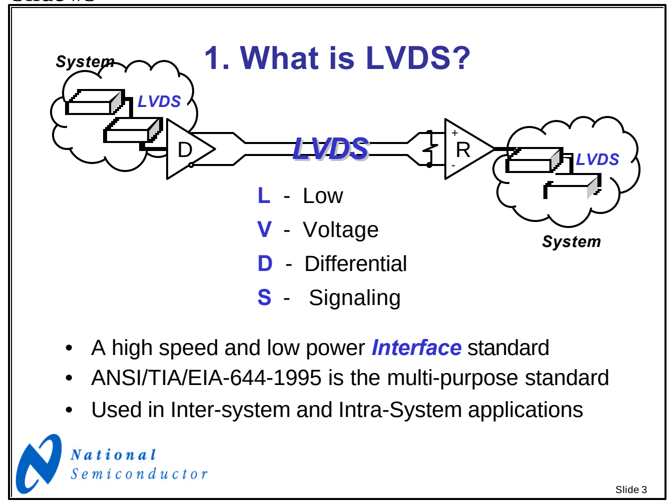


Due to the Internet's tremendous growth, data transfers are increasing dramatically in all areas of communications. In addition, data streams for digital video, HDTV, and color graphics are requiring higher and higher bandwidth. System designers, who need to transfer large amounts of data, have to rely on analog techniques for circuit design and data transmission. An analog technology that is meeting the mixed signal needs of these system designers is LVDS, or Low Voltage Differential Signals. LVDS uses high-speed analog circuit techniques to provide multi-gigabit data transfers on copper interconnects.

LVDS is now spawning follow-on technologies that expand the applications for the technology. The first follow-on is Bus LVDS, which allows the low voltage differential signals to work in bi-directional and multi-drop configurations. Another LVDS derivative Ground referenced LVDS, or GLVDS is progressing through the standardization process. GLVDS moves the differential signal's common mode voltage close to ground, which allows chips operating from very low supply voltages to communicate over a high-speed standard interface.

This presentation will cover six points listed in Slide #2. There is an introduction to LVDS and BusLVDS technologies. Also, a look at LVDS's system advantages and at how BLVDS extends the LVDS advantage to systems with bussed signals. Finally, a look at testing system applications issues for the LVDS technologies. Examples of tests for LVDS and BLVDS using the HP 81200 Data Generator and Analyzer equipment are given. Finally, the conclusion that describes LVDS benefits in system design.

Slide #3



Low Voltage Differential Signaling is a generic interface standard for high-speed data transmission. The ANSI/TIA/EIA-644-1995 standard specifies the physical layer as an electronic interface. This standard defines driver and receiver electrical characteristics only. It does not define protocol, interconnect, or connector details because these details are application specific. The LVDS Standard's Working Group chose to define only the electrical characteristics to ensure that LVDS becomes a multi-purpose interface standard. Therefore, each application that uses LVDS should also reference the appropriate protocol and interconnect standard.

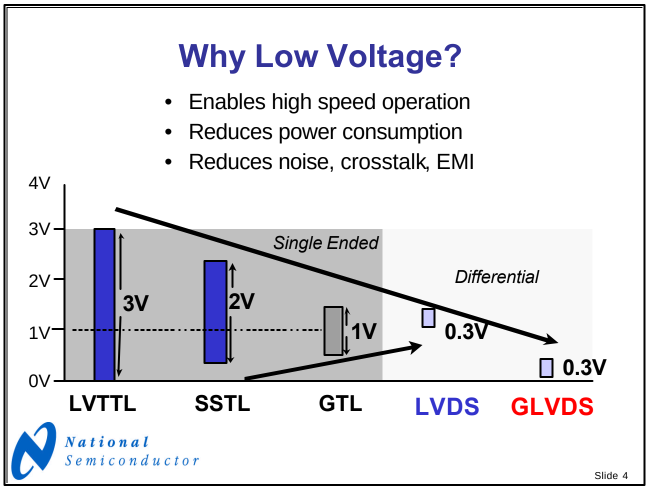
Wherever you need high-speed data transfer, such as 100 Mbps and higher, LVDS offers a solution. There are many applications in many market segments that use LVDS for data transmission. These include:

Stackable Hubs for datacom,
Wireless Base Stations and ATM Switches in Telecom,
Flat Panel Displays and Servers in the compute market,
Peripherals like Printers and Digital Copy Machines,
High Resolution Displays in Industrial applications,
and, Flat Panel Displays in the Automotive market.

In these applications, high-speed data moves within, and between systems. We refer to moving data within a system as <u>intra-system</u>. This is the main use for LVDS solutions today. Moving information between systems, or <u>inter-system</u>, requires standard communication protocols such as IEEE 1394, Fibre Channel, and Gigabit Ethernet. Since the hardware and software overhead for inter-system protocols is too expensive to use for intra-system data transfers, a simple and low cost LVDS link is an attractive alternative. Thus, LVDS solutions move information on a board, and between boards, modules, shelves, racks, or box-to-box. The transmission media can be copper cables, or printed circuit board (PCB) traces.

In the future, LVDS will also carry protocols for inter-system communication.

Slide #4



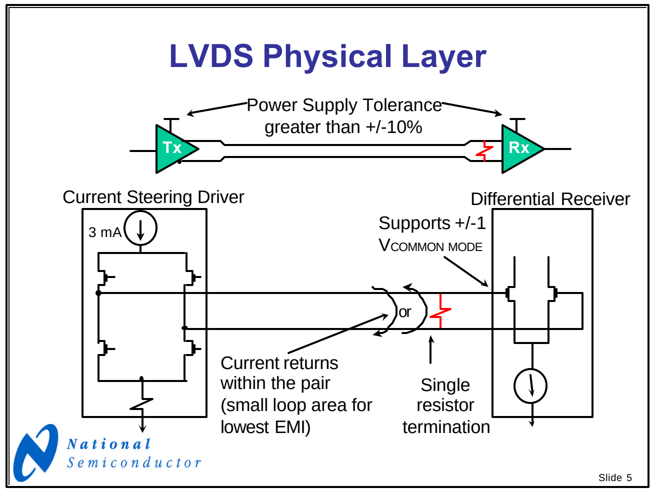
There are three good reasons for using low voltage signals. They are fast bit rates, lower power, and better noise performance.

Design engineers have previously used full swing CMOS and LVTTL Logic, but as bit rates increase, these solutions become unattractive. More recently, designers have turned to reduced swing technologies such as SSTL and GTL to gain speed, save power, and reduce noise. LVDS even further increases these advantages by lowering voltage swings to about 300 mV. However, you may think low voltage swings would reduce noise margins as well. But, to increase noise immunity and noise margins, LVDS uses differential data transmission. Differential signals are immune to common mode noise, which we will see is the primary source of system noise.

Because the voltage change is only 300 mV between logic states, it can change very fast. An additional advantage is the signal changes voltage levels without a fast slew rate. By slowing the transition rate, the radiated field strength decreases. Also, reflections from transmission path impedance discontinuities are less of a problem because of slower transitions. This decreases the emissions and crosstalk problems.

Low voltage swing reduces power consumption because it lowers the voltage across the termination resistors and lowers the overall power dissipation.

Slide #5



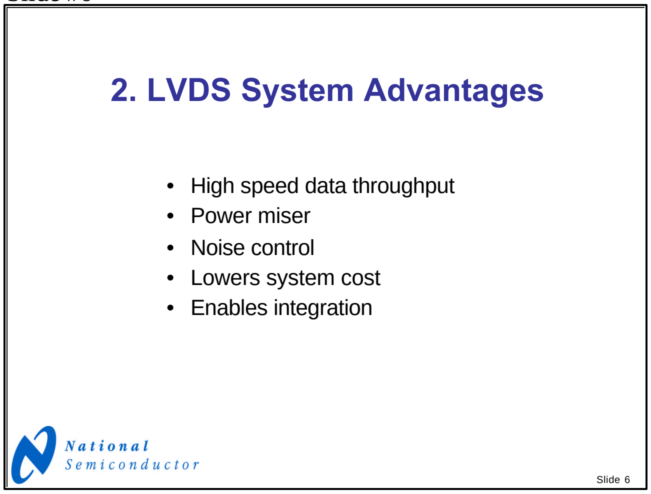
The LVDS physical layer equivalent circuit structure is shown in Slide #5. In the driver, a current source limits output to about 3 mA, and a switch box steers the current through the termination resistor. This differential driver produces odd-mode transmission, which means equal and opposite currents flowing in the transmission lines. The current returns within the wire pair, so the current loop area is small, and therefore, generates the lowest amount of EMI. The current source limits any spike current that could occur during transitions. Because there are no spike currents, data rates as high as 1.5 Gbps are possible without a substantial increase in power dissipation. In addition, the constant current driver output can tolerate transmission lines shorted together, or to ground, without creating thermal problems.

The differential receiver is a high impedance device that detects as little as 20 mV differential signals and then amplifies them into standard logic levels. The signal has a typical driver offset of 1.2V, and the receiver accepts an input range of Ground to 2.4V. This allows up to plus and minus 1V of common mode rejection from noise picked up along the interconnect.

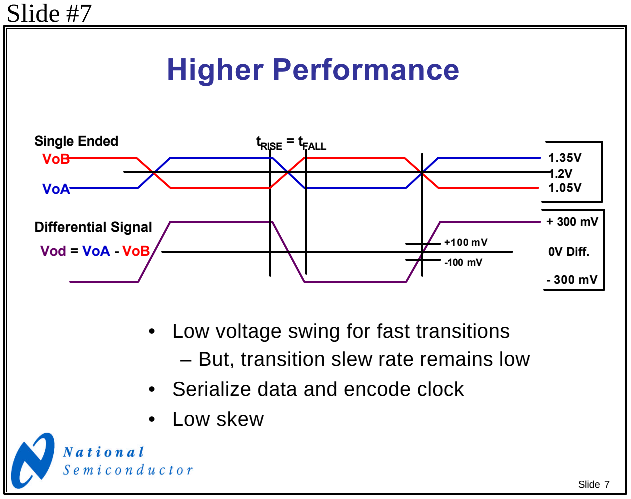
In addition, hot plugging of LVDS drivers and receivers is possible because the constant current drive eliminates damage potential. Another feature is the receiver's failsafe function to prevent output oscillations when the input pins are floating.

When choosing the signal level voltages for drivers and receivers, the standards committee considered LVDS implementation in technologies such as Bipolar, BiCMOS, CMOS, and even GaAs. In addition, the working group targeted a wide range of power supplies; for example 5V, 3.3V, and 2.5V, for implementing LVDS. This was done to ensure that LVDS would be the interface of choice for future generations of products.

Slide #6



Slide #7

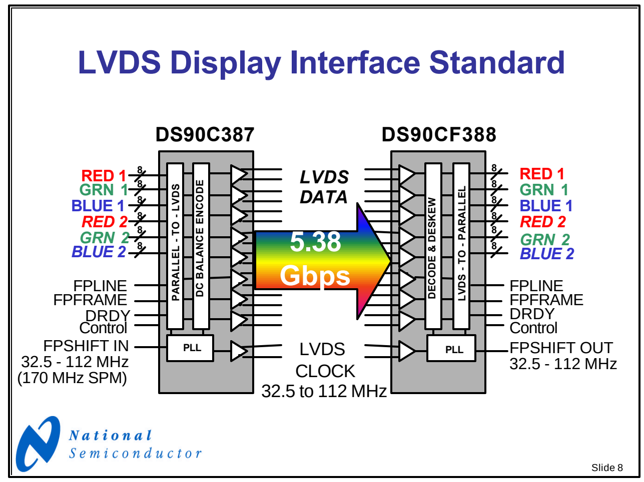


LVDS system benefits consist of high-speed data throughput, power miser operation, noise control, low cost, and higher integration. The simple phrase **"Gigabits at milliwatts!"** conveniently describes the LVDS system benefits.

The diagram in Slide #7 emphasizes the low swing voltage advantage for higher performance. For example, when the signal level changes 300 mV in 333 picoseconds, the slew rate is only 0.9 V/ns. That is less than the 1 V/ns benchmark slew rate that is commonly acceptable for minimizing signal distortion and crosstalk. Also, if you use the old benchmark that the rise and fall times should be no more than two thirds of the bit width, then signals with 333 picosecond transitions can operate as high as 1 Gbps with plenty of margin.

System features, such as serializing data, encoding the clock, and low skew, all work together for higher performance. Skew is a big problem for sending parallel data and its clock across cables or PCB traces. The problem is the phase relation of the data and clock can be lost due to different travel times through the link. However, with the ability to serialize parallel data into a high-speed signal with embedded clock, it eliminates the skew problem. The problem disappears because the clock travels with the data over the same differential pair of wires. The receiver uses clock and data recovery to extract the embedded clock, which is phase aligned to the data.

Slide #8

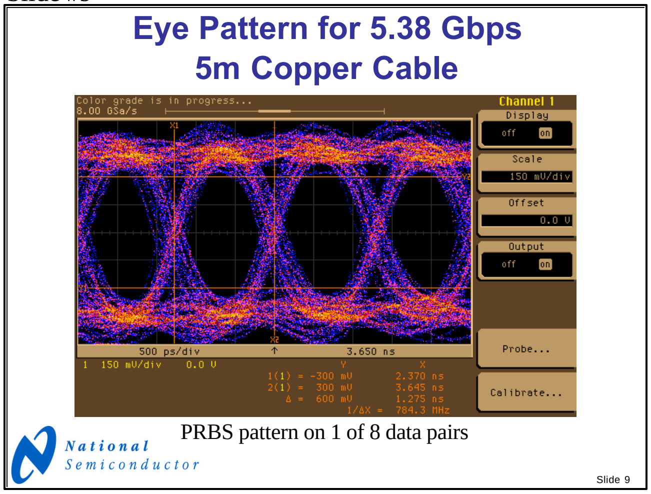


An example of LVDS's high performance is the OpenLDI (Open LVDS Display Interface) chipset that supports 24 bit color and provides over **5 Gbps** throughput. This throughput uses only 8 data pairs and a clock pair. The chipset serializes a 48-bit TTL interface down to the 8 pairs and then deserializes it at the receiver. The chip set supports TTL clock rates up to 112 MHz. To do this, each LVDS data channel serializes 6 TTL lines, plus a DC balance bit, into a single high speed LVDS pair. That pair operates at 784 Mbps with a data throughput of 672 Mbps. The OpenLDI chip set can also operate at TTL bit rates as low as 33 Mbps.

Along with the tremendous throughput, the chip set reduces the interconnect width and provides multiple system benefits. The cable is smaller, more flexible, and lower cost, and the connector has fewer pins, is smaller, and again, lowers cost.

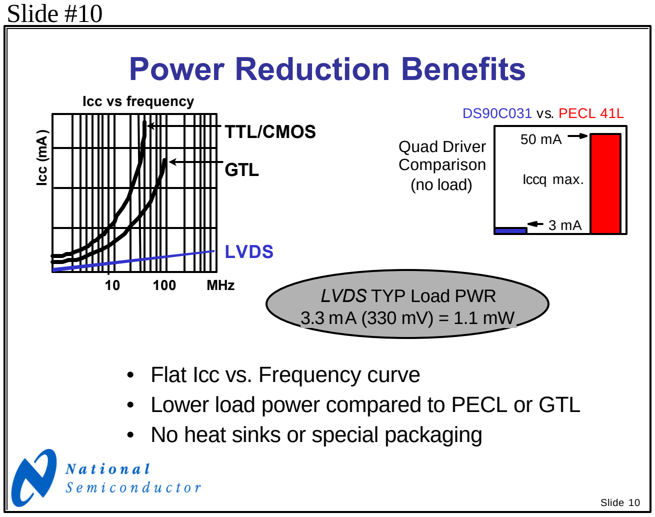
The chip set supports cable lengths up to 10 meters by integrating special functions. These functions are transmitter Pre-emphasis, DC Balance coding, and Cable Deskew. They all work to extend the reach and bandwidth of FPD-Link interconnects to flat panel monitor applications that may require longer cables.

Slide #9



The beautiful eye pattern in Slide #9 is taken at the end of a 5-meter cable between the Transmitter and Receiver of the OpenLDI chip set. The transmitter drives a Pseudo Random Bit Sequence through the cable and the receiver recovers the signal. The markers show the bit width to be 1.275 ns wide, which indicates a 784 Mbps data rate. Each of the 8 pairs carries this raw data rate for an aggregate bandwidth of almost 6.3 Gbps. This data rate includes overhead for DC balance, which makes the actual payload bandwidth 5.38 Gbps.

Slide #10



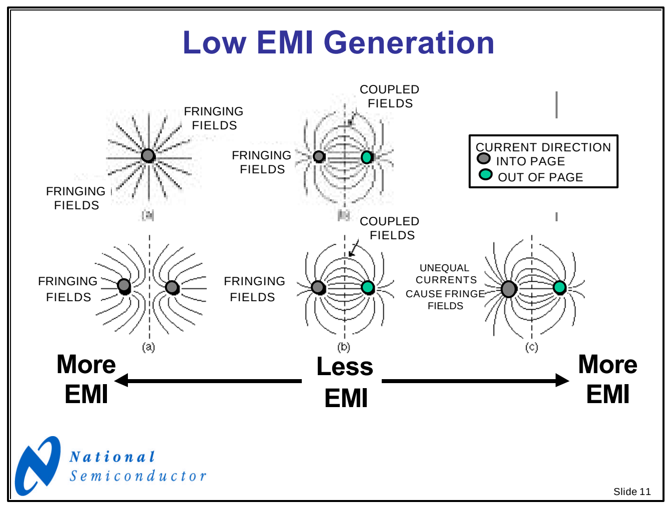
A significant advantage for LVDS technology is the power reduction benefit. The graph in Slide #10 shows LVDS's supply current remaining flat as the operating frequency increases. For comparison, the supply current for CMOS and GTL technology increases exponentially as frequency increases. Again, LVDS benefits because it is a constant current line driver rather than a voltage mode driver.

The load power calculation shows that 3.3 mA times the 330-mV drop across the 100 Ω termination resistor means LVDS has only 1.1 mW load power consumption. As a comparison, GTL consumes 40 mA of load current through a 1V drop across the load resistor, which is a whopping 40-mW load power dissipation.

The bars graph on the right shows the supply current reduction for LVDS compared to Pseudo ECL. The DS90C031 is a pin-compatible replacement part for the Pseudo ECL 41L Quad Differential Line Driver. The LVDS part consumes 16 times less supply current than the PECL part.

Furthermore, the low power consumption inherent in LVDS technology eliminates the need for either heat sinks or special packaging. This is an added benefit because it reduces the system cost of gigabit data transfers.

Slide #11

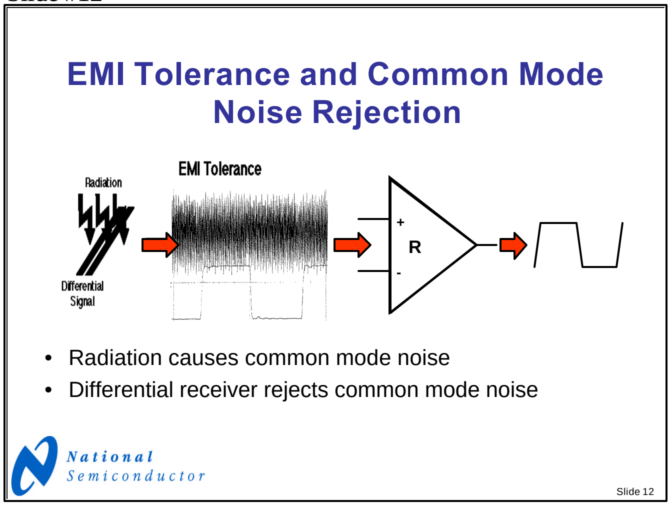


Another LVDS benefit is the low electromagnetic interference generation. The reasons LVDS generates low emissions are the low voltage swing, the slow edge rates, the odd mode differential signals, and the minimal I_{cc} spikes from constant current drivers.

High frequency signal transitions flowing through a transmission path create electromagnetic fields that radiate emissions. The field's strength is proportional to the energy carried by the signal. By reducing the voltage swing and the current energy, LVDS minimizes these fields. However, even the reduced electromagnetic fields can cause radiation problems.

Differential signal paths reduce the harmful effects of these fields to further minimize these radiation problems. Balanced differential lines have equal but opposite currents, which we call odd mode signals. When the fields created by these odd mode signals are closely coupled, they tend to tie each other up and thus can not escape to cause harm. For this reason, it is important to maintain a balanced and closely coupled differential transmission path. The net effect will be the reduced emission of electromagnetic interference.

Slide #12

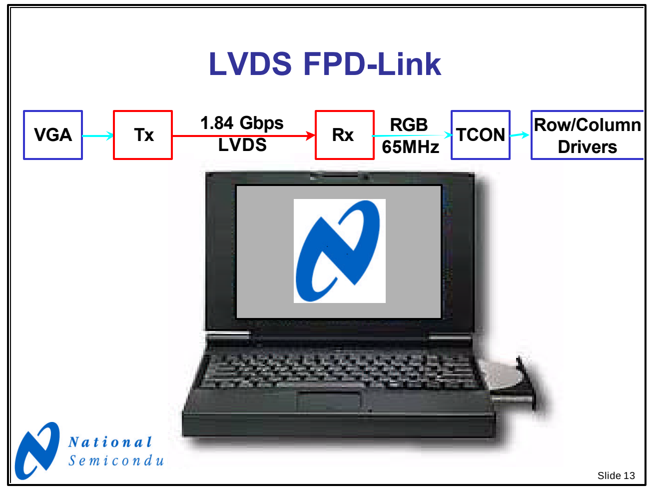


Differential signals also have the benefit of tolerating interference from outside sources. Good examples are the problems caused by inductive radiation from electric motors or crosstalk from a neighboring transmission line. When the differential transmission lines are closely coupled, the induced signal will be common mode noise. That means that the noise will appear as a common mode voltage at the receiver input.

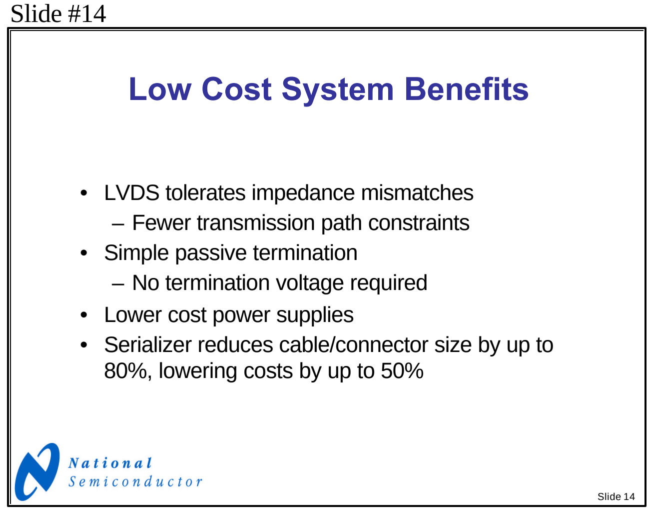
The differential receiver responds only to the difference between the plus and the minus inputs so when the noise appears commonly to both of the inputs, the input differential signal amplitude is undisturbed. This common mode noise rejection also applies to such noise sources as power supply variations, substrate noise, and ground bounce.

The LVDS Flat Panel Display Link standard shown in Slide #13 demonstrates the low noise generation characteristics for LVDS while targeting LCD applications for Notebooks and Sub-Notebooks. The FPD link moves large amounts of display data from the notebook PC to the display panel. The system designers had to solve the problem of twisted pair cables or flex circuit carrying high-speed data through the panel hinge without creating EMI problems. They chose to use the LVDS technology because it has better EMI performance than all the other interface technologies.

Slide #13



Slide #14

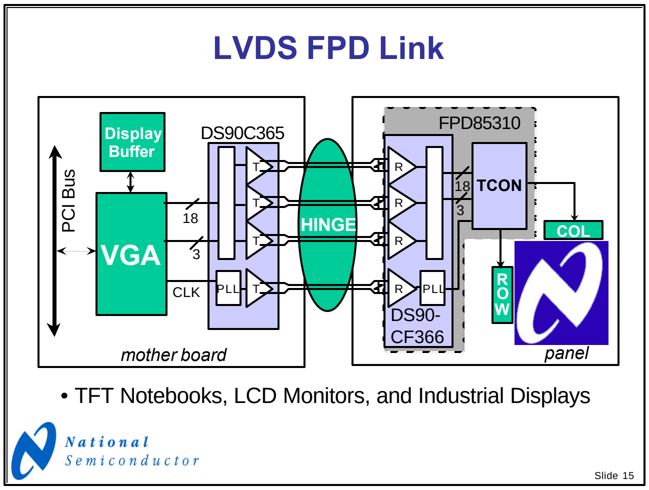


All of the benefits discussed so far affect the system cost savings. There are even more system cost savings from using LVDS. The first is LVDS's ability to tolerate minor impedance mismatches in transmission paths. As long as the differential signal passes through balanced discontinuities in closely coupled transmission paths, the signal can maintain integrity. The effect of non impedance-controlled connectors, printed circuit board vias, and chip packaging is not as detrimental to differential signals as it is to single ended signals. In addition, it is possible to use less circuit board layers because of the relative immunity to crosstalk that is inherent in differential signals.

LVDS requires only a simple termination resistor, and it is possible to integrate this resistor onto the chip. This is much lower cost than using multiple resistor and capacitor components for each transmission line. In addition, LVDS requires no termination or Vddq voltage supply. This is a big cost advantage over technologies such as GTL, LVTTL, and SSTL.

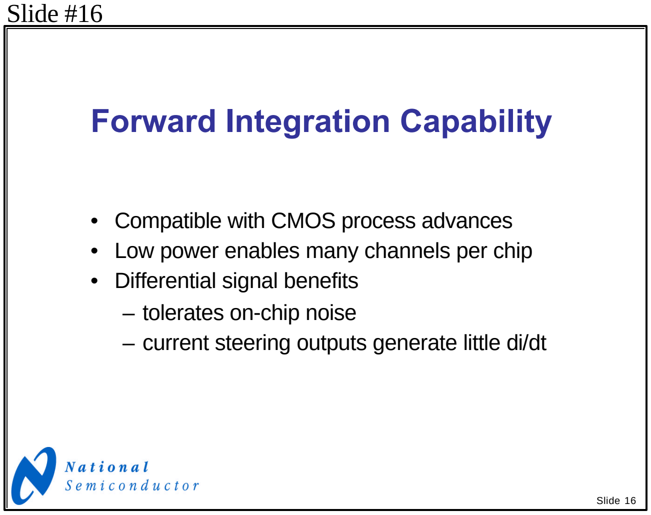
Because LVDS is capable of handling the high-speed data that results from serializing many parallel bits into a single data stream, LVDS chips commonly integrate serializers and deserializers. This saves about 50% of the cost due to cabling, connector, and PCB when compared to a parallel interconnect.

Slide #15



The FPD-Link chipset also demonstrates the system cost savings from using LVDS. The chipset takes the 18- or 24-bit wide RGB (Red/Green/Blue) bus and the VSYNC, HSYNC, and Data Enable control lines and multiplexes them down to only 4 or 5 pairs. This low-cost 4 or 5 pair link passes data through the hinge to the panel where it is de-multiplexed. Typical interconnects range from about 8 cm to 40 cm in length and use low cost flex circuit or twisted pair cabling.

Slide #16



The last LVDS system benefit to discuss is the integration capability. Because it is possible to implement high speed LVDS in a standard CMOS process, integrating complex digital functions with LVDS's analog circuits is a huge advantage. Integrating serializers and deserializers is only the beginning to mixed signal LVDS chips.

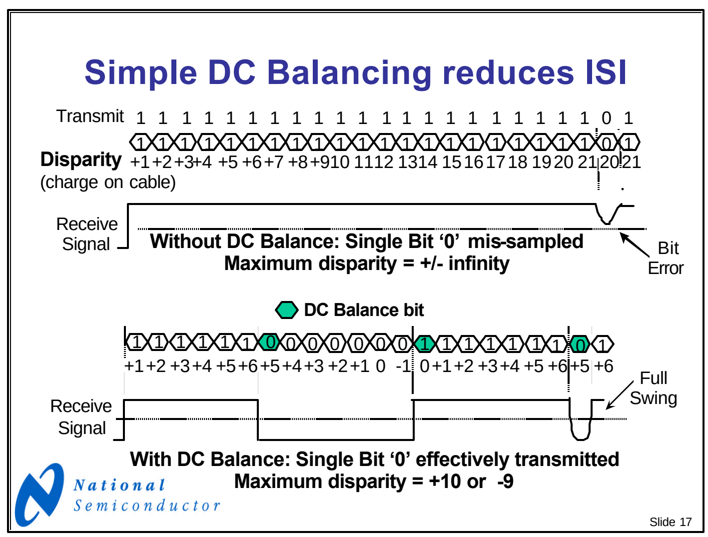
LVDS's low power consumption enables integrating many channels per chip. For example, it is possible to serialize a 128-bit, on-chip parallel bus down to 8 differential channels. This narrower link dramatically reduces pin count and total link cost.

Integration also benefits from differential signals. Their ability to tolerate high levels of switching noise increases their reliability when integrated with large-scale digital circuits. In addition, LVDS generates very little noise due to the constant current nature of the output structures.

Therefore, complete Interface Systems-on-a-Chip are feasible. Digital blocks for integration include DC Balance circuits, Clock Embedding, Clock Recovery, Encoders and Decoders, and De-skew blocks. Higher level digital functions such as hardware protocol assist, management and statistics counters, and routing decision logic are also using LVDS on-chip as the interface of choice.

Further integration of the blocks shown in the FPD-Link chipset (see Slide #13) is already happening. The obvious integration path is the LVDS transmitter with the VGA controller and the LVDS receiver with the timing controller.

Slide #17



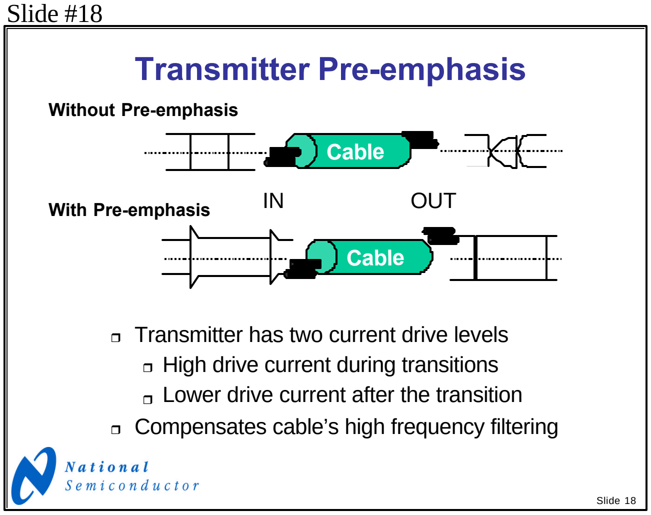
Slide #17 shows a simple DC balancing scheme on the OpenLDI chipset that reduces inter-symbol interference. It demonstrates integrating digital functions onto the same chip as the LVDS interface.

Without DC Balance, a long cable can result in ISI for a single bit transition and cause a bit error. This happens because a single bit transition, after a long string of no transitions, may not contain the energy necessary to change the stored charge through the entire cable. The term "disparity" describes the stored charge on the cable. If the disparity magnitude is large, then the single bit transition can not overcome the inter-symbol interference at the end of the cable.

The OpenLDI part provides DC balance on a frame by frame basis. During the frame, the transmitter monitors the input signal for transitions. If no transitions occur, the transmitter inverts the next frame to maintain balanced cable charge, and thus, keeping the disparity between plus 10 and minus 9. The 7th LVDS data bit indicates whether the data in the payload is "true" or "inverted".

This simple DC balance scheme keeps the signal eye diagram wide open at the receiver end. In addition, this scheme provides enough DC balance to satisfy fiber optical interconnect requirements, allowing this chip set to interface with standard parallel optical fiber products.

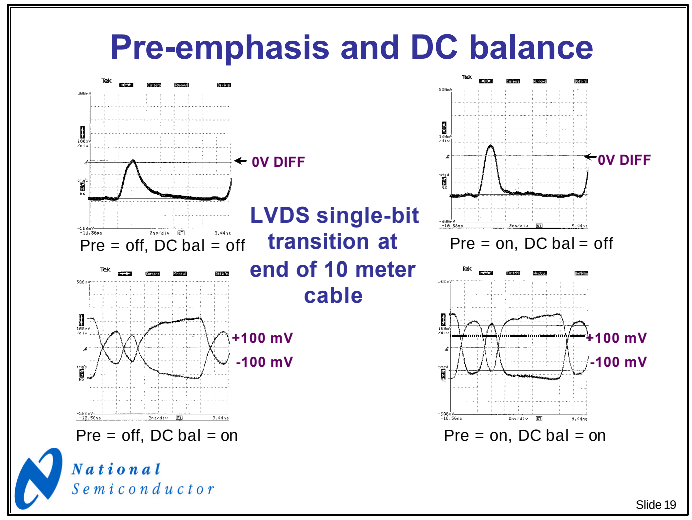
Slide #18



Another integrated enhancement to the OpenLDI chip set is the transmitter pre-emphasis feature. Without pre-emphasis, the signal coming out of a cable has lost the sharp transition edges due to the cable's high frequency filter effect. With pre-emphasis, the driver accentuates the transitions to compensate for the filter effect at the end of the cable.

The Pre-emphasis feature is user selectable. When selected, the transmitter has two current drive levels. It delivers additional dynamic current during transitions to overcome the cable's filtering. Then, the transmitter supplies a lower drive current after the transition. It works to open the signal eye diagram by overcoming cable distortion of the signal.

Slide #19

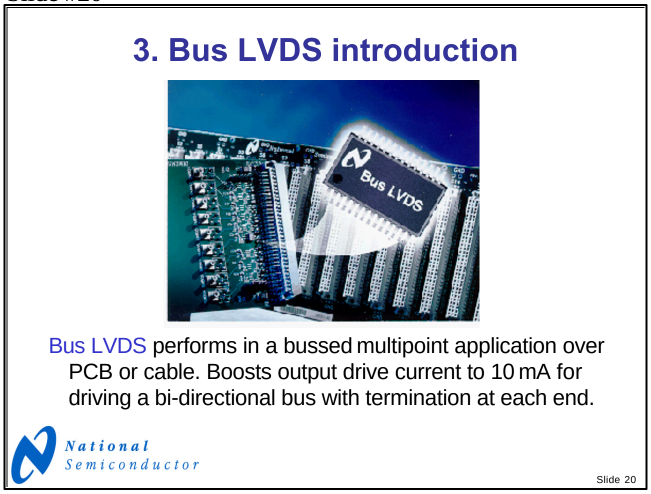


In Slide #19, we see actual scope plots demonstrating pre-emphasis and DC balance. The scope plots show the differential waveform of a single-bit transition at the end of a 10-meter cable. The bottom two scope plots use the persistence mode and show the single bit transition with DC balance turned-on.

The upper right hand plot shows the single-bit transition without the aid of pre-emphasis or DC balancing. We can see that the bit barely crosses the 0-Volt differential level. The upper left diagram shows that by turning on the pre-emphasis, the bit does pass the 0 Volt differential level but with very little noise margin. Notice, also, how both edges of the bit are sharper with the pre-emphasis feature on.

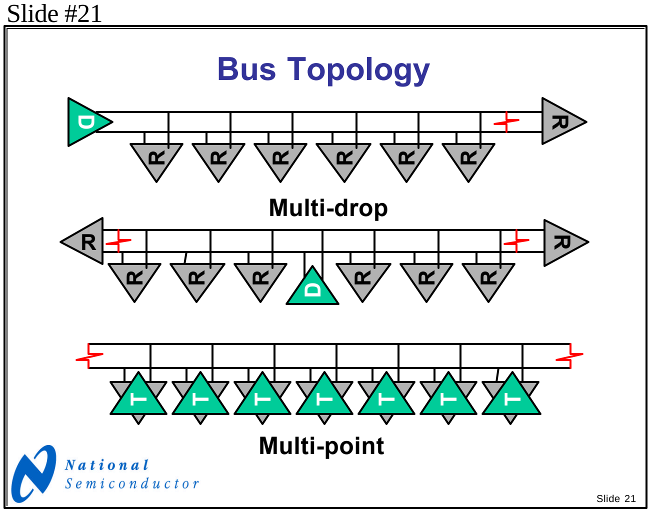
The lower two plots show the differential signal in persistence mode. This mode shows the single bit transition and the DC balance bit being either high or low because the balance scheme inverts the bit in alternate words. The lower right diagram shows that using only the DC balance feature does allow for clean bit transitions that exceed 100 mV. The lower left diagram shows that when both pre-emphasis and DC balance are on, the single bit transitions are sharp and provide plenty of noise margin, and this is after traveling down a 10 meter cable.

Slide #20



Bus LVDS uses LVDS in bussed multi-drop and multi-point applications over printed circuit board or cables. Bus LVDS uses the same basic schematic as shown for LVDS in Slide 3. The difference is that BLVDS boosts output drive current to 10 mA to drive a bi-directional bus that is terminated on each end.

Slide #21



A review of bus topology helps before discussing Bus LVDS.

The top two buses in Slide #21 show multi-drop configurations. The top configuration is uni-directional because there is a single driver at one end of the bus. This simple multi-drop bus requires only a single termination that is on opposite end of the bus from the driver, to stop reflections of the driven signal.

Each of the attached receivers reduces the loaded bus impedance. The loading amount depends on the connector, vias, packaging, and receiver input capacitance. With good design of these factors to keep the loading small, plain LVDS can drive this configuration.

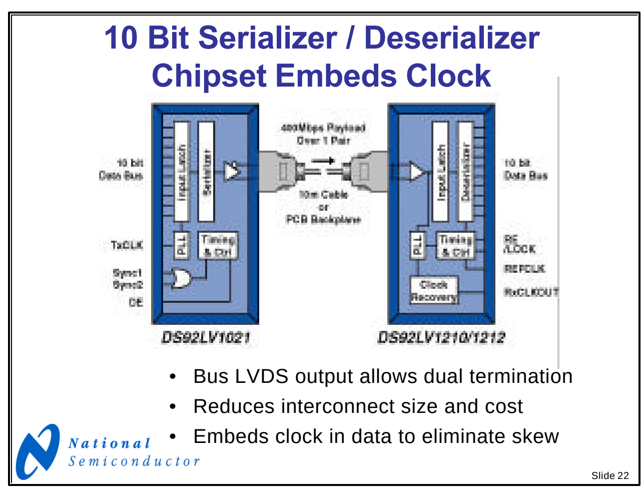
The most important factor for high-speed performance in all bus topologies is keeping each receiver's non-terminated stub very short, which minimizes reflections from that stub.

The second multi-drop bus differs from the first because it is driven from the center rather than the end of the bus. This configuration is useful for reducing flight time from the driver to all receivers. However, it requires a termination resistor at each end of the bus to prevent reflections. The two termination resistors are seen in parallel by the driver, so the driver must source twice as much current to drive this bus to the same differential voltage level as in the simple multi-drop bus example.

The third bus is a multi-point, bi-directional bus because there are multiple drivers and receivers, or transceivers, on this bus. This is the most difficult bus to design for high performance because of the variable driver positions, which cause various reflections that depend on where the signal originates in the bus. It, also, must be terminated on both ends to prevent reflections.

Signal integrity in a heavily loaded backplane is a very complicated problem due to the many impedance discontinuities that are inherent to the backplane environment. The worse case situation in bus signaling occurs when a card in the middle of the bus drives a signal into the backplane and the card in the adjacent slot looks to receive the signal. The edge rate from the driving card is very fast as it leaves the driving card and travels down the backplane. This means the adjacent cards see the fast edge propagate into the signal stub. This fast edge rate causes reflections on the stub that can glitch through the receiver threshold region.

Slide #22



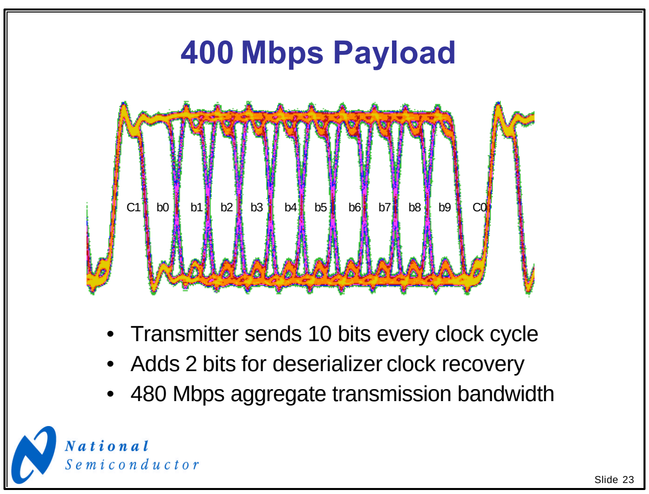
Bus LVDS extends LVDS's point-to-point and simple multi-drop applications to true multi-point busing functionality. It does this by boosting the drive current to 10 mA to drive double terminations, and providing driver output impedance that matches the line impedance to reduce reflections from driver outputs

An example of where to apply Bus LVDS technology is the Serializer and Deserializer chip set shown in Slide #22. The transmitter serializes a 10 bit parallel LVTTL interface into a single Bus LVDS data channel. The transmitter also embeds the clock in the serial stream. The Bus LVDS Receiver recovers the clock and data to deserialize back into the 10 bit parallel interface.

This chipset distributes data over a serial channel in multi-drop distribution systems. One serializer can drive many deserializers in either of the multidrop configurations shown in the previous slide. Multi-point application is also possible with certain limitations due to PLL lock time. The limitations arise when a new driver begins to drive the bus and all the receivers must lock to that driver's clock signal. In addition, the chip set also works in point-to-point applications

The chip set supports TTL clock rates from 16 to 80 MHz. For example, the chip set transfers an 800 Mbps payload over a 10-meter cable when the 10-bit interface operates with an 80 MHz clock.

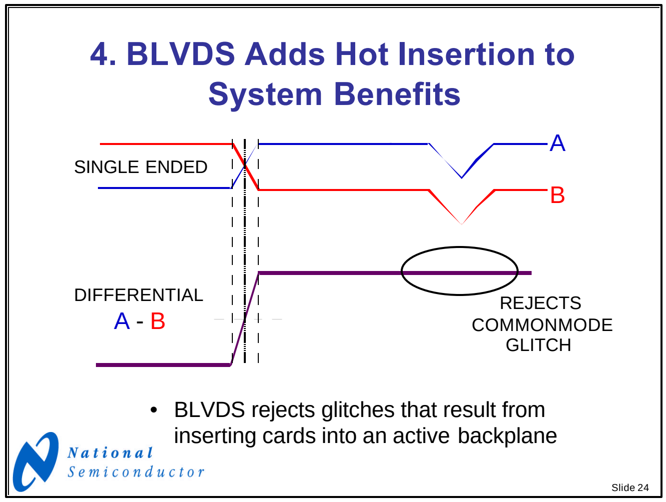
Slide #23



The waveform in Slide #23 illustrates the chipset's 10-bit payload surrounded by two embedded clock bits.

The actual serial bit rate with a 40 MHz clock is 480 Mbps, but the throughput is 400 Mbps. The receiver uses the embedded clock edges to lock onto the inbound serial stream and to align the data at the parallel output. It provides greater system benefits than other LVDS parts by eliminating the cost of a cable or PCB differential pair for the clock signal.

Slide #24



Bus LVDS carries the LVDS advantages to systems that require multidrop bus communications. One of the essential features required in multidrop busses is the ability to insert cards into the bus without powering down the bus. The most optimal hot insertion capability is to insert cards without stopping or disturbing the data traffic on the bus.

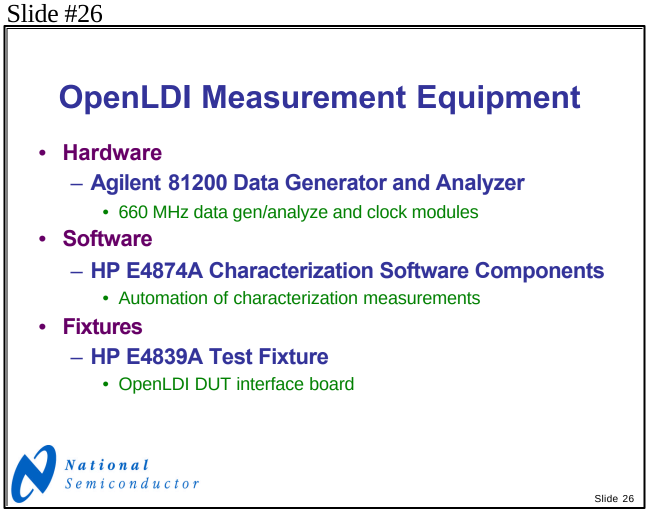
Bus LVDS supports the optimal hot insertion capability. It does this because the signal glitch caused by inserting the capacitive load of the plug-in card occurs equally on each of the differential lines. This results in no change to the differential signal as shown in Slide #24.

Slide #25

Testing LVDS System Design Issues

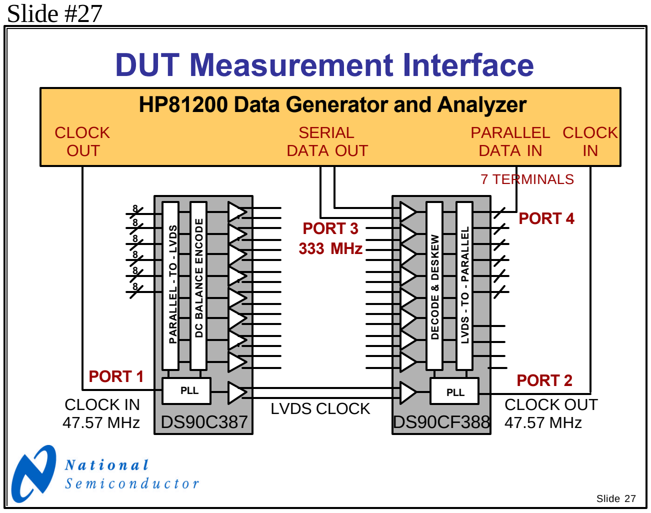
Now we can look at performance issues with high-speed LVDS chips. There are many considerations with testing these high performance devices. For example, the test equipment needs the two clock rates that result from serializing the parallel data into high-speed signals. The test system must be able to generate and analyze the data at both clock frequencies. Testing the Open LDI receiver is an example that can demonstrate some performance issues.

Slide #26



The Agilent 81200 Data Generator and Analyzer is a complete test system capable of 1.32 Gbps testing. The Generator and Analyzer achieves the 1.32 Gbps by multiplexing two of the 660 Mbps channels into one generator or analyzer channel. The test fixture uses an Open LDI chip set DUT board. The Characterization Software Components (CSC) takes the raw test data and places it in easy to understand visual format. Some examples of the CSC will show how LVDS responds to system situations.

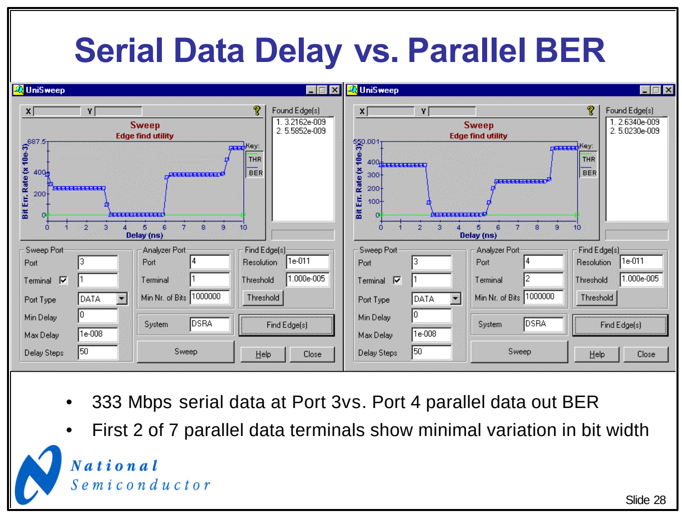
Slide #27



The Agilent 81200 test system uses ports to identify groups of generator and analyzer signals. In the Open LDI deserializer test example, there are 2 generator ports and 2 analyzer ports. The generator ports, Port 1 and Port 3, supply the two frequencies required for testing the LVDS deserializer. The analyzer ports, Port 2 and Port 4, sample the data.

The set-up block diagram shown in Slide #27 is for the Open LDI DUT interface board that is in the foreground of the test fixture shown in Slide #25. For the first set of tests, the Agilent 81200 generates the high frequency serial data at 333 MHz, which corresponds to 333 Mbps NRZ data generation. The generator also provides the serializer's input clock at 1/7 the serial data rate. The serializer then generates the LVDS clock input to the deserializer. The analyzer monitors the clock out from the deserializer and samples the data off the 7 parallel data terminals.

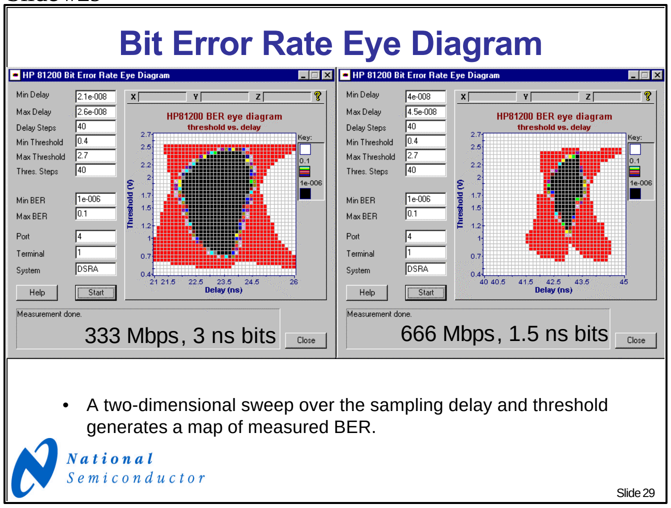
Slide #28



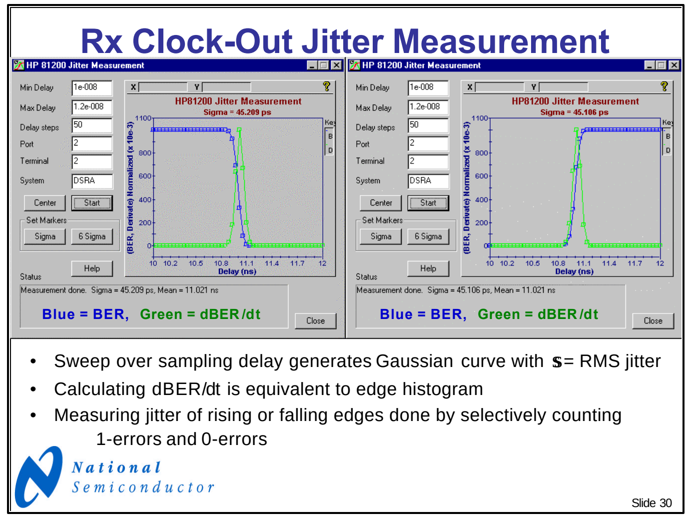
The first analysis that uses the visual display capability of the CSC shows the actual recoverable bit width of the serial data. By sweeping the serial data delay and checking the BER at the parallel Port 4, we can actually see the data bit width.

Slide #28 shows the delay vs. BER for the first two of the seven parallel bits. The bit width at 333 Mbps is nominally 3 ns, but as the BER graph shows, the recoverable bit is about 2.4 ns wide. On each side of the valid data window, the BER increases to a non-0 value. The BER is a constant value for each of the serial bits on both sides of the bit being checked for correctness. The values are constant but not at 1 because of the repetitive bit pattern used in this test. If the repetitive bit pattern had been a PRBS pattern, then the bit error rate for each of the other bits would be 0.5, which means there is equal, and random, chance that the bit would be either a 1 or a 0.

Slide #29



Slide #30



The next analysis tool is the BER Eye Diagram. The CSC generates this diagram by sweeping the sampling delay and the threshold of the analyzer on Port 4. The graph displays the BER as a color at each sampling point. The result is an eye pattern with the black colored center as the correctly sampled data. Other colors show the increasing errors as the sample point moves further away from the window.

This eye pattern differs from the oscilloscope eye diagram shown in Slide #9 because it does not simultaneously show multiple transitions. The Slide #9 eye diagram displays signal integrity information such as overshoot, undershoot, and edge jitter. Instead, the BER eye diagram demonstrates the valid data window for the recovered bits, which ultimately depends on receiver sampling performance in addition to the signal integrity.

Slide #29 visually emphasizes the useable portion of the serial bit width that was also shown in Slide #28. The BER eye width for Port 4, terminal 1 at 333 Mbps shows the same 2.4 ns bit width as in the serial port delay vs. BER graph.

The BER eye diagram for the 666 Mbps serial data shows how the bit width reduces as the signaling frequency increases. The graph on the right shows that although the nominal bit width at 666 Mbps is 1.5 ns, the valid data window delivered by the receiver and deserializer is really about 1.1 ns wide.

This BER eye diagram is useful in characterizing the receiver performance. It allows for examining the individual eye diagram for each bit. At the highest performance level, these eye diagrams must show limited variation between bits to assure there is maximum margin for board and cable skew. This characterization aids system designers to achieve data transfers that will be reliable.

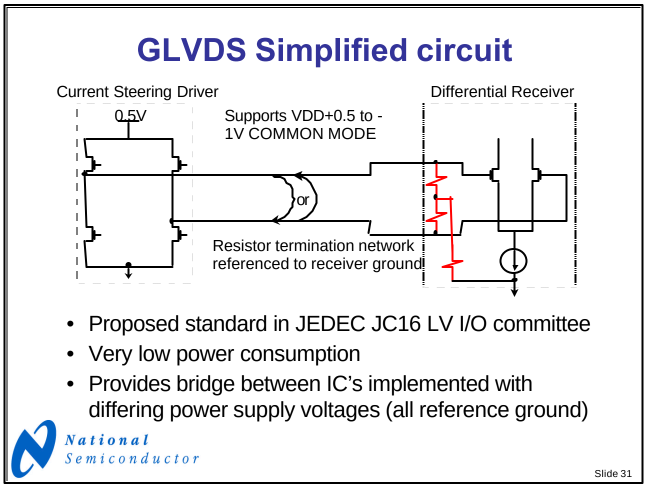
We can also examine the Deserializer's recovered clock-out jitter with the CSC. In this case, the HP81200 generates a histogram using the BER measurement. It performs these histogram measurements on a running device to obtain accurate jitter measurements.

The CSC uses the deviation of the BER (dBER/dt) to calculate the jitter. It measures the signal transitions by selectively looking at the pass-to-fail and the fail-to-pass BER transitions.

Slide #30 shows the jitter on both the rising edge and the falling edge for the Deserializer recovered clock-out signal. Because the sampling point for the analyzer is set at the same point for both the high and low transitions, 1.4V in this case, we can see that the jitter is symmetrical on the transitions. By setting the sampling point at different thresholds for the rising transition (2V) and falling transition (0.8V), it is possible to see different mean transition times for each of the edges.

The CSC also provides calculations for sigma and 6-sigma analysis of the histogram. The Sigma button displays a measurement that corresponds to the RMS jitter, while the 6-Sigma button would display a measurement that corresponds to a peak-to-peak jitter measurement. In Slide #30, the CSC reports that RMS jitter is about 45.2 ps for both the rising and falling edges of the deserializer clock-out.

Slide #31



The last topic to cover in this paper is a few words about GLVDS, which is not yet a standard interface. The JEDEC JC-16 committee for low voltage interface standards is currently considering the standard. The committee is analyzing the details for a standard that has transmitter output voltages between 0V and 0.5V and receiver input sensitivity of at least 100 mV. The very low transmitter output voltage provides for low power consumption by the interface. This lower power consumption is an advantage this technology brings to the LVDS family of standards.

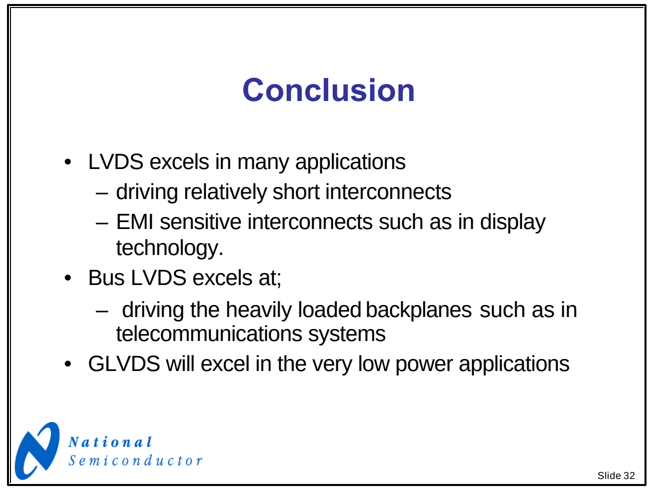
Another very important feature of this technology is the ability for chips with far different power supplies—from 5V down to 0.5V—to still communicate with each other. This is possible because all of these power supplies use ground as a common reference. That common ground is the common voltage levels where GLVDS signals are working.

The simplified GLVDS schematic shown in Slide #31 is very similar to both LVDS and BLVDS. One of the few differences is the circuit from the middle of the receiver termination to the receiver's ground. The GLVDS name refers to this ground reference for the receiver termination. GLVDS requires termination to be on-chip rather than an off-chip option, which is the case with LVDS and BLVDS.

The GLVDS standard does not specify any transmitter drive current. The intention is to leave that open to the individual applications that will use the interface technology. This would allow the driver to provide a small current—for example, 1.5 mA to 3 mA—for chip-to-chip applications that have short interconnects. In other cases, large driver current output—8 mA to 15 mA—for applications that need to drive long cable lengths.

In conclusion, Low Voltage Differential Signaling will continue to evolve toward more and more system applications. The

Slide #32



applications for LVDS technologies do overlap in some instances, but they also have applications in which each excels. For plain old standard LVDS, it excels in applications having to do with driving relatively short interconnects. In addition, it excels where EMI is a critically sensitive issue for the interconnect, such as in display technology.

Bus LVDS excels at driving heavily loaded backplanes such as those used in telecommunications systems. It also works well in distributing signals from a single driver to multiple receivers. Bus LVDS also finds applications in driving bussed cable interconnects of a few meters in length.

GLVDS will excel in the very low power applications such as remote base stations where power may be locally supplied and generated by wind or sun. Also as a chip-to-chip interconnect for very short distances. The main function for GLVDS might be the interconnect technology for chips that have power supplies of 1V and less.