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High-Power Density Switching Regulators LM2830/31/32 2

Dual High-Power Density Switching Regulator LM26400Y 4

Calculating Losses and Junction Temperature for High-Power-Density Switching Converters

— By Matthew Reynolds, Principal Applications Engineer

Introduction

Today's silicon fabrication technology has allowed power conversion ICs to increase power density by an order of magnitude from the technology that existed just five years ago. Smaller geometries and other power-process improvements have enabled National Semiconductor to create more efficient devices. Increases in efficiency are realized by new intellectual property including lower R_{DS-ON} and lower capacitive devices. Further, smaller silicon geometries decrease the size of the logic circuits, allowing for a greater amount of space for the main power-pass elements.

In the last five years, National Semiconductor has leveraged new process technologies and created a family of buck, boost, and buck-boost converters, as well as Single-Ended Primary Inductor Converters (SEPICs) in small packages that are industry leaders in power density. Examples of devices available today are the LM2734Z, LM2830/31/32 buck converters, and the LM2735 boost and SEPIC converter. The LM2734Z has an input voltage range of 3V to 20V and a switching frequency of 3 MHz. The LM2830/31/32 buck converters hold a leadership position in power density as does the LM2735 converter. This article will provide an overview of these devices as well as application circuits and tips that are helpful in using high-density DC-DC monolithic converters.

To explain how fabrication process developments increase efficiency, one must first understand power losses in a monolithic DC-DC converter. Losses can be categorized into two types: conduction losses and switching losses. Conduction losses are the easiest to understand, and these will be addressed first.

Conduction Losses

All silicon devices have resistance associated with them. Conduction of current through resistances in the IC and package results in I_{RMS}^2 x R power losses.

To illustrate the losses within a DC-DC converter, it is useful to consider the buck converter. The buck converter is the most common DC-DC converter today. This topology produces an output voltage lower in magnitude than the input voltage.

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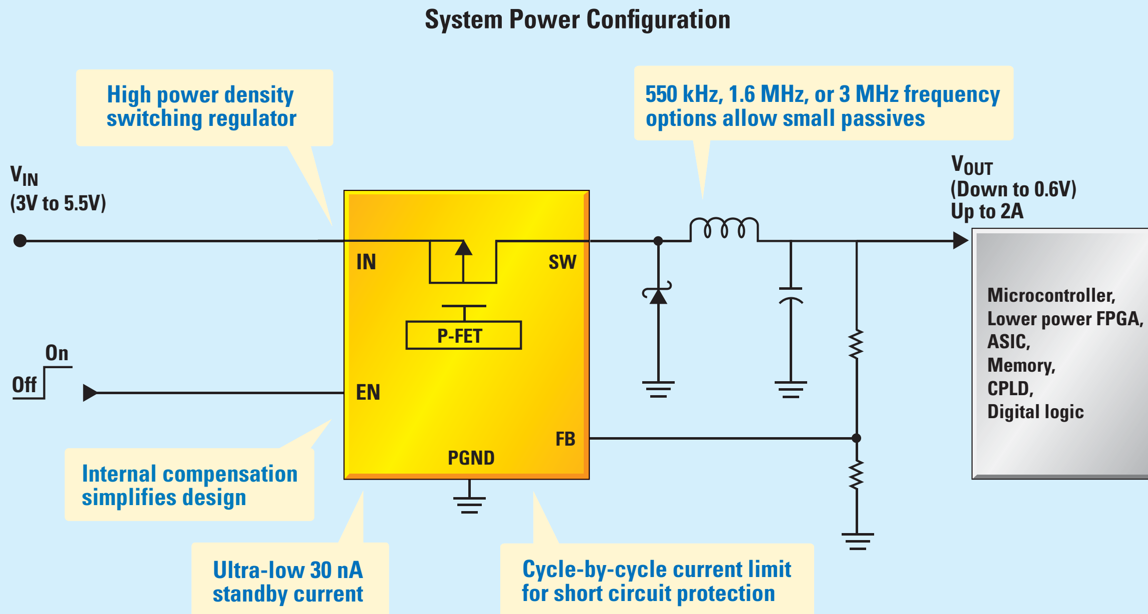

Product ID	I_{OUT}	Packaging
LM2830	1A	SOT23-5, LLP-6
LM2831	1.5A	SOT23-5, LLP-6
LM2832	2A	eMSOP-8, LLP-6

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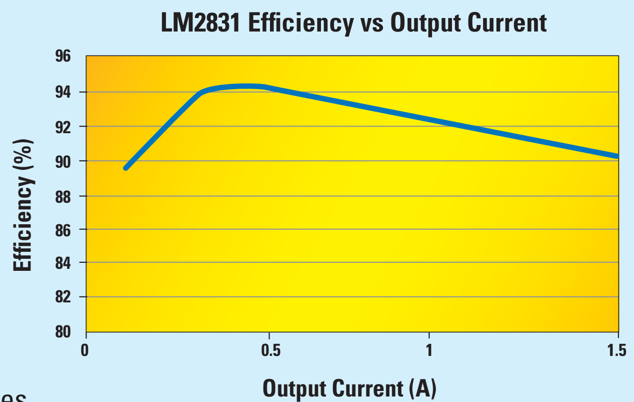

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Calculating Losses and Junction Temperature for High-Power-Density Switching Converters

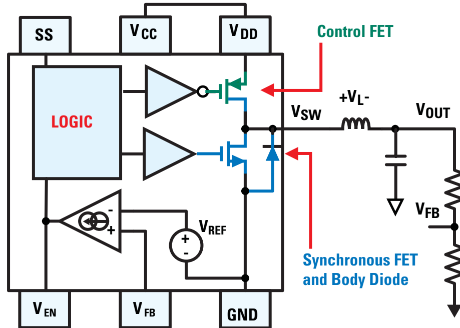

Figure 1. Simplified Buck Converter Schematic

A simplified diagram of a synchronous converter and its associated waveforms are shown in ***Figure 1*** and ***Figure 2***.

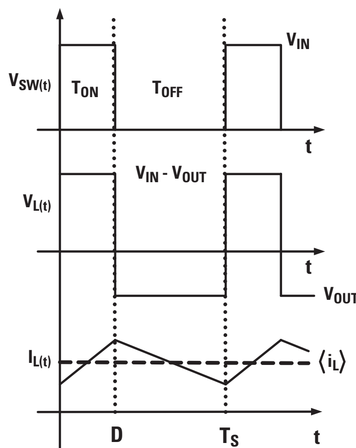

Figure 2. Simplified Buck Converter Waveforms

Figure 3 is an illustration of the typical switch-node voltage and inductor-current waveform. These waveforms explain the losses in one switching cycle.

The conduction losses for one full switching cycle are illustrated in Area 1 and Area 2. During the DT_S part of a switching cycle, the control FET is on, and conduction losses in Area 1 are calculated. $R_{DSON\text{-}CTRL}$ can be empirically calculated by knowing the load current and the voltage difference between V_{IN} and the switch node.

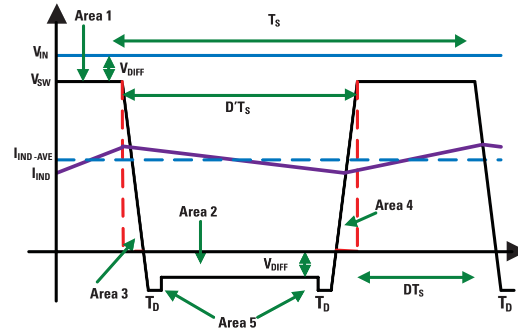

Figure 3. Losses within a Buck Converter

D = Duty Cycle

D' = (1 - D)

F_{SW} = Switching Frequency

The power loss during the DT_S interval is:

$$P_{CTRL} = I_{RMS} \times V_{DIFF} \times D$$

or

$$P_{CTRL} = I_{RMS}^2 \times R_{DSON-CTRL} \times D$$

where I_{RMS} is the output-load current in a buck converter.

During the $D'T_S$ period, the bottom synchronous FET is on. $R_{DSON\text{-}SYNC}$ can be empirically calculated knowing the load current and the voltage difference between GND and the switch node.

The power loss during the $D'T_S$ interval is:

$$P_{SYNC} = I_{RMS} \times V_{DIFF} \times D'$$

or

$$P_{SYNC} = I_{RMS}^2 \times R_{DSON-SYNC} \times D'$$

Switching Losses

Switching losses are a bit more difficult to calculate, but with good bench practices very accurate results can be obtained.

Switching losses occur during the transition from one MOSFET being turned on while the other MOSFET is being turned off. ***Figure 3*** illustrates that this transition occurs twice in one switching cycle (Area 3 and Area 4). The inductor current is continuous; therefore there will always be a path for this current even if both MOSFETs are off. The synchronous MOSFET body diode conducts the current during the dead time when both MOSFETs are off. A typical switching cycle is as follows: Start with the control MOSFET on, and the synchronous MOSFET off. At time DT_S, the converter's loop signals the control MOSFET to turn off. Both

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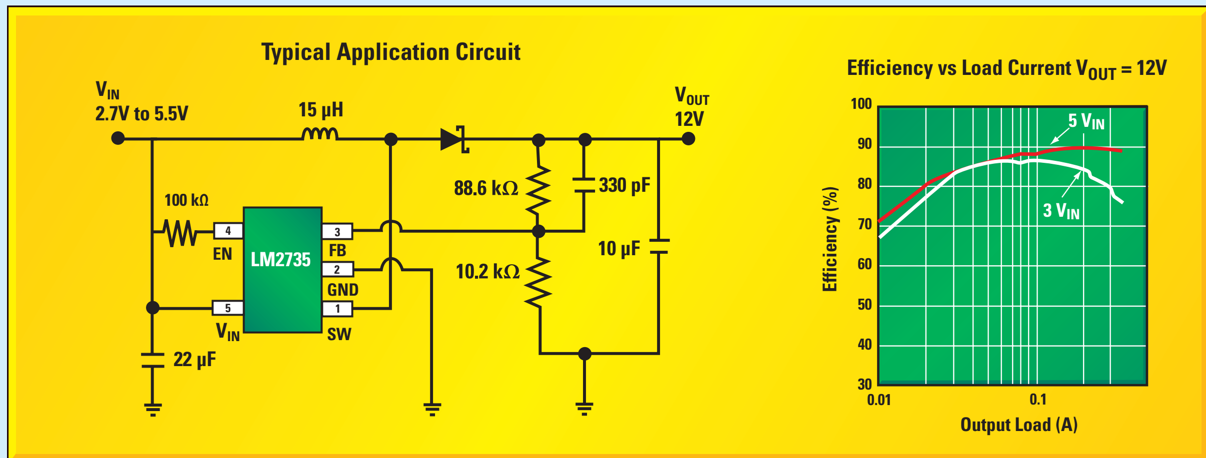

Features

High Output Current

- 2.1A Switch current over full temperature range
- Boost from 5V to 12V at 700 mA

Easy-to-Use, Small Solution Size

- Internal compensation allows for ease-of-use and minimal external components
- 1.6 MHz operating frequency uses tiny passive components
- SOT23-5, LLP-6, and eMSOP8 packages ideal for space constrained applications

Product ID	V_{IN} Range	Switch Current	V_{OUT} Max	Frequency	Ideal For	Package
LM2731	2.7V to 14V	1.4A	22V	600 KHz 160 MHz	XDSL modem, portable devices, white LED current sources	SOT23-5
LM2733	2.7V to 14V	1A	40V	600 KHz 1.60 MHz	TV tuners, set top boxes, white LED current sources	SOT23-5
NEW **LM2735**	2.7V to 5.5V	2.1A	24V	520 KHz 1.60 MHz	LCD and OLED displays for portable applications, USB powered devices, white LED current source	SOT23-5 LLP-6, eMSOP-8

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Calculating Losses and Junction Temperature for High-Power-Density Switching Converters

MOSFETs are to be off for a short period of time in order to eliminate “shoot through”. Shoot through is a term used to describe what would happen if both MOSFETs were on at the same time, and allowing V_{IN} to be shorted to ground. This would create a very large current spike through both MOSFETs. As the current ramps down in the control MOSFET, the body-diode current increases. There are losses associated with this transition, and it can be approximated with simple geometry. The area of the two triangles is a fairly good approximation of the power loss in the rising and falling transitions. The area of a triangle is 1/2 base x height. The power loss during the falling transition is:

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL})$$

The power loss during the rising transition is:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE})$$

The losses associated with the time that only the synchronous FET body diode is on are:

$$P_{DIODE} = (V_D \times I_{OUT} \times F_{SW} \times T_D)$$

The quiescent power losses associated with powering internal circuitry can be empirically measured by powering the device and disconnecting any load from the output. The input current drawn multiplied by the input voltage is a good approximation of the quiescent power loss.

$$P_Q = I_{IN} \times V_{IN}$$

Now that all significant power losses have been calculated, the overall efficiency can be calculated:

$$\text{Efficiency} = \eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Where $P_{LOSS} = P_{SWF} + P_{SWR} + P_{DIODE} + P_{SYNC} + P_{CTRL} + P_Q$

After understanding the most significant losses associated with a buck converter, it will be easier to see how recent advances in silicon technology have allowed National Semiconductor to create a family of high-density SOT-23 switchers. One of the easiest methods to describe the improvements is to discuss a common myth about monolithic power converters and efficiency. It is fairly common to hear that “if you want to improve efficiency, you need to use a lower switching-frequency device”. This is true only when comparing two DC-DC converters that are fabricated on similar processes. As an example, it was common to see 50 nS rise and fall times five years ago. Today, similar applications with newer technology delivering 5 nS rise and fall times are commonly seen. This is a significant improvement in order of magnitude.

By looking at the previous equations for transition losses, one can see how the switching losses easily could be much greater in a lower switching-frequency converter, depending on the two different technologies being compared. These improvements in switching transition times have allowed National to create 3 MHz converters with decreased losses compared to previous generations of lower switching-frequency converters. Higher switching-frequency converters also allow the customer to use smaller external capacitors and inductors allowing for a much smaller total application space.

A significant loss in a buck converter application is the conduction loss in the external inductor. The inductor has continuous current through the DT_S and $D'T_S$ periods, and R_{DCR} losses can be significant. For a given amount of PCB space for a converter, a lower-value inductor will allow a larger wire diameter and lower power loss.

The time that the body diode is on (time T_D), is another significant power loss that can be minimized with proper design. This time can increase or decrease depending on changes in input voltage and output load. By implementing active circuitry that minimizes this time, the body diode losses are minimized within the IC. Many National synchronous-buck-converter designs use active circuitry that reduces this time.

Thermals

After it is understood how losses in a DC-DC converter are calculated, it becomes easier to determine the temperature of the silicon junction of a specific application.

Calculating junction temperature with any amount of accuracy when using monolithic DC-DC converters has always been difficult for the customer. Often there is a recommended maximum junction temperature from the IC manufacturer without an accurate means of measuring this temperature.

Calculating Losses and Junction Temperature for High-Power-Density Switching Converters

The junction temperature of the device needs to be calculated to ensure reliable operation in a given application. There are many "rules of thumb" and helpful guides within National's datasheets. Following are also a couple of easy methods that will approximate the junction temperature of the device in a specific application.

$R_{\Theta JA}$, $R_{\Theta JC}$, and $R_{\Psi JC}$ Definitions:

$R_{\Theta JA}$: Thermal impedance from silicon junction to ambient air temperature. The units of measurement are °C/Watt.

$$R_{\Theta JA} = \frac{T_J - T_A}{P_{DISSIPATION}}$$

$R_{\Theta JC}$: Thermal impedance from silicon junction to device case temperature.

$$R_{\Theta JC} = \frac{T_J - T_{CASE}}{P_{DISSIPATION}}$$

Most data sheets contain values for $R_{\Theta JA}$ and $R_{\Theta JC}$ for each package. The datasheet values for $R_{\Theta JA}$ and $R_{\Theta JC}$ are given so that a comparison can be made between the thermal performances of one package to another. To compare packages, all other variables must be held constant (such as PCB size, copper weight, thermal vias, and power dissipation). This sheds some light on package performance, but it can be misleading to use these values to calculate the actual junction temperature in a given application.

$R_{\Theta JA}$ is the sum of smaller thermal impedances (see simplified thermal model in ***Figure 4***). To illustrate thermal impedance, an electrical analogy is commonly used. Thermal resistance is analogous to electrical resistance. Potential is analogous to temperature delta, and current is analogous to power flow. The capacitors shown in ***Figure 4*** represent delays that are present from the time that power and its associated heat is increased or decreased from a steady state in one medium until the time that the heat increase or decrease reaches a steady state in the other medium.

A common mistake is to assume that the top-case temperature represents the appropriate temperature when calculating $R_{\Theta JC}$. In fact, $R_{\Theta JC}$ represents the thermal impedance of all six sides of a package, not just the top side.

Therefore it would be improper to calculate the junction temperature using the $R_{\Theta JC}$ value given on the datasheet, while monitoring just the top-case temperature.

In order to properly calculate the junction temperature in the laboratory, one could define a thermal impedance that allows us to measure the top-case temperature with a thermal sensor attached. Let $R_{\Psi JC}$ represent the thermal impedance associated with just the top case to silicon junction.

Another common thermal impedance used to calculate junction temperature in the laboratory is $R_{\Psi J\text{-}PCB}$. This thermal impedance is defined as the thermal resistance from the silicon junction to the ground lead of the device.

These two thermal impedances allow the end user to calculate the junction temperature of our devices using the following method.

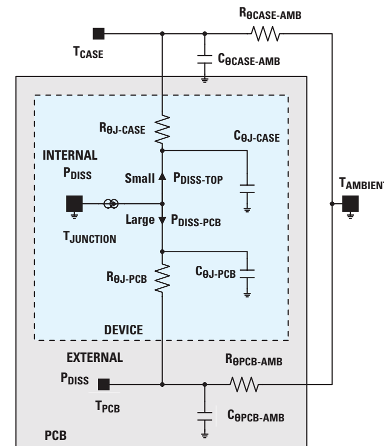

Figure 4. Monolithic DC-DC Converter Thermal Model

As is shown in the thermal model in ***Figure 4***, a few quick observations can be made about calculating junction temperature. Power dissipation from other components and devices will thermally couple into the device under test. This may seem obvious when stated explicitly, but when one looks at the equation that determines the junction temperature of the device under test, only its internal power dissipation is taken into account. The external power dissipation is accounted for to some extent if one uses the $R_{\Psi JC}$ and/or the $R_{\Psi J\text{-}PCB}$ method of determining junction temperature.

Calculating Losses and Junction Temperature for High-Power-Density Switching Converters

In most DC-DC converters, most of the heat is dissipated from the silicon to the package to the PCB, and finally to the ambient air. A much smaller amount of heat is dissipated from the silicon to the case and then to the ambient air. The split depends on how the device is manufactured. The device could be manufactured with a heat slug on the top or bottom of the die. Often a bottom thermal pad is used. Therefore, it is recommended to thermocouple to the case of the device and the ground lead to accurately measure the smallest thermal impedance. By using the smallest thermal impedance path, the error in calculating the junction temperature will be reduced.

Many of National's high-density converters contain an internal thermal-shutdown circuit. When the silicon reaches an approximate temperature of 165°C, the device shuts down until the temperature reduces to approximately 150°C. Taking advantage of the thermal shutdown allows the user to calculate the $R_{\Theta JA}$ or $R_{\Psi JC}$ of a specific application with reasonable accuracy.

Calculating T_J

During the prototyping stage of the design, the specific application is placed in a thermal chamber. Enough power in the device is dissipated to obtain a good thermal impedance value. It is important to remember that thermal impedance is not static over all input voltages, output voltages, and output current. Each time the specifications change, the thermal impedance may change.

The ambient air temperature should be increased and the top-case, ambient air temperature, and V_{OUT} or V_{SW} should be monitored. When the device shuts down, the two temperatures are recorded. The result is the ambient air temperature, the top-case temperature, and the internal power dissipation. Next, the value for $R_{\Theta JA}$ and/or $R_{\Psi JC}$ can be calculated. This is quite simple to accomplish, and is necessary if the design may be marginal with regard to thermals.

By knowing the ambient air and the top-case temperature when the junction is at 165°C, one can calculate the specific application thermal impedance.

Once thermal impedance is found and by working backwards, it is possible to determine the maximum power dissipation or ambient temperature that keeps

$$R_{\psi JC} = \frac{T_J - T_{TOP\text{-}CASE}}{P_{DISSIPATION}}$$

the junction temperature at or below the recommended maximum of 125°C.

Example: The LM2735 SOT-23 Boost Converter Junction Temperature

$V_{IN} = 5V$

$V_{OUT} = 12V$

$I_{OUT} = 500\ mA$

$P_{LOSS} = P_{DISS} = 475\ mW$

Airflow = 0 LFM

T_A @ Shutdown = 112˚C

$T_{TOP\text{-}CASE}$ @ Shutdown = 134˚C

$$R_{\Theta JA} = \frac{165°C - 112°C}{0.475W} = 112°C/W$$

$$R_{\psi JC} = \frac{165°C - 134°C}{0.475W} = 65°C/W$$

$$R_{\Theta JA} = \frac{125°C - T_A}{0.475W} = 112°C/W$$

As long as the ambient air temperature is below 72°C, the junction temperature will be within specification.

$$R_{\psi JC} = \frac{125°C - T_{TOP\text{-}CASE}}{0.475W} = 65°C/W$$

As long as the top-case temperature is below 94°C, the junction temperature will be within specification.

This is a first-order approximation and reasonable success has been achieved with matching actual junction temperature and measurements of T_J. This approximation is a much better method than simply using the thermal impedance numbers included in the device datasheet. ■

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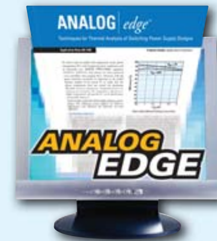

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