

ON-CHIP POWER MANAGEMENT UTILIZING AN EMBEDDED HARDWARE CONTROLLER AND A LOW-POWER SERIAL INTERFACE

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Abstract

This paper describes a hardware controller to reduce active power consumption in standard cell ASICs by adaptively adjusting the supply voltage to the minimum value required for a desired system performance. The hardware controller is embedded on the same die as the application ASIC. It consists of a hardware performance monitor, control logic and a serial interface logic. These functions combine to form a new control loop that regulates the speed of the application. A chip including the controller and a video processor was implemented in a 0.18 μ m standard CMOS process. Experimental results demonstrate operation over a frequency range from 6 MHz to 48 MHz and a supply voltage variation from 1.2 V to 1.8 V. Simulation results for a system implemented in a 0.13 μ m process are also presented.

1. Introduction

Power consumption of computing systems has grown to be of crucial importance in the recent years. The increased integration in embedded processing systems has led to an increase in their functional complexity. The current industry trend in portable computing demonstrates the demand for increased performance and low power / energy consumption. This puts a severe strain on the battery life. Hence what is needed is a low-power, high-throughput design methodology that extends the battery life without compromising the performance of the portable application.

In an embedded system, performing a processing task within a given time constraint can be accomplished in different ways. In a fixed voltage, fixed frequency scheme, the embedded processor is designed to operate at a supply voltage and clock frequency that satisfy the timing constraint for the worst-case processing task under worst-case operating conditions. Hence, for a task that has a lower timing constraint, the embedded processor is consuming energy even after the task has completed. This is especially true in systems that involve a user interface, in which the processor spends most of its time waiting for a response or command from the user. In a Run / Idle (or On / Off) scheme, energy is saved by operating the processor in a standby state (processor clock shut down) after the task is complete. The advantage of this scheme is its simplicity of implementation. In a variable voltage, variable frequency scheme, the idea is to scale the operating frequency according to the timing constraints of the application. Rather than completing every task in the shortest time possible and wait in standby mode until the next task, the processor could lower its frequency for low priority tasks and increase its frequency for high priority tasks while satisfying timing constraints under all operating conditions. In such a scheme, the supply voltage can be scaled with the frequency such that significant energy savings

are realized. At the software level, this scheme requires the operating system or task scheduler to provide the variable clock frequency to the embedded processor [1]. At the hardware level, this scheme requires a controller that varies the supply voltage to the processor to a value that is sufficient for correct operation for the given clock frequency.

The contribution of this paper is to introduce a hardware control scheme by which the supply voltage to a standard-cell CMOS digital application is optimized for a given performance requirement and for varying operating conditions. As shown in the block diagram of Figure 1, the input to the controller is a given performance requirement which is represented by the application clock frequency C_{Appclk} . The function of the controller is to determine the adaptive supply voltage V_{AVS} to the application which is sufficient for the application to operate properly at the given clock frequency. The output of the controller is a voltage value that is provided by an external high-efficiency voltage regulator. The controller is synthesizable in a standard-cell CMOS library and is embedded on the same die as the application. The controller design consumes little area and power overhead and allows for fast transient response to step changes in the performance requirement.

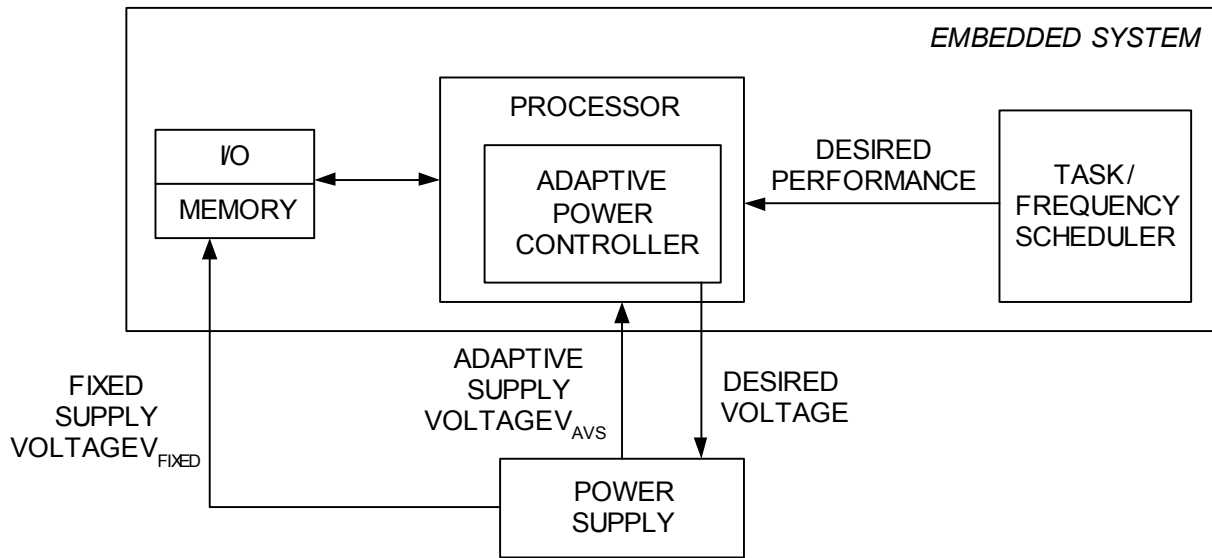


Figure 1. A block diagram of the adaptive voltage scaling system

This paper is organized as follows. In Section 2, the energy consumption in CMOS is described and a closed-loop adaptive supply voltage control scheme is compared to a Run / Idle control scheme for energy savings. In Section 3, the various approaches to adaptive voltage scaling are presented. A block diagram of the proposed controller is presented in Section 4 and the operation of the supply voltage control scheme is explained. Results from a test chip that incorporates the controller and a 32-bit microprocessor are shown in Section 5, followed by conclusions in Section 6.

2. Power / Energy Savings Using Different Supply Voltage Control Schemes

The power consumption of any CMOS digital circuit is the sum of its switching, leakage and short-circuit losses. Typically, the short-circuit losses are a small percentage of the total power consumption, hence the average power P of a processor can be given as

$$P = P_{switch} + P_{leakage} \approx C \times V_{DD}^2 f + V_{DD} \times I_{leakage}, \quad (2.1)$$

where C is a constant representing the average capacitance resulting from all the active switching cells in a processor, V_{DD} is the supply voltage, f is the clock frequency, and $I_{leakage}$ is the average leakage current of the processor.

Consider a processing environment with a fixed task time T . For a fixed voltage, fixed frequency scheme, the average energy for a given task completed in time $T_1 < T$ is given as:

$$E_{FIXED} = \int_0^T (P_{switch} + P_{leakage}) dt \approx \int_0^{T_1} (C_1 \times V_{DD}^2 f) dt + \int_{T_1}^T (C_2 \times V_{DD}^2 f) dt + \int_0^T (V_{DD} \times I_{leakage}) dt, \quad (2.2)$$

where C_1 is the average switching capacitance during the processing of the task, and C_2 is the average switching capacitance after the task is complete.

When the processor is operated in a Run/Idle scheme, the application clock is shut down after the task completes at time T_1 . In this case, the average energy consumption is given as

$$E_{RUN/IDLE} = \int_0^T (P_{switch} + P_{leakage}) dt \approx \int_0^{T_1} (C_1 \times V_{DD}^2 f) dt + \int_0^T (V_{DD} \times I_{leakage}) dt \quad (2.3)$$

It is observed from (2.3) that the energy losses due to switching power consumption P_{switch} are reduced compared to (2.2).

In an adaptive voltage scaling (AVS) scheme, the clock frequency f_1 is reduced such that the same task can be completed in time T . Accordingly, the supply voltage is adaptively changed to V_{DD1} for the reduced clock frequency. The average energy consumption in this case is

$$E_{AVS} = \int_0^T (P_{switch} + P_{leakage}) dt \approx \int_0^T (C_1 \times V_{DD1}^2 f_1) dt + \int_0^T (V_{DD1} \times I_{leakage}) dt. \quad (2.4)$$

Since in both cases the task performed is the same, we have $f * T_1 = f_1 * T$. Hence the average energy savings ΔE of the adaptive voltage scaling (AVS) scheme compared to a Run / Idle scheme is

$$\Delta E = \frac{(E_{RUN/IDLE} - E_{AVS})}{E_{RUN/IDLE}} \cong \frac{(V_{DD}^2 - V_{DD1}^2)}{V_{DD}^2} \times 100(\%) , \quad (2.5)$$

using (2.3) and (2.4) and with the leakage energy term ignored.

3. Open-Loop Dynamic Voltage Scaling (DVS) and Closed-Loop Adaptive Voltage Scaling (AVS)

A simple approach to voltage scaling is to generate a lookup table of voltage vs. frequency values as shown in Figure 2. This paper refers to this open loop, table based method as dynamic voltage scaling (DVS). For a given clock frequency, the supply voltage value is the

worst-case value needed over all process and temperature variations. While open-loop DVS can yield a good amount of energy savings, it does not realize all the energy savings available. Every operating frequency/voltage pair in a processor must be characterized such that over parts and temperature the operating voltage is high enough to meet timing criteria. This characterized voltage must also include headroom for the power supply regulation error (typically 5 to 10%). Accounting for process, temperature, and power supply variation, the table based DVS is at best conservative, and requires tedious characterization at all the operating frequencies.

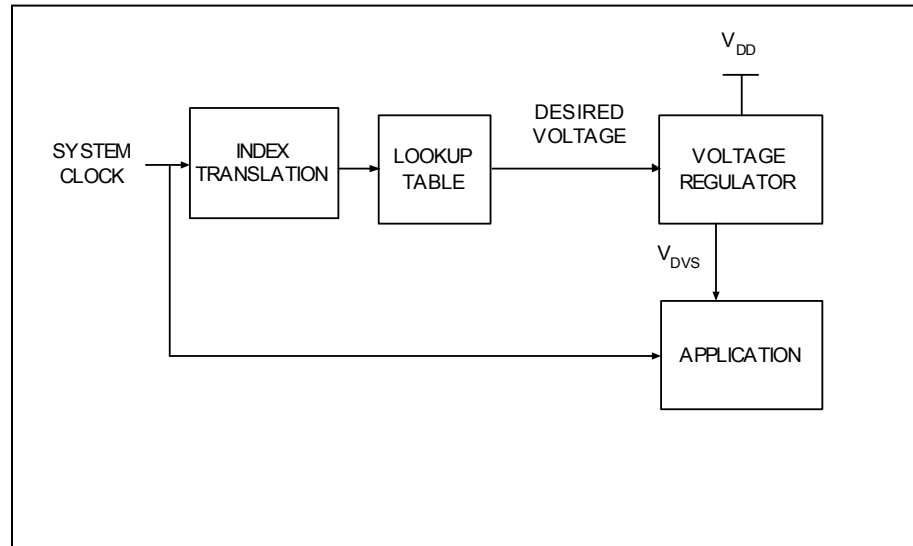


Figure 2. Block diagram of an Open-loop Dynamic Voltage Scaling scheme

A closed-loop AVS scheme uses a feedback loop to regulate the logic cell delay over “disturbances” in the system (process, temperature, and power supply variations). The feedback loop automatically adjusts the supply voltage to the minimum value required to meet timing criteria. Closed loop AVS offers a significant energy savings without the careful characterization required for determining the open loop DVS voltage/frequency table.

The block diagram of a closed-loop AVS system described in this paper is shown in Figure 3. It consists of three functional blocks: the adaptive power controller (APC), PowerWise™ Interface (PWI) [2], and a power management unit (PMU). These components form a system that automatically sets the minimum supply voltage for any performance level (clock frequency), temperature, or process variation. The hardware performance monitor (HPM) senses the silicon performance in real time. The HPM and the processor share a common supply voltage such that the silicon performance for the processor is reflected by the HPM. The HPM resides with the processor, enabling it to detect temperature and silicon processing variations. The APC, which is also part of the processor, provides an interface to and from the host processor and power supply, and processes data to control the power supply. Serial data is sent to the power supply via the 2 wire, open standard PWI. The power supply provides the supply and auxiliary voltages for the processor. The power supply must be able to adjust its voltage as commanded by the APC, and do so in a timely manner such that the AVS feedback loop is stable.

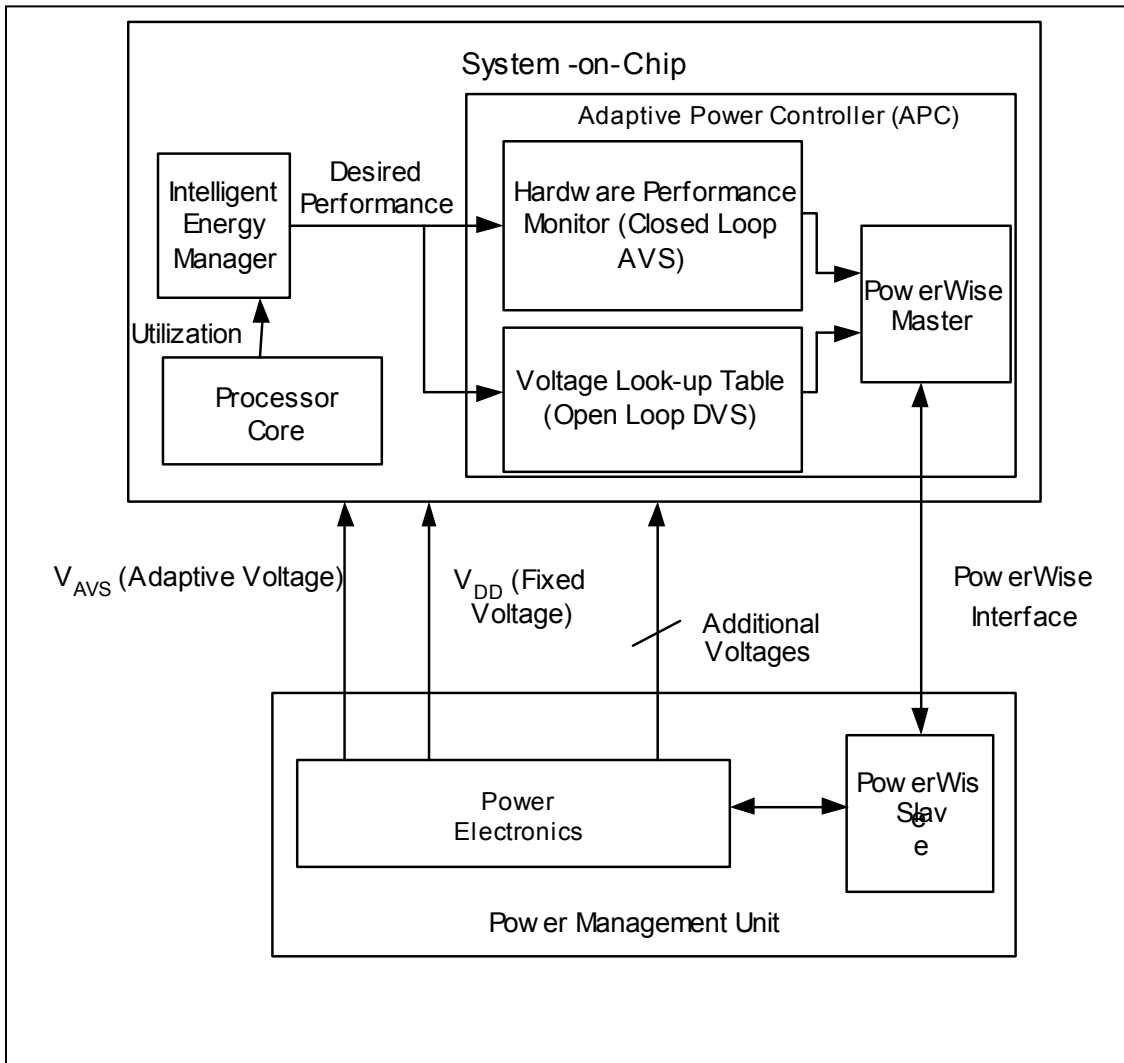


Figure 3. Block diagram of the proposed open-loop DVS / closed-loop AVS system

Closed loop AVS guarantees near minimum power dissipation of the core logic. A control loop can be designed to regulate its output to a reference input, even if disturbances enter the system. Thus the challenge of output control is reduced to the simple matter of picking a reference input. In closed loop AVS, the HPM and sampled-data control form the discrete-time sensing, feedback, comparing, and compensation part of the loop, with the power supply closing the control loop, as shown in Figure 3.

4. The Adaptive Power Controller (APC)

The adaptive power controller handles all aspects of voltage control, and has the ability to actively minimize the power consumption of the host processor. It is realized in synthesizable

RTL and has the following functional components: (i) Hardware Performance Monitor (HPM), (ii) digital loop filter and (iii) PowerWise™ Interface (PWI) master module. These elements work together to allow simple and accurate voltage control from the external power supply.

The hardware performance monitor (HPM) and digital loop filter are used in closed loop AVS to measure the performance of the digital circuit for a given operating performance requirement. The measurement data from the HPM is processed in the digital loop filter and sent to the PWI master to transmit to the power supply. The APC can also be used for open-loop DVS through a programmable voltage-vs-frequency lookup table.

The HPM is a key component of the control loop. The HPM generates a measurement that relates the maximum number of logic levels an input vector to the application can travel through at the given clock frequency, supply voltage and operating conditions. This is a useful measurement, since the minimum supply voltage to the application is dictated by the critical path delay satisfying a timing constraint. While the HPM does not provide an absolute measure of the logic timing, it provides a relative measurement that is coupled to the process, temperature, and voltage variation seen by the application. A relative measurement of silicon performance is sufficient to control the actual performance.

Understanding the measurement reveals the objective of the control loop: to regulate silicon performance. The control loop accomplishes this by comparing, through a feedback path, the measured output from the HPM to the input reference. The input reference represents the desired performance level that the control will regulate to. If the HPM output is not equal to the reference, some error (difference) will be processed to give some adjustment to the supply voltage until equilibrium is established.

In the closed loop AVS system, there exists both continuous time (power supply) and discrete time (HPM, discrete compensation) elements. Therefore, sampled-data theory can be used to analyze the system. Detailed analysis of sampled-data control is not presented here, but the reader is directed to [3], one of the many sampled-data text available. Instead, some key points to the analysis will be made. The HPM outputs a digital word and has as its input both desired performance (clock frequency) and analog voltage. This digital word is a relative measurement of the processor core performance. The sampled-data control loop attempts to regulate this measured output to the reference input, which is also a digital word. The loop stability will be determined by the discrete-time compensation, which can be implemented any number of ways. However, assuming that the loop is made stable, there is a requirement to calibrate the reference input to the processor core properties.

As shown in the simplified block diagram of Figure 4., the Adaptive Power Controller consists of the following components:

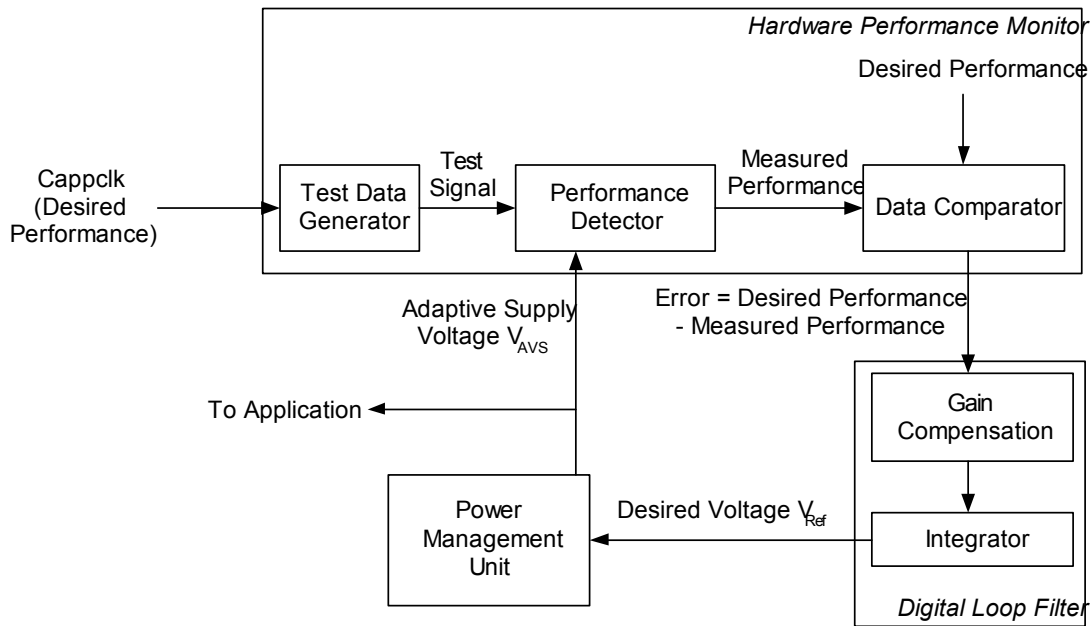


Figure 4. Simplified block diagram of the Adaptive Power Controller (APC)

1. Hardware Performance Monitor: The functionality satisfied by this module is two-fold:

(a) in the closed-loop AVS scheme it provides a supply voltage which is greater than the minimum operating voltage for the application for a given performance and operating conditions.

(b) the closed-loop supply voltage is greater than the minimum operating voltage by a design margin over all performance and operating conditions.

The Hardware Performance Monitor (HPM) consists of the following blocks:

- (i) Test Generator: This module generates a test vector that is used to measure the silicon performance.
- (ii) Performance Detector: This module measures the performance of the application. The performance measurement is performed on a timing model that closely represents the the timing characteristics of the application. Changes in the timing of the application due to variation in supply voltage, process technology, and temperature are reflected in the performance measurement. The performance detector is designed to be fully synthesizable with programmable parameters that tailor it to a given application and process technology. Programming of the performance detector is performed during hardware characterization of the application silicon.
- (iii) Output Data Comparator: This module compares the output of the performance detector to the desired performance level and outputs a signed integer representing the error between the two. This error gets processed by the loop filter to ultimately transmit to the power supply as a voltage command.

2. Digital Loop Filter: The output of the Hardware Performance Monitor (HPM) is sent to a digital loop filter that consists of a gain compensator block and an integrator block, to obtain an averaged voltage value $V_{Ref} \propto V_{DD}$. In steady state, when the output of the HPM is zero (no error) the voltage value V_{ref} (represented as a digital word) is proportional to the desired supply voltage for the given performance requirement.

3. PowerWise™ Interface Master: The digital output from the loop filter is serialized and sent off-chip to the Power Management Unit (PMU) to provide the adaptive supply voltage $V_{AVS} \propto V_{Ref}$ (in steady state). The rate at which the digital voltage value is sent off-chip is a function of the time constant of the power supply to respond to changes in the steady state voltage value. To adapt to different power supplies that can be used with APC, the serial interface rate is made programmable.

4. Results

The proposed scheme is implemented in a 0.18 μm standard CMOS process. The application is a video processor consisting of an ARM-7 core processor and associated memory and I/O logic. The processor and the peripheral logic modules are provided with an adaptive supply voltage varying from 1.2 V to 1.8 V typical. I/O, analog and clock generation circuitry are provided a fixed voltage supply of 1.8v.

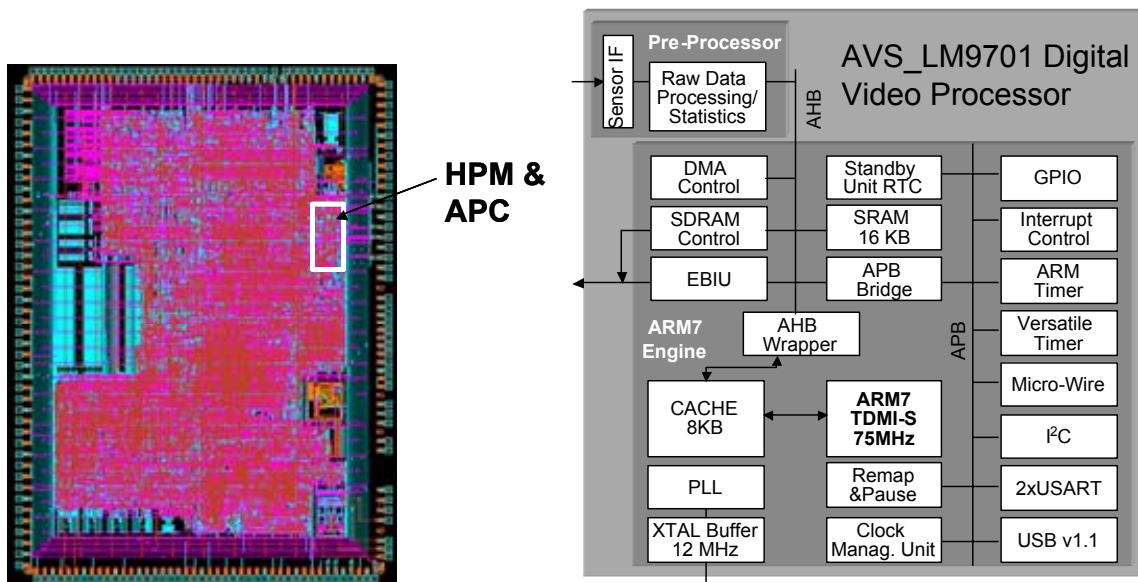


Figure 5. Die photo of the implemented system consisting of the proposed controller and a video processor based on the ARM-7 core

Figure 6 shows a plot of the power at different performance (clock frequency) levels for the video processor chip. The test system has the ability to switch between fixed frequency/voltage and closed loop AVS in real time, with power measurement feedback to capture the data shown in the figure. The result is a side-by-side comparison of the fixed frequency/voltage and closed loop AVS methods processing the same code at the same frequencies on the same processor. For the test case shown in Figure 6, the total energy consumed without AVS is 342 mJ and with AVS is 141 mJ, a 59 % savings in energy consumption.

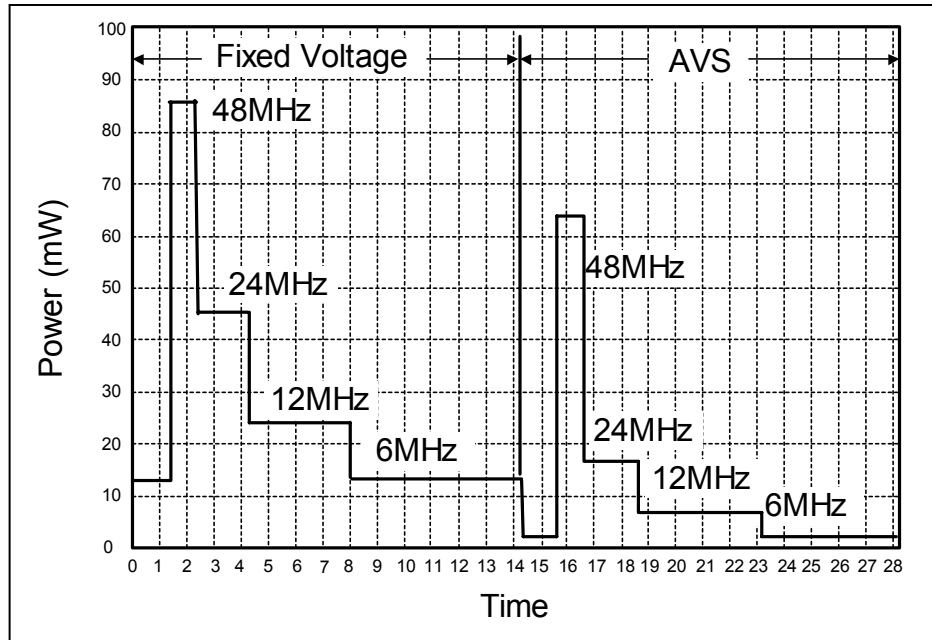


Figure 6. Power measurements taken on a 0.18 um video processor.

Figure 7. is a simulation plot of an open-loop DVS scheme versus the proposed closed-loop AVS scheme for a 0.13um process. Inherent to closed-loop AVS is the ability to automatically compensate for temperature and process variations. The effect is that slow silicon at high temperature will operate at a higher voltage than fast silicon at cold temperatures. The voltage is adaptively set for the conditions of the processor. This results in dramatic power and energy savings even when compared to an open loop AVS scheme. The reason is that process and temperature guard bands can be ignored in the closed loop AVS scheme, and typical silicon at typical operating temperatures will operate at substantially lower voltages

The open loop AVS scheme used to capture this data is a two level method in which the voltage is 1.2V between clock frequencies of 48MHz and 96MHz, and 0.9V between 6MHz and 48MHz. The open loop voltage levels have to be worst case figures to allow for temperature and process variations, and also power supply regulation. Assuming gaussian distribution, typical silicon at room temperatures are the most common occurring conditions, and from Figure 7 it is clear that closed loop AVS provides significant efficiency improvements over open loop DVS at the typical conditions. Indeed, even at the worst case conditions (slow silicon at high temperature), closed loop AVS operates at a lower power.

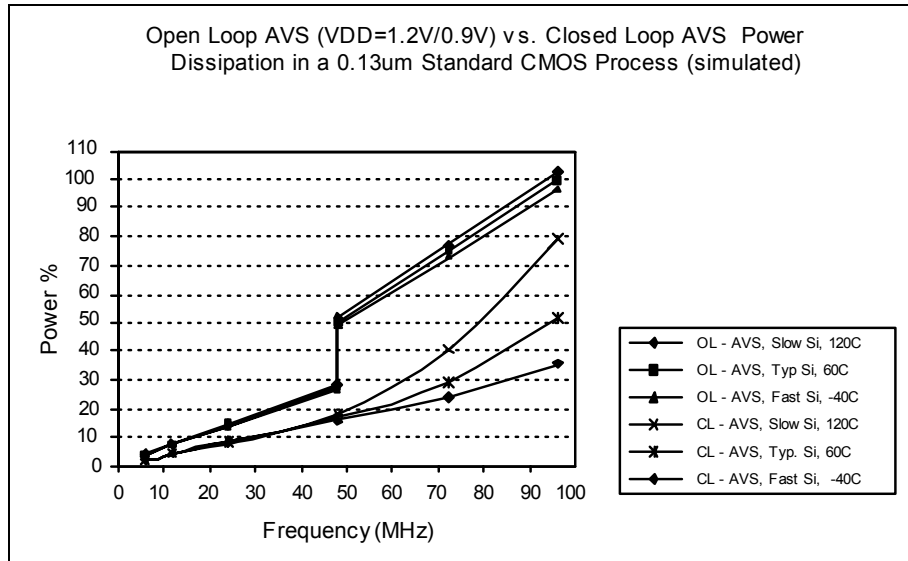


Figure 7. Power dissipation comparison between Open loop AVS and Closed Loop AVS. The open loop method uses two voltages (1.2V between 48MHz and 96MHz, and 0.9V between 6MHz and 48MHz).

6. Conclusions

A hardware controller for adaptive voltage scaling (AVS) has been demonstrated. It is shown that the controller can adaptively adjust the supply voltage to the minimum possible value for correct operation of the application. For a given performance requirement, a simple implementation consisting of a performance measuring hardware, digital control and a serial interface allow for scaling of voltages over a wide range of clock frequencies. Experimental results for a video processor show an energy savings upto 80 % when compared to a fixed voltage scheme and simulation results for a 0.13um process show energy saving upto 66 % when compared to a two-step (two-tier) open-loop DVS scheme.

7. References

- [1] K. Flautner and T. Mudge, Vertigo: Automatic Performance-Setting for Linux, *Proceedings of the 5th Symposium on Operating Systems Design and Implementation (OSDI 2002)*, Boston, MA, 2002
- [2] PowerWise™ Interface, URL: <http://powerwise.national.com>
- [3] *Digital Control of Dynamic Systems*, F. Franklin, J. David Powell and Michael L. Workman