

Application Challenges of High Voltage Hysteretic Buck Regulators

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Abstract: - Hysteretically controlled Buck regulators offer low cost, ease of implementation and excellent transient response, since loop compensation is unnecessary. The application challenges associated with hysteretic buck regulators include, variable operating frequency and protection during overload conditions. These challenges are exacerbated in higher input voltage applications. This paper describes a hysteretic control method which allows constant frequency operation for a large portion of the operational load range and widely varying input voltage. A protection method has been developed which protects the power switching components in the event of a small overload or complete short circuit, while minimizing foldback. The proposed application solutions and test results will be presented.

When the feedback voltage exceeds the OFF reference voltage, the comparator output goes low, turning off the buck switch. The switch will remain off until the feedback voltage falls below the ON reference hysteresis voltage, at which time the comparator output goes high, turning on the switch and allowing the output voltage to rise again.

This topology provides many benefits. It is extremely fast at reacting to load and line transients, due to the very wide bandwidth control loop that does not require an error amplifier or frequency compensation. Thus, total component count is reduced and the output capacitance can be minimized. However, the operating frequency of a hysteretic regulator is dependant on several variables, including the input / output voltages, output filter inductance, hysteresis window and capacitor equivalent series resistance.

I. BACKGROUND

The hysteretic architecture is the simplest control method for a Buck regulator. The modulator is simply a comparator with input hysteresis that compares the output feedback voltage to a reference voltage.

$$F_{SW} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT}) \cdot ESR}{V_{IN} \cdot L \cdot V_{HYS}}$$

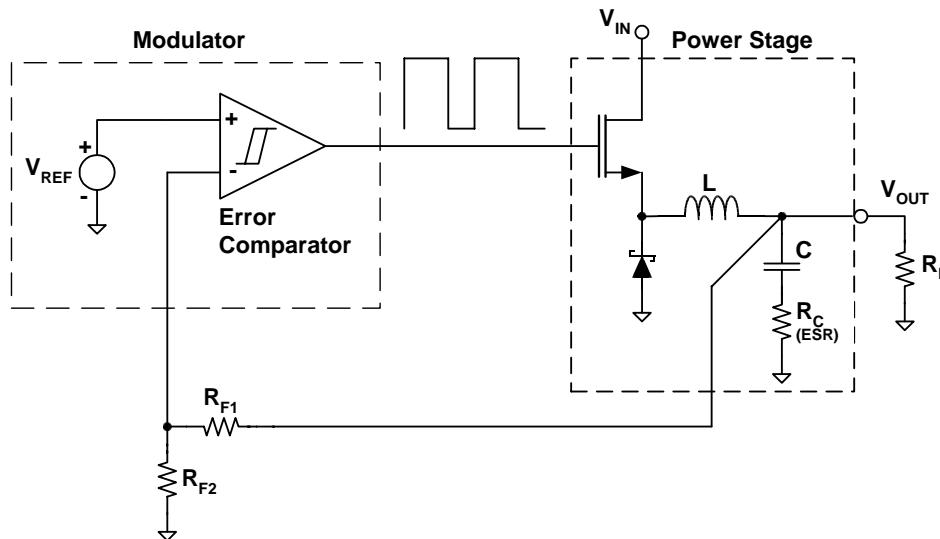


Figure 1. Hysteretic Buck Regulator

Constant On Time Architecture

Hysteretic regulators implemented with a comparator as described, operate over a wide frequency range as the line and load conditions are varied. This varying frequency imposes filtering and noise challenges since the filtering components cannot be optimized due to the varying frequency. The Constant On Time architecture is a variation of hysteretic control which operates at a relatively fixed frequency without a clock, even with varying input line and output loading conditions. Shown in Figure 2 is the power stage of a Buck regulator operating in continuous conduction (the inductor current always remains positive) mode.

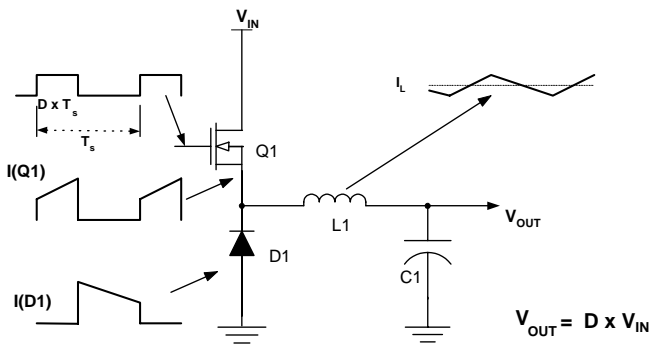


Figure 2. Buck Regulator Operation

The output voltage (V_{out}) is equal to $D \times V_{in}$, where D is the duty cycle ratio of the Buck switch $Q1$ and V_{in} is the input voltage. The duty cycle D is equal to T_{on} / T_s , where T_{on} is the on time of $Q1$ and T_s is the switching period ($1/F_s$). If we assume the diode forward drop is small relative to V_{out} then in steady state:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{T_{ON}}{(1/F_s)} = T_{on} \cdot F_s$$

Shown in Figure 3 is a hysteretic regulator, which rather than using a dual level comparator, uses a circuit which turns on $Q1$ for a time (T_{on}) which is inversely proportional to the input voltage (V_{in}). This regulator does not contain a clock oscillator, yet operates at a fixed frequency even as the input voltage varies from 12V to 75V. The two main blocks within this regulator are the ON Time One-shot and the Regulation Comparator. The Regulation Comparator monitors the output voltage. If the output voltage is lower than the turn-on target value the comparator enables the buck switch $Q1$ for a period of time determined by the ON Time One-shot. The time period of the ON Time One-shot:

$$T_{on} = \frac{K \cdot R_{ON}}{V_{IN}}$$

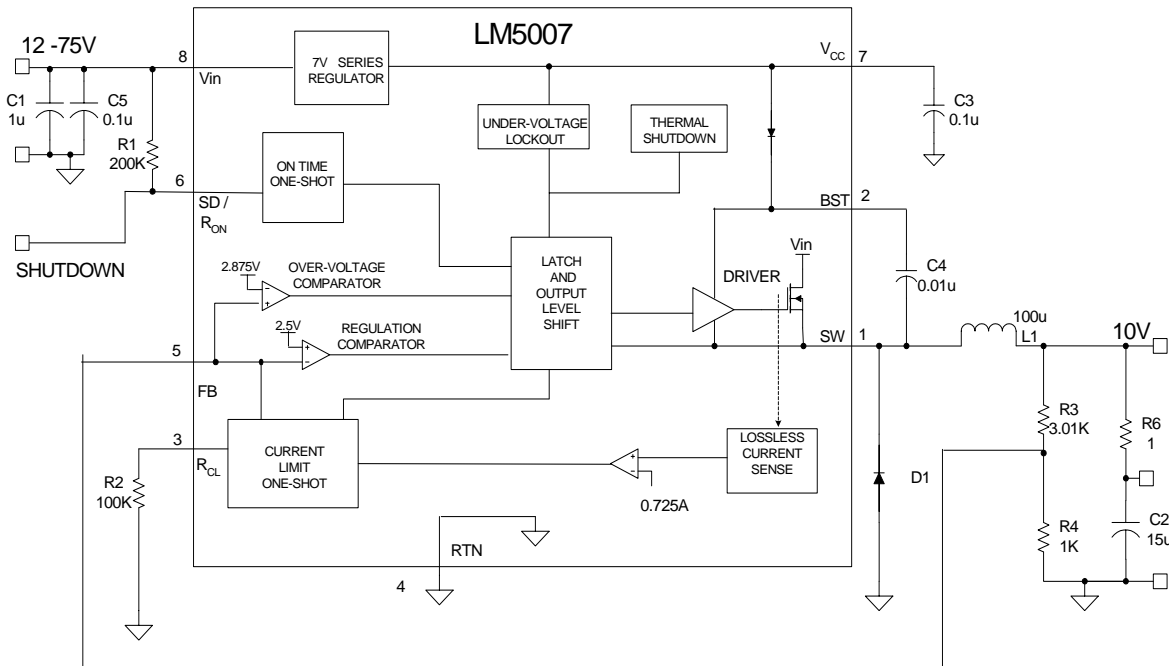


Figure 3. Buck Regulator with On Time Inversely Proportional to V_{in}

Where K is a constant (1.3×10^{-10}), R_{ON} is a configuration resistor and V_{in} is the input voltage.

If we now substitute T_{on} into the previous Buck Regulator equation an interesting result occurs:

$$\frac{V_{out}}{V_{in}} = \frac{F_s \times K \times R_{ON}}{V_{in}}$$

If we re-arrange and solve for F_s we get:

$$F_s = \frac{V_{out}}{K \times R_{ON}}$$

Since the output voltage (V_{out}) remains regulated and the K and R_{ON} terms are constants the switching frequency also remains constant. Actual operating frequency measurements for varying input voltage are shown in Figure 4.

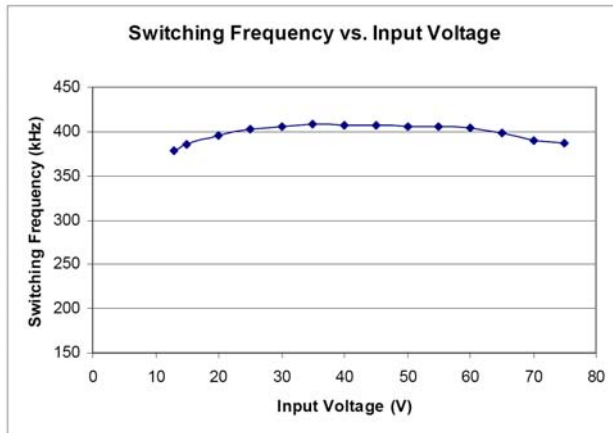


Figure 4. Operational Frequency vs Input Voltage

The constant frequency relationship holds true provided the inductor current remains continuous. At lighter loading the current in the inductor will become discontinuous (the inductor current returns to zero before the end of the switching cycle). At the onset of discontinuous operation the switching frequency will begin to reduce. The switching frequency at discontinuous mode is derived as follows:

Peak Inductor Current:

$$I_p = \frac{(V_{in} - V_{out}) \times T_{on}}{L} = \frac{(V_{in} - V_{out}) \times K \times R_{ON}}{L \times V_{in}}$$

$$= \frac{(1 - V_{out}/V_{in}) \times K \times R_{ON}}{L}$$

For high input, lower output voltage applications the discontinuous mode peak inductor current can be simplified to:

$$I_p = \frac{K \times R_{ON}}{L}$$

Output Power:

$$P_{out} = \frac{V_{out}^2}{R_{LOAD}} = \frac{L \times I_p^2 \times F}{2} = \frac{F \times K^2 \times R_{ON}^2}{2}$$

Solving for F_s :

$$F_s = \frac{V_{out}^2 \times L}{R_{LOAD} \times K^2 \times R_{ON}^2}$$

Note that the switching frequency will vary inversely to the output load resistance (R_{LOAD}) since all of the other parameters in the above equation are constants. Actual operating frequency measurements with varying load current are shown in Figure 5. The sharp reduction in operating frequency occurs at the onset of discontinuous operation.

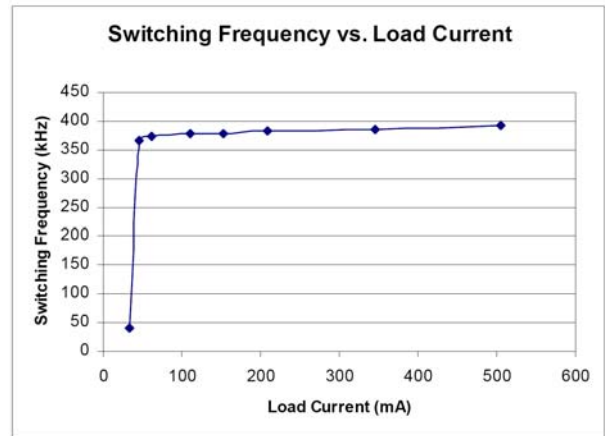


Figure 5. Operational Frequency vs Load Current

A reduction in operational frequency will occur at low loading levels when the output inductor enters discontinuous mode. This effect is desirable to maintain the conversion efficiency at light loads since the switching losses will be reduced in proportion to the switching frequency.

II. Overload Protection

A current monitoring circuit is required to protect the regulator in the event of an output overload condition. Overloads vary widely from minor over-current events to complete short circuits. The current limit protection approach used in a hysteretic regulator is similar to the cycle-by-cycle protection used in most clock driven switching regulators. The buck switch current is continuously monitored using a loss-less sensing technique and a comparator. If an over-current level is detected, the comparator trips and the buck switch is immediately turned off. The remainder of the clock period determines the Toff time for clock-based regulators. Since hysteretic regulators do not rely on a system clock a challenge arises to determine an appropriate Toff time following a detected overload condition.

There are several considerations when determining an appropriate Toff time. First, the current monitor and comparator will have some delay and associated current overshoot before the buck switch actually turns off once the overload is detected. This delay leads to a minimum on time each cycle, even for the largest overloads since the comparator requires a finite time to react to the overload. Once off, the buck switch must remain off for a minimum Toff time period necessary for the inductor current to decay back below the over-current threshold. Secondly, a volt second balance must be satisfied for the output inductor to keep the inductor current in control and prevent a runaway condition. The inductor volt-second ON product must be less than the volt-second OFF product to limit the current in the inductor. If the response time of the over-current comparator is not sufficiently fast a potential exists for a runaway inductor current condition. The worst-case condition is seen at high line input voltage and a short-circuited output creating a zero output voltage. In order to ensure this runaway condition does not develop the following inequality must be satisfied:

$$(V_{in} - V_{out}) \times T_{on} < T_{off} \times (V_d + V_{out} + (I \times R))$$

Ton is the switch on time determined by the over-current comparator response time. Toff is the switch off time, which is determined by the controller. Vd is the freewheeling rectifier diode voltage drop. I is the inductor current and R is the total series resistance around the inductor / diode / Vout loop. It can be seen that higher input voltages and a slower comparator response time (increasing Ton) increases the left side of the equation. Whereas, a short circuit (Vout = 0), small diode voltage drops or a low resistance inductor reduces the left side of the equation.

One way to eliminate the possibility of a runaway condition, for a very conservative design, is to set the overload off time very large. Although effective, even the smallest overloads, once detected, can cause the output voltage to completely collapse to zero. A large Toff time after current limit produces a large amount of foldback in the output I vs V characteristic. This foldback will require that the load be greatly reduced following an overload event in order for the regulator to return to normal regulation.

A better approach for a hysteretic regulator overload protection circuit is to dynamically choose the Toff time. Referring again to the inductor runaway equation, the off time is best set inversely proportional to the output voltage (Vout). Using this approach during small overloads when the output voltage is still close to the regulation point a minimum overload off time is selected. During large overload conditions when the output voltage falls greatly (to zero at short circuit) a large overload off time is selected to preclude a runaway condition. This dynamic overload off time approach can be configured such that the regulator is fully protected during all types of faults while minimizing the foldback. Figure 6 shows a hysteretic regulator overload response implemented with a fixed 9us delay for the overload response off time. This regulator is designed for 10V output with a 0.5A current limit. The input range is 12V to 75V. The plot shows the output voltage as load is increased from zero to beyond the current limit then decreased back to zero.

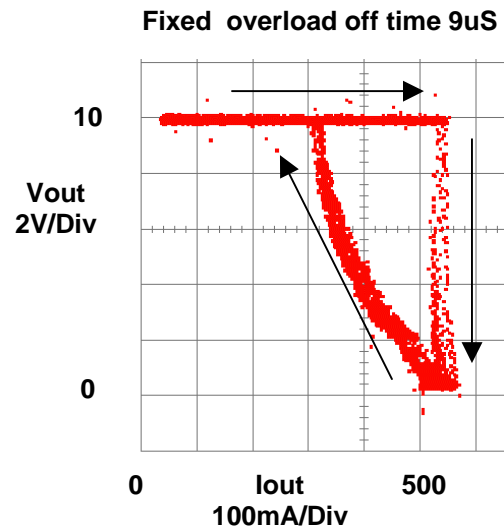


Figure 6. Overload Profile Utilizing Fixed Overload Off Time

Approximately 40% foldback in loading is required following an overload condition, before the output voltage recovers to the normal regulation level. Although adequately protected, this regulator could have start up issues plus a minor overload transient may collapse the regulator plus output all the way to zero volts.

Figure 7 shows the same hysteretic regulator; with the overload response off time implemented using a dynamic delay.

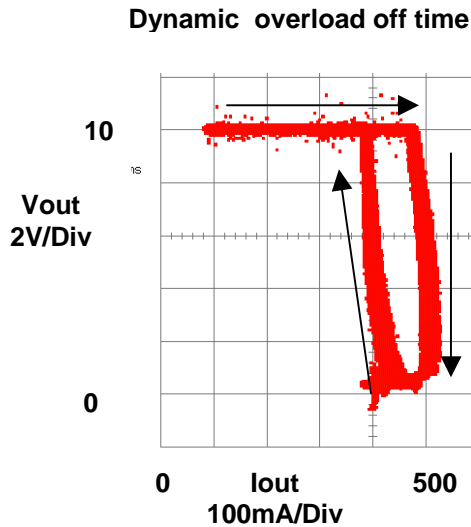


Figure 7. Overload Profile Utilizing Dynamic Overload Off Time

With this implementation utilizing the dynamic approach, the overload response time is varied from 2.5us for small overloads where Vout is still near the regulation point (10V) to 17us for short circuit conditions where Vout is zero. Using this dynamic approach the foldback is reduced to approximately 20%.

IV. Summary

Fixed frequency operation can be achieved in a hysteretic buck regulator without an oscillator. This approach offers a low cost, easy to implement, step down regulator. There are no loop compensation or stability issues to worry about. The transient response is very fast, since there is no bandwidth limiting feedback components. Depending upon the inductor value and load range, the operating frequency will remain constant for most of the output power range.

A dynamic off time overload protection scheme protects the regulator during overloads. This dynamic approach minimizes the foldback load effect.

V. Acknowledgments

The author would like to thank and acknowledge Steven Barrow and David Pace for their significant contributions to this work.