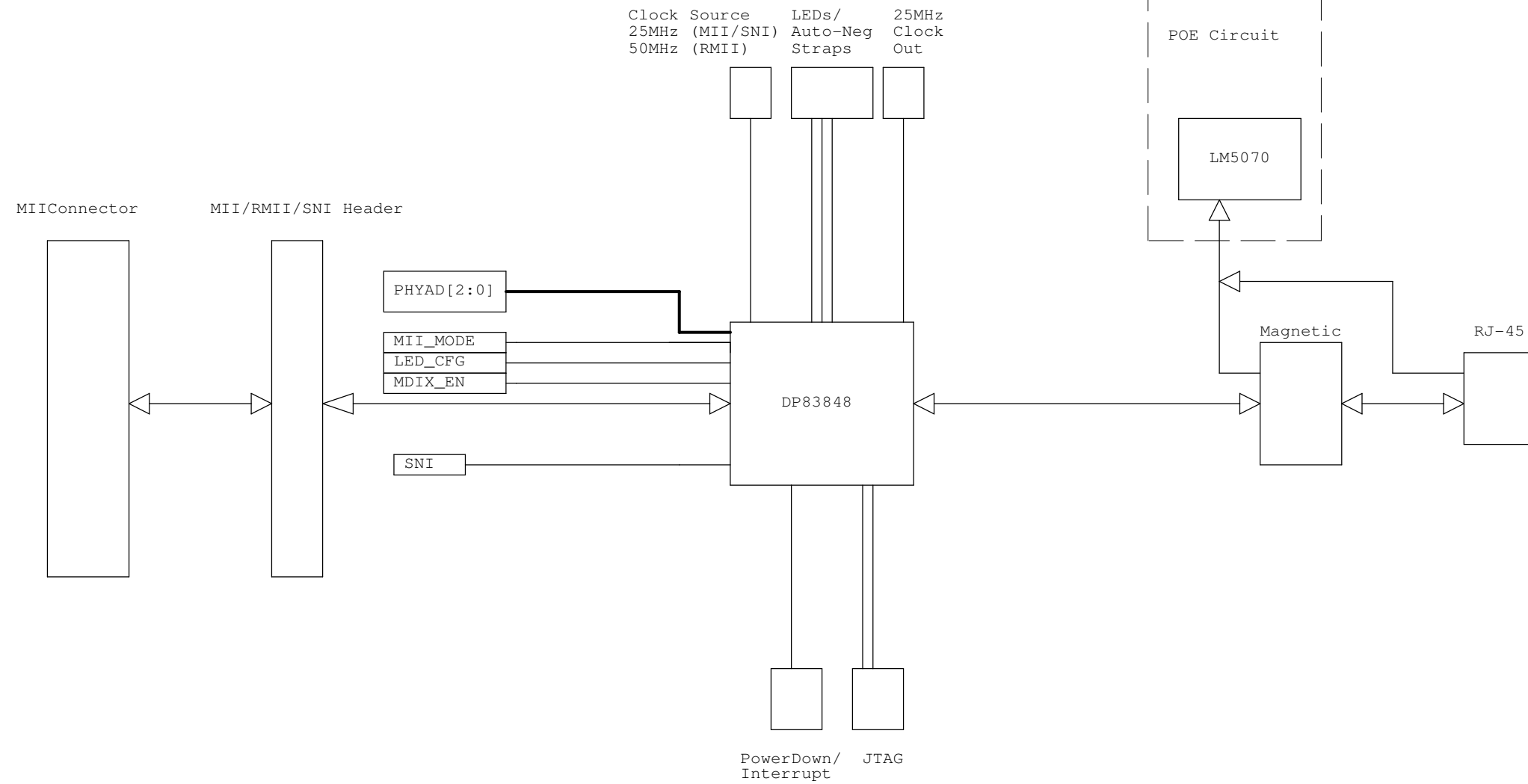


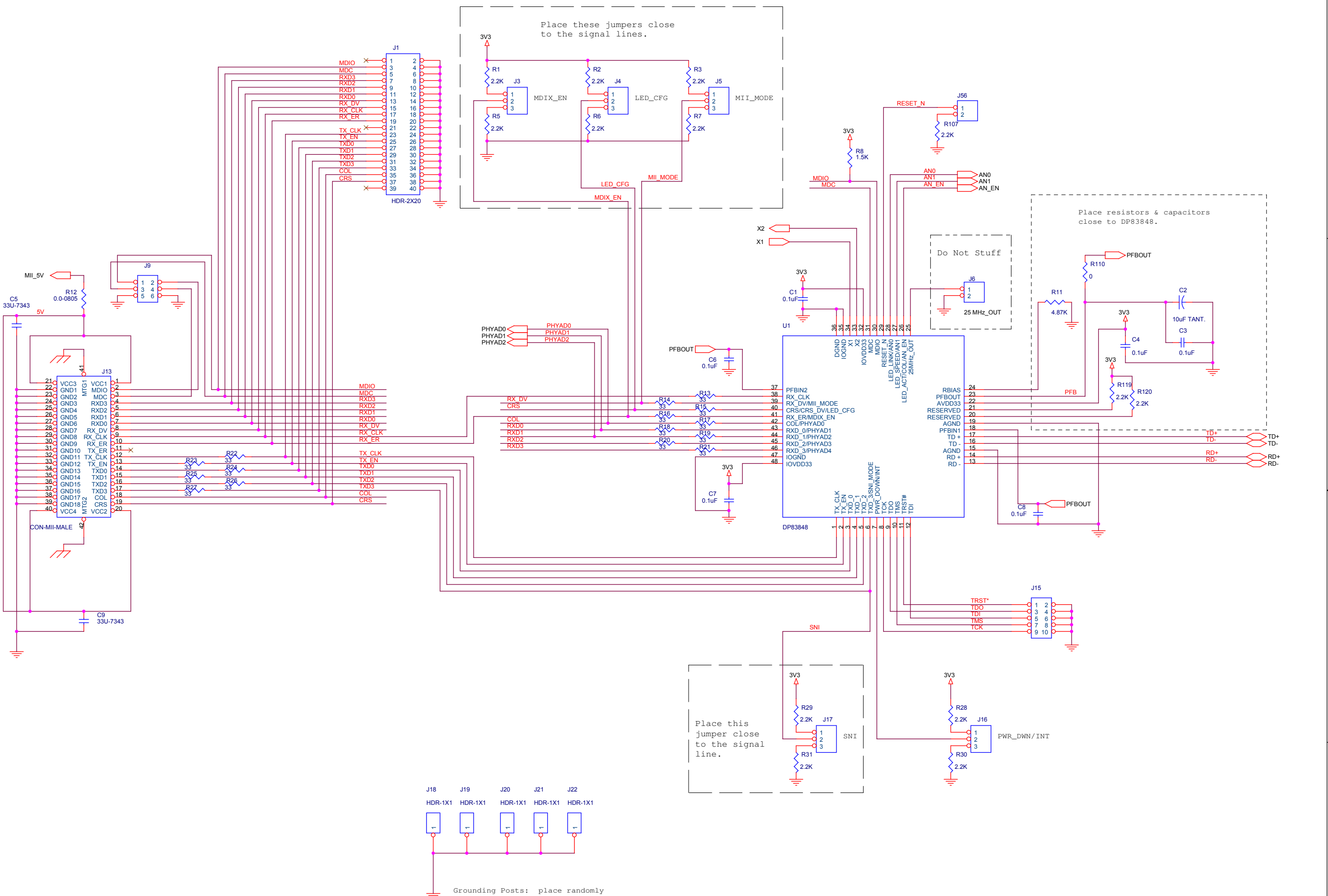
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Release note:

- Revision B is to provide actual implementation on how to improve EMI beyond revision A2. This is to be used for information purpose only. No board has been fabricated.



Title		
DP83848 AspenPhy Demo II - Cover		
Size	Document Number	Rev
C	870012505-100	B
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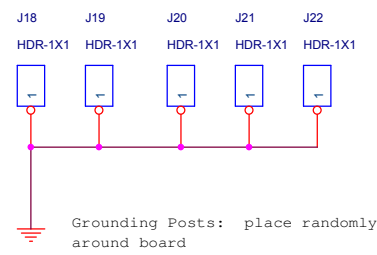


Place these jumpers close to the signal lines.

Place resistors & capacitors close to DP83848.

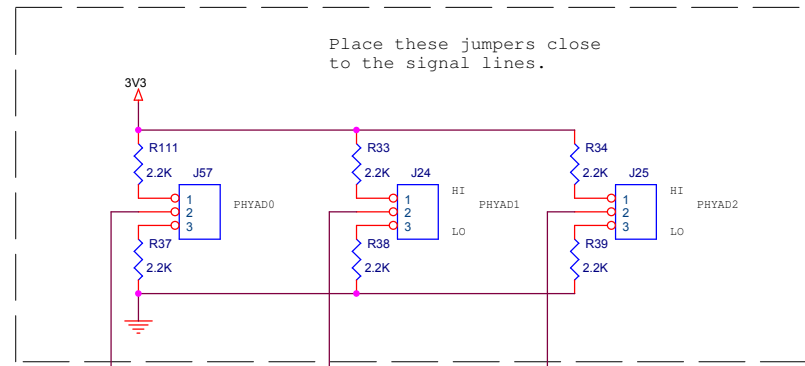
Do Not Stuff

Place this jumper close to the signal line.



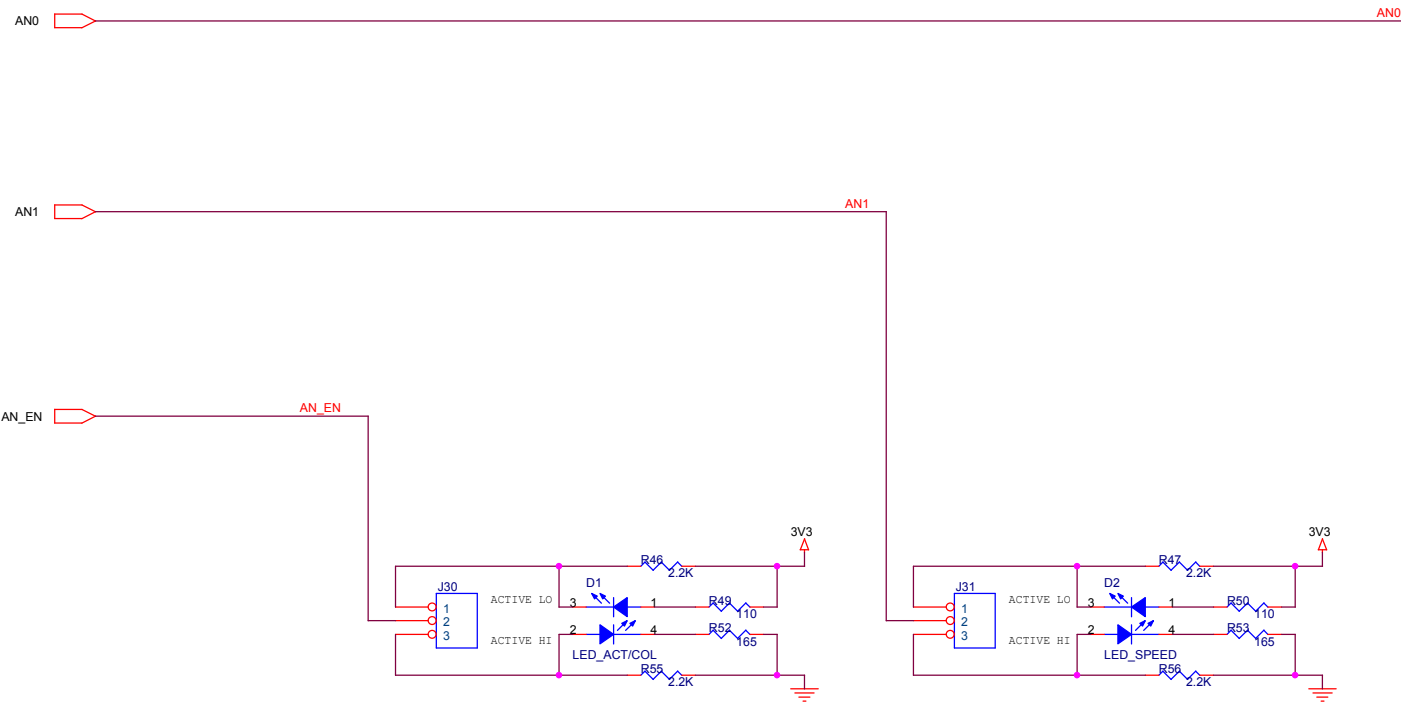
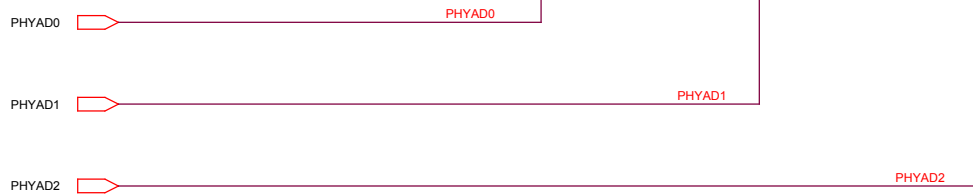
Grounding Posts: place randomly around board

Title		
DP83848 AspenPhy Demo II - Ethernet Phy Page		
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C	870012505-100	B
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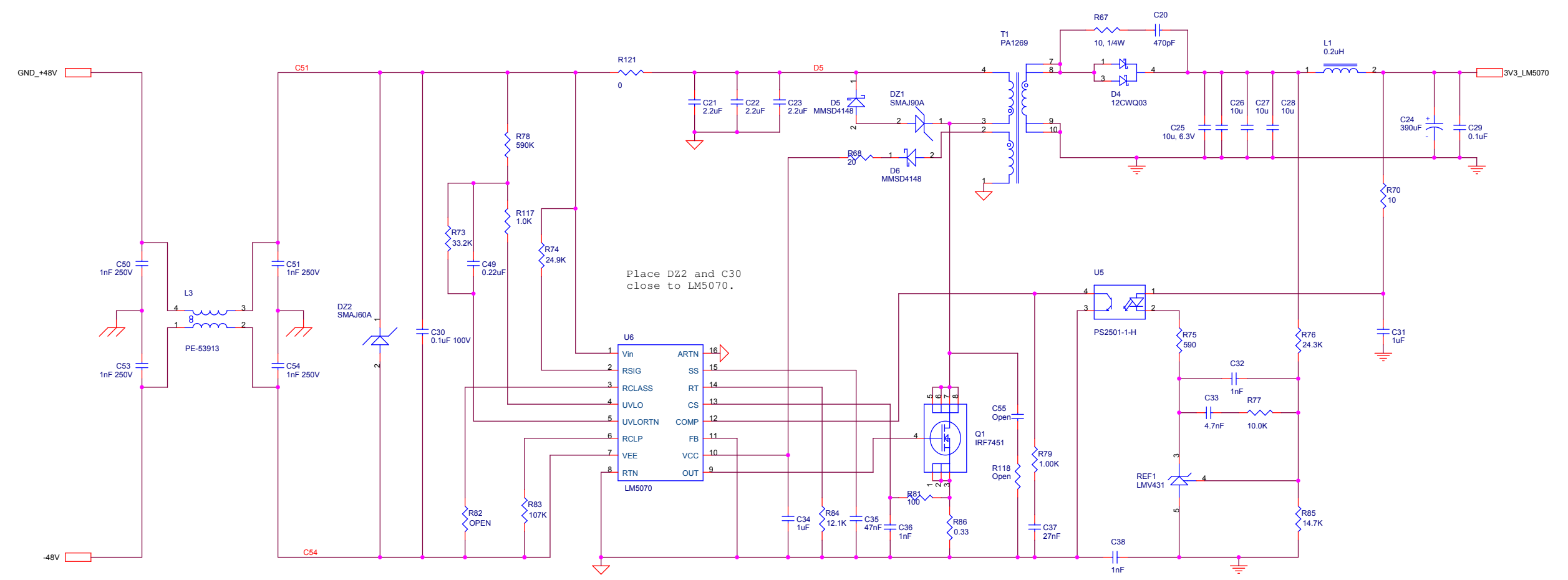
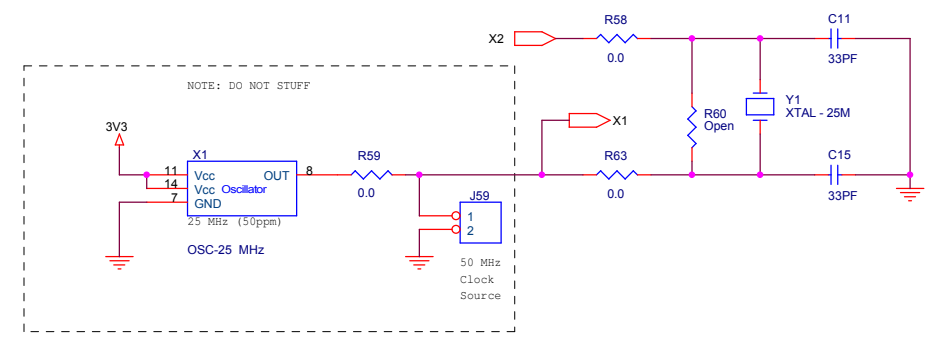
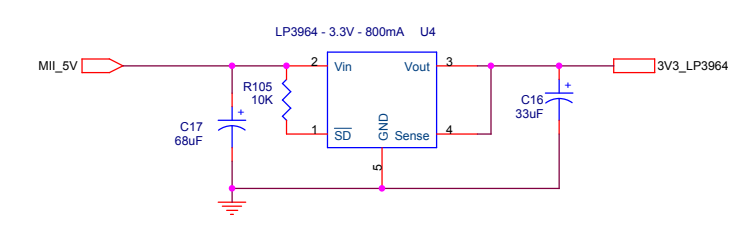
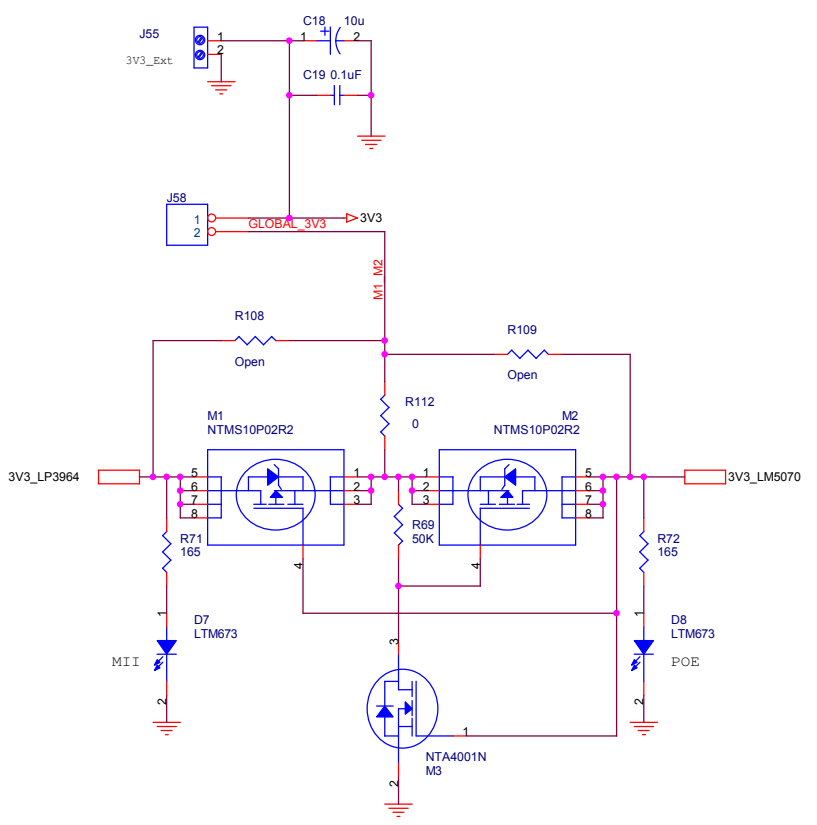
Phy Address Straps: Default is PHYAD0 = 1

J24	J25	Address
0	0	1
1	0	3
1	1	7
etc.		



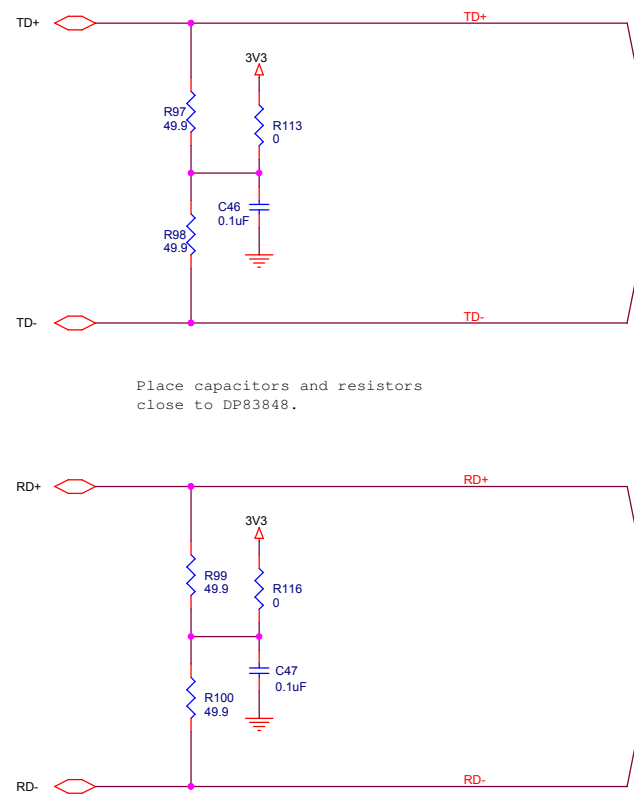
Auto-Negotiation Straps

AN0	AN1	AN_EN	Description
0	0	0	10Mbps HD Force
1	0	0	10Mbps FD Force
0	1	0	100Mbps HD Force
1	1	0	100Mbps FD Force
0	0	1	10Mbps H/FD Advertised
1	0	1	100Mbps H/FD Advertised
0	1	1	10/100Mbps HD Advertised
1	1	1	10/100Mbps H/FD Advertised (default)

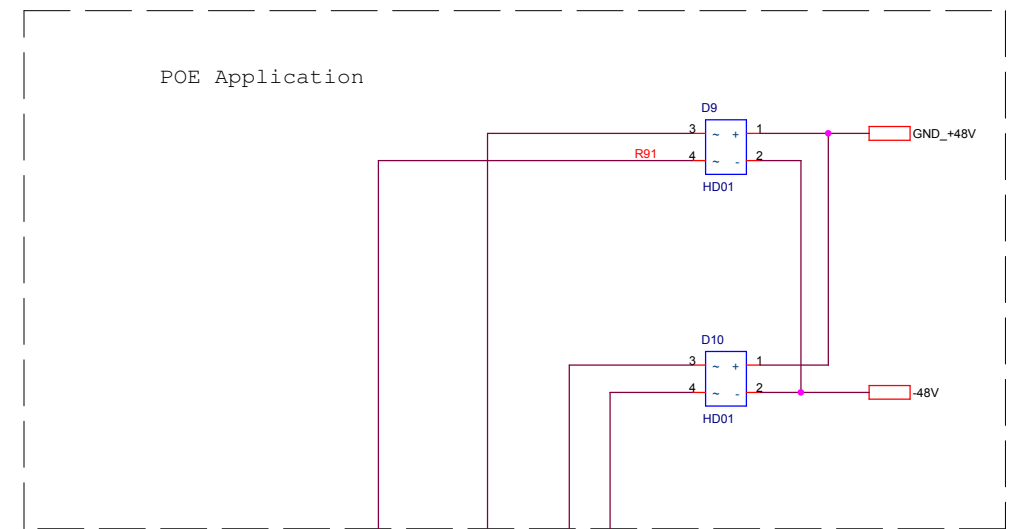


Note: Void Power and Ground planes underneath the POE circuit.

Title		DP83848 AspenPhy Demo II - Power & Clock	
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C	870012505-100	B	
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Place capacitors and resistors close to DP83848.



POE Application

Place jumpers, capacitors close to the transformer center taps.

Place these resistors close to TXC_S, RXC_S, NC1- NC4 traces. Do Not Stuff.

Note: Void Power and Ground planes underneath the transformer.

Remove R101-R104 when R91-R94 (0 ohm values) are used.

Note: Things are implemented to improve EMI.
 - Connect only one mounting hole to Chassis Ground.
 - Add capacitive coupling networks, C56 & C57 and C58 & C59, on either side of the RJ-45 connector.

Title		
DP83848 AspenPhy Demo II - TP_IF		
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C	870012505-100	B
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