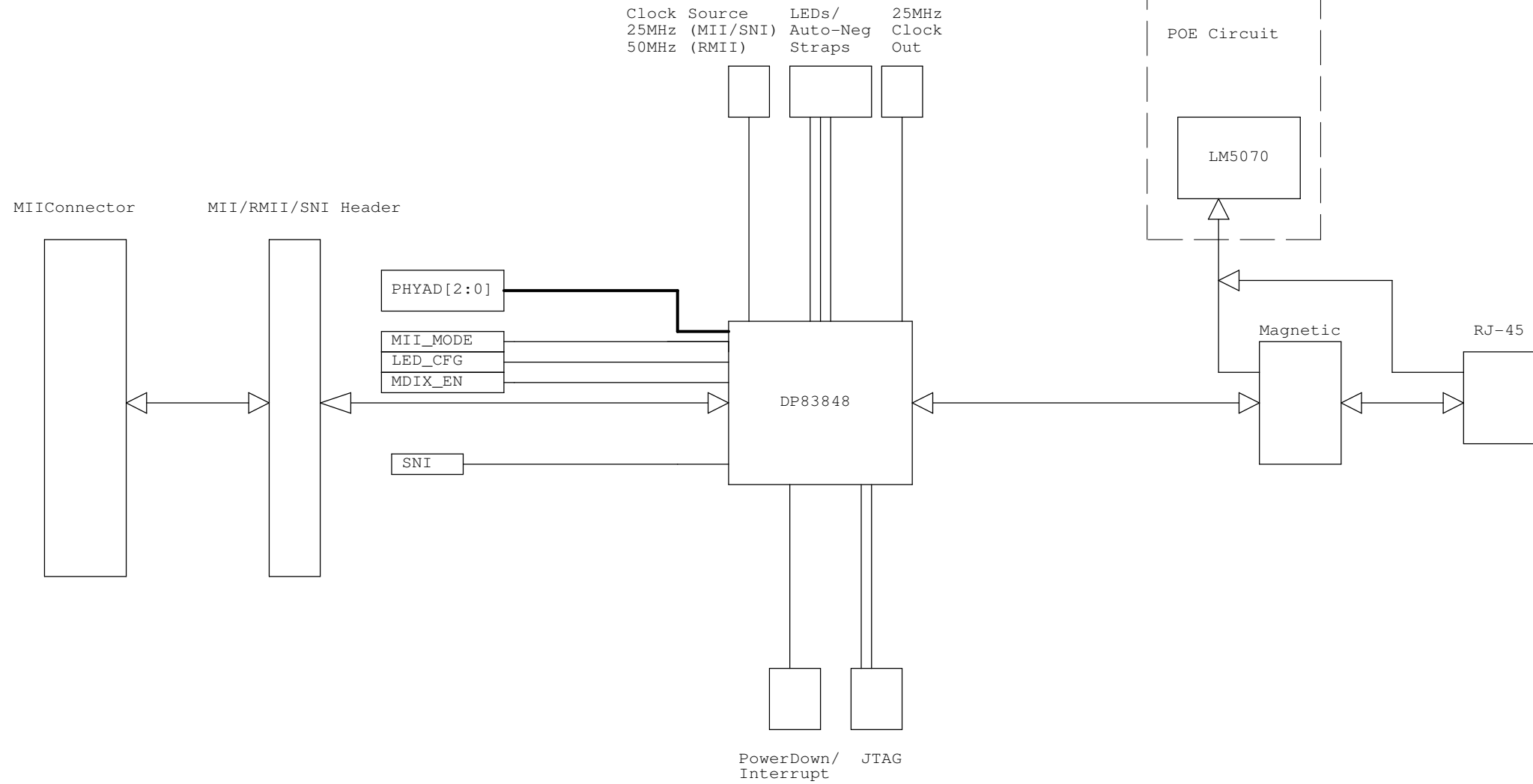
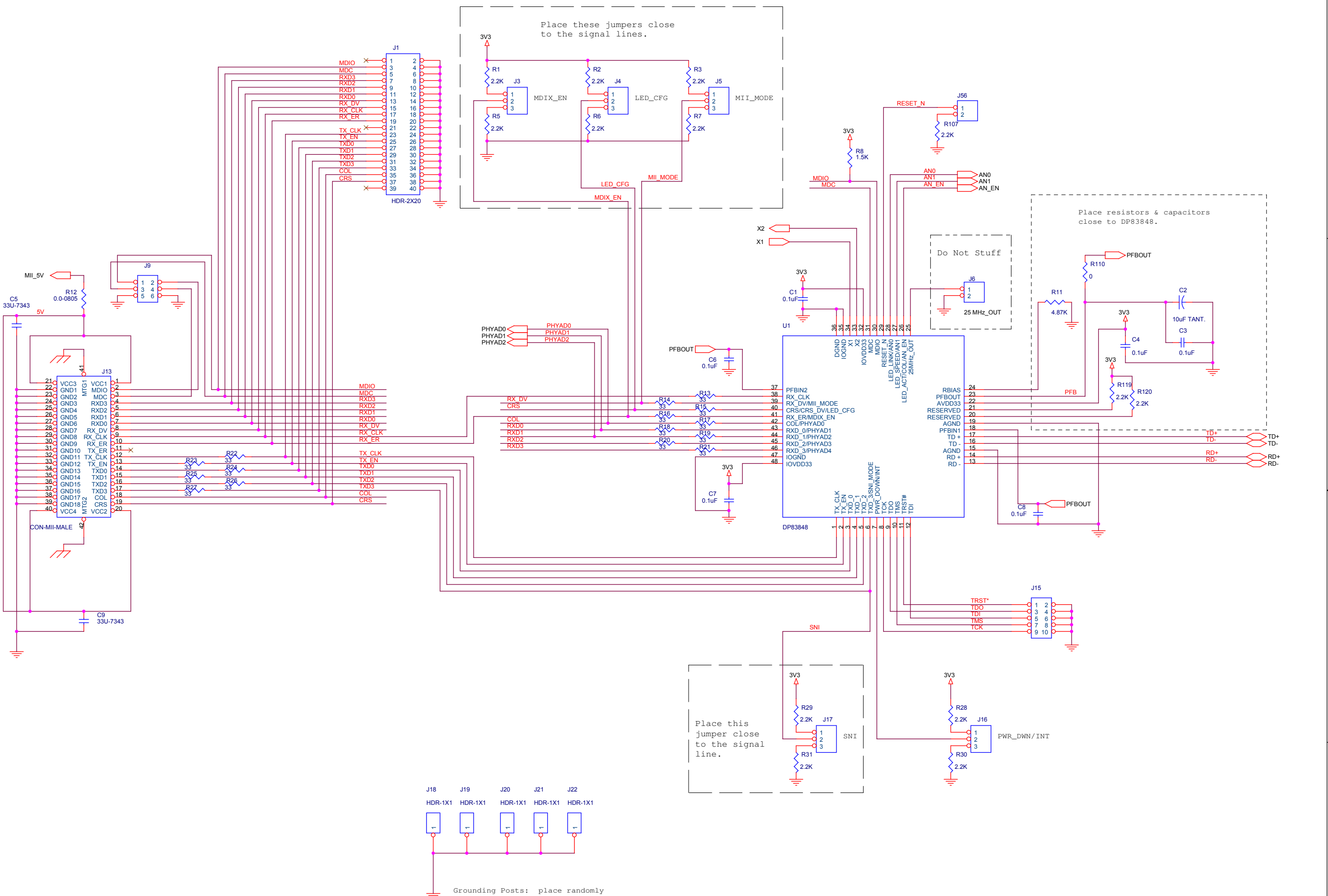


These schematics are provided for reference only. For any designs based on these schematics always contact National Semiconductor Corporation BEFORE initiating PCB manufacturing and ask for your design to be reviewed. Copyright (c) 2005 National Semiconductor Corporation. All Rights Reserved. Unpublished rights reserved under the copyright laws of the United States of America, other countries and international treaties. These schematics are provided without fee. Permission to use, copy, store, modify, disclose, transmit or distribute the schematics is granted, provided that this copyright notice must appear in any copy, modification, disclosure, transmission or distribution of the schematics. National Semiconductor Corporation retains all ownership, copyright, trade secret and proprietary rights in the schematics. THESE SCHEMATICS HAVE BEEN PROVIDED "AS IS", WITHOUT EXPRESS OR IMPLIED WARRANTY INCLUDING, WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND NON-INFRINGEMENT.

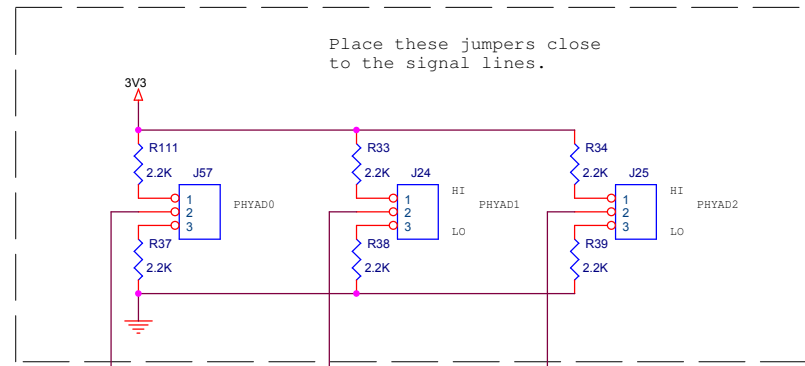
Revisions note:
 Rev A: Initial release.
 Rev A2:
 - Replaced L2 with R121.
 - Replaced C11 and C15 with 33 pF.
 - Added note for EMI related on TP_IF page.



Title		
DP83848 AspenPhy Demo II - Cover		
Size	Document Number	Rev
C	870012505-100	A2
Date:	Thursday, August 11, 2005	Sheet 1 of 5

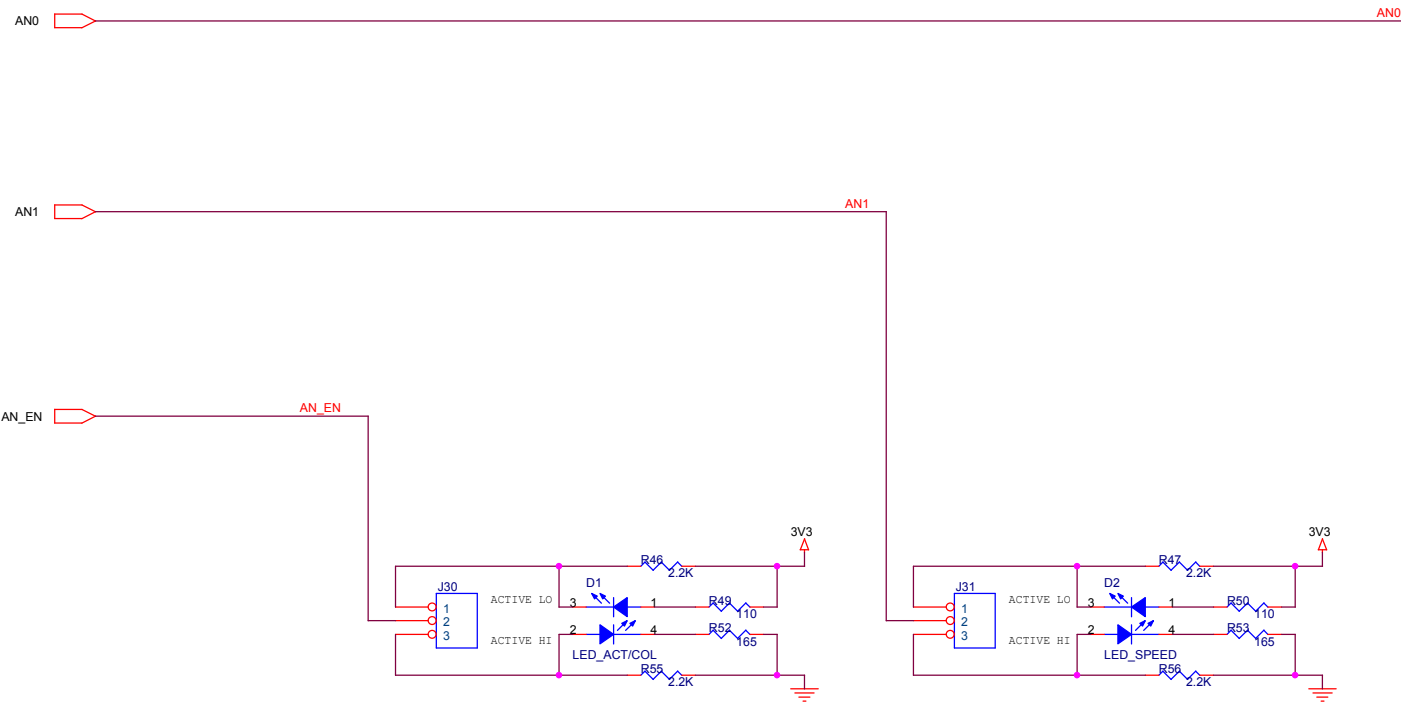
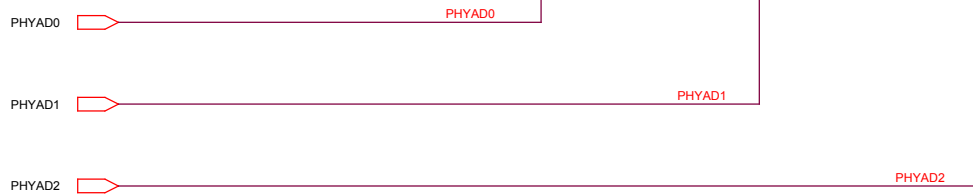


Title		
DP83848 AspenPhy Demo II - Ethernet Phy Page		
Size	Document Number	Rev
C	870012505-100	A2
Date:	Thursday, August 11, 2005	Sheet 2 of 5



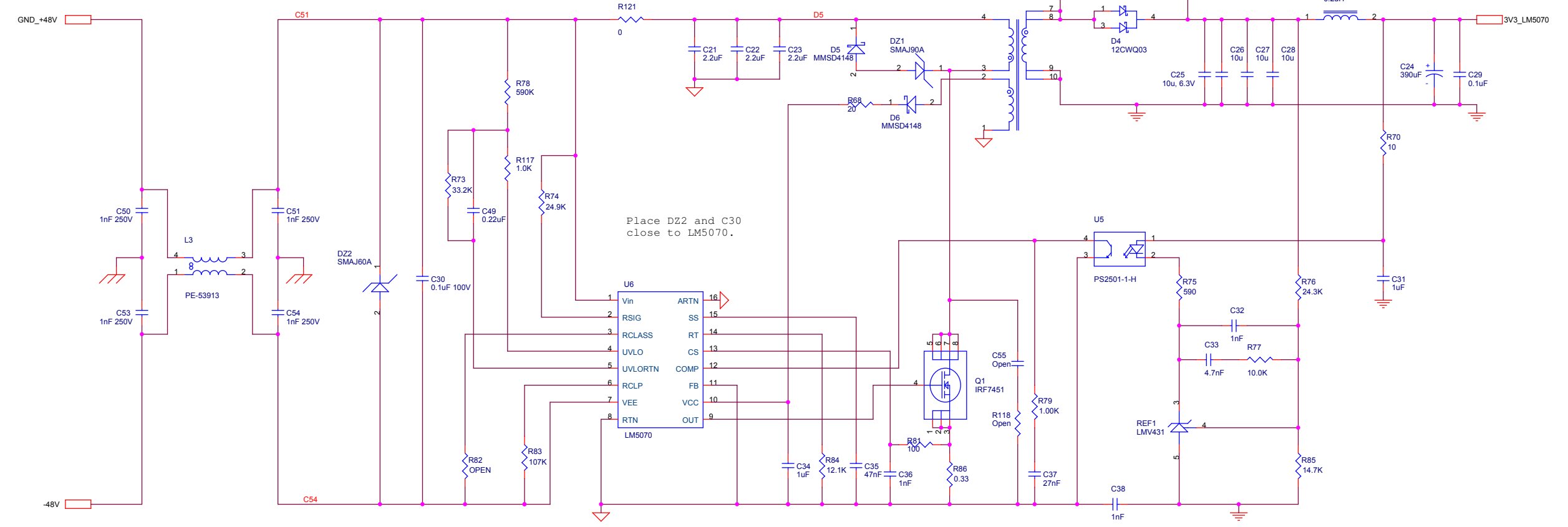
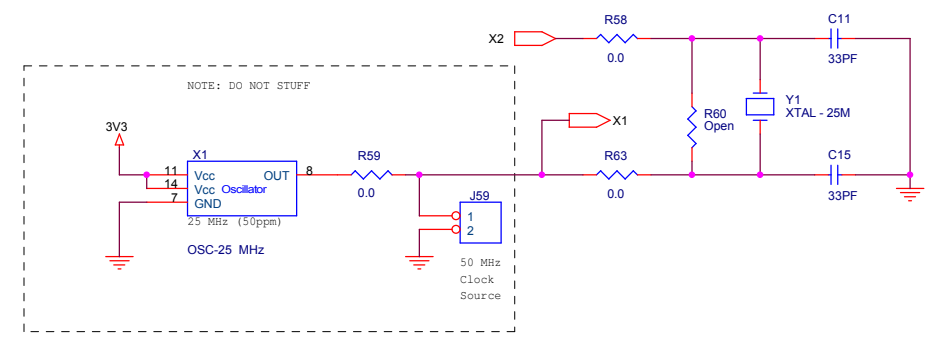
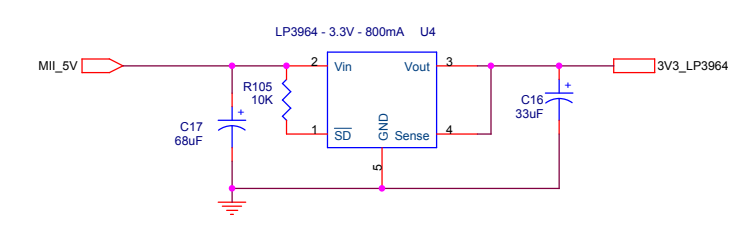
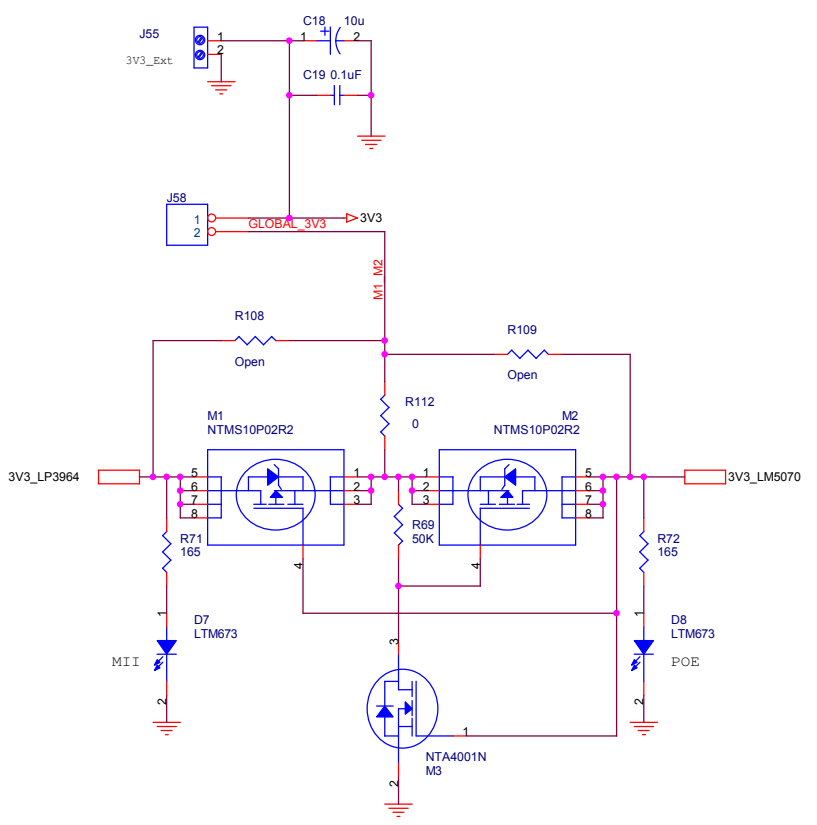
Phy Address Straps: Default is PHYAD0 = 1

J24	J25	Address
0	0	1
1	0	3
1	1	7
etc.		



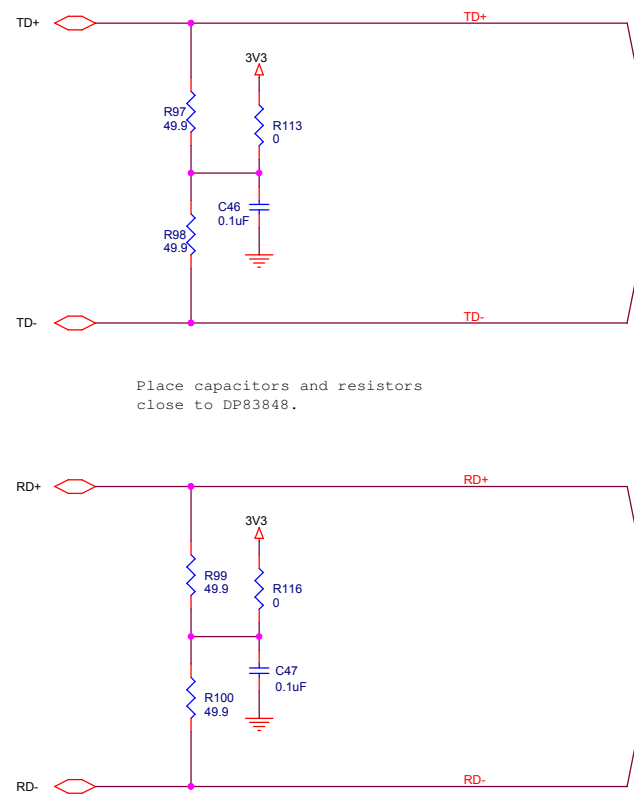
Auto-Negotiation Straps

AN0	AN1	AN_EN	Description
0	0	0	10Mbps HD Force
1	0	0	10Mbps FD Force
0	1	0	100Mbps HD Force
1	1	0	100Mbps FD Force
0	0	1	10Mbps H/FD Advertised
1	0	1	100Mbps H/FD Advertised
0	1	1	10/100Mbps HD Advertised
1	1	1	10/100Mbps H/FD Advertised (default)

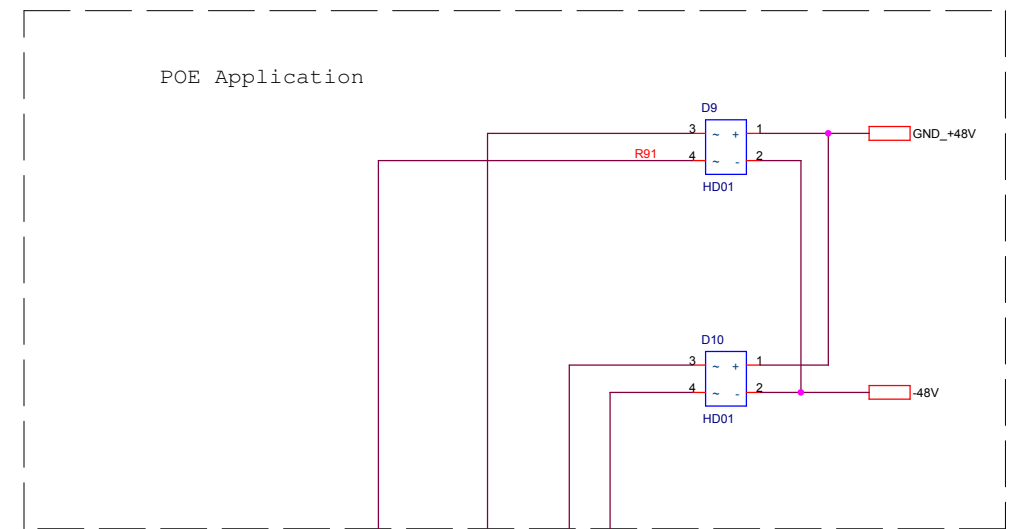


Note: Void Power and Ground planes underneath the POE circuit.

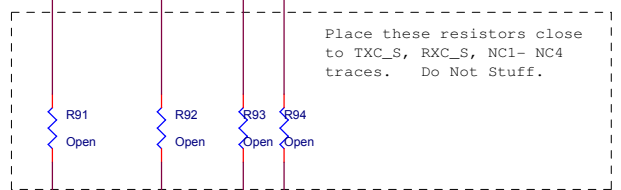
Title		DP83848 AspenPhy Demo II - Power & Clock	
Size	Document Number	Rev	
C	870012505-100	A2	
Date:	Thursday, August 11, 2005	Sheet	4 of 5



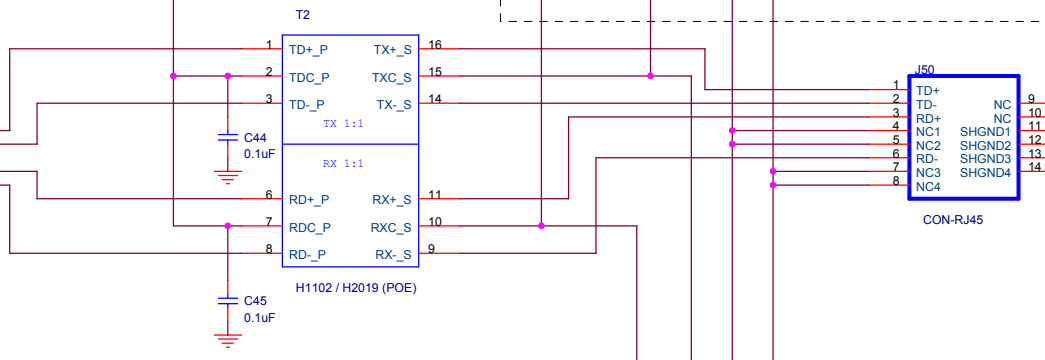
Place capacitors and resistors close to DP83848.



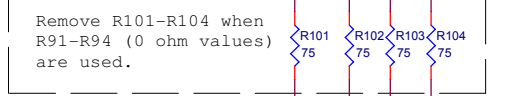
Place jumpers, capacitors close to the transformer center taps.



Place these resistors close to TXC_S, RXC_S, NC1- NC4 traces. Do Not Stuff.



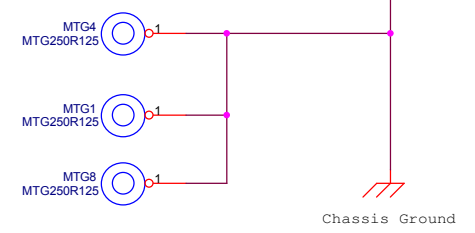
Note: Void Power and Ground planes underneath the transformer.



Remove R101-R104 when R91-R94 (0 ohm values) are used.

Note for further improvement on EMI:

- Allow only 1 mounting point connects to chassis ground.
- Add two capacitive coupling networks between chassis and common ground. Coupling consists of two caps, .1 uF and .001 uF. Place this on either side of RJ-45.
- See rev B for the implementation.



Title		
DP83848 AspenPhy Demo II - TP_IF		
Size	Document Number	Rev
C	870012505-100	A2
Date:	Thursday, August 11, 2005	Sheet 5 of 5