

COP8FLASH

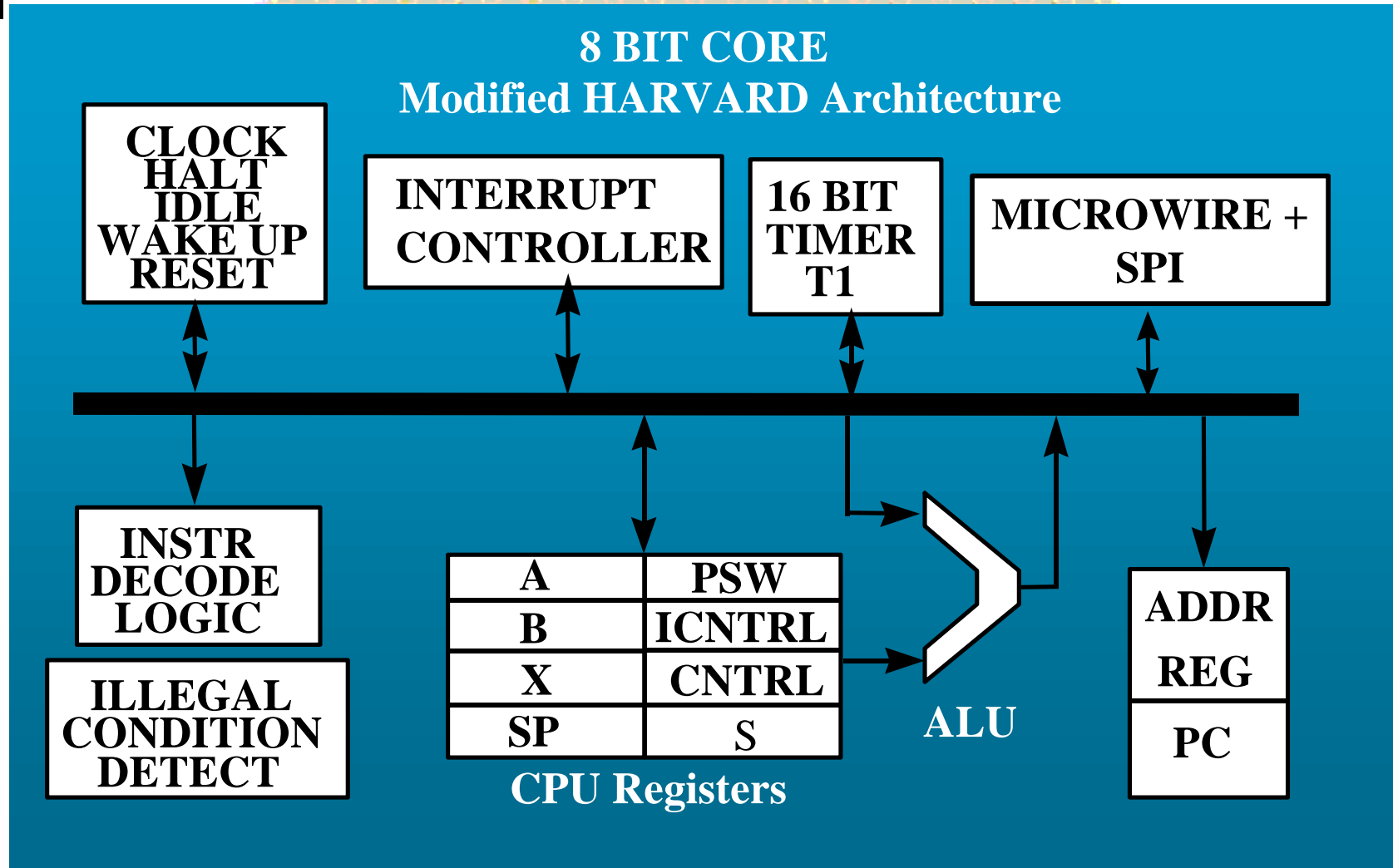
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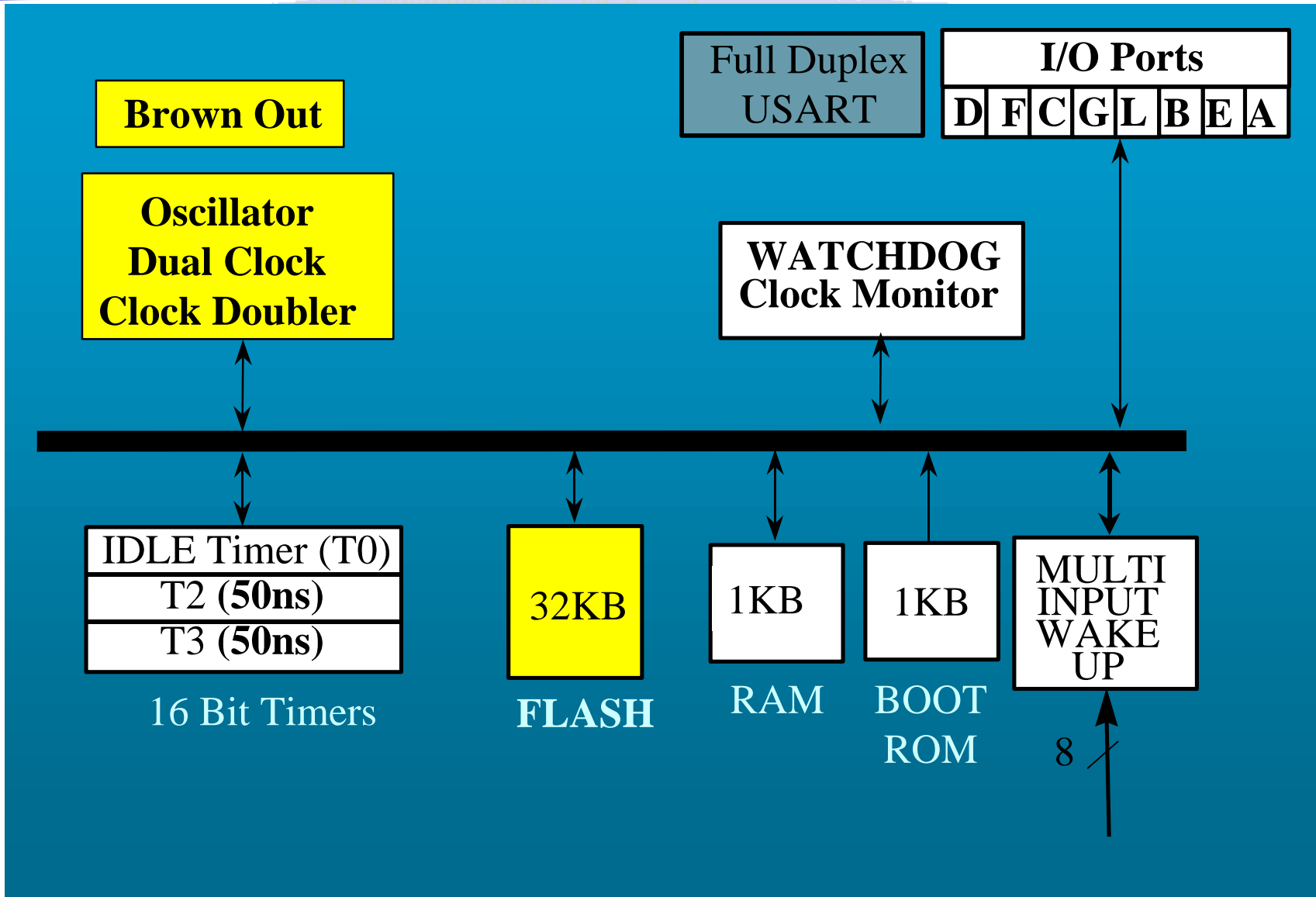
Agenda

- COP8SBR block diagram
- Memory Organization
 - SRAM
 - FLASH program memory
 - Boot ROM Organization
 - Zero Cost EEPROM (Virtual EEPROM)
 - Option Register
 - FLEX Bit
- Clock Doubler
- Power Save Modes
 - HALT, IDLE
- Multi-Input-Wake-Up (MIWU)
- Dual Clock Oscillator
- Timers
- Serial Interfaces (USART, MICROWIRE™)
- Brown-Out WATCHDOG™
- I/O Ports
- Higher Integration COP8FLASH devices
 - COP8CBR
 - 10-bit SAR A/D
 - COP8AME
 - Op-Amps

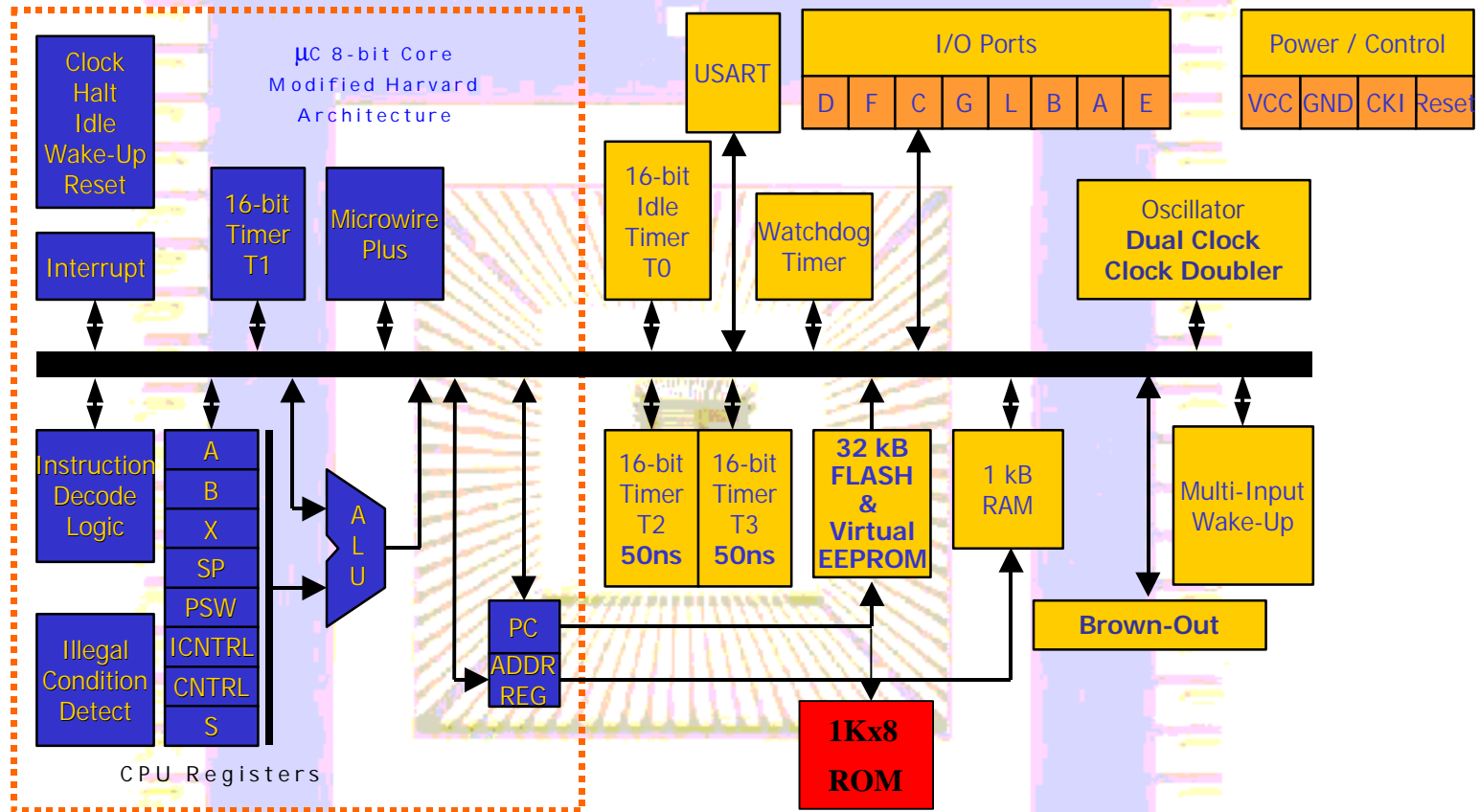
ARCHITECTURE : COP8 CORE



COP8SBR PERIPHERALS

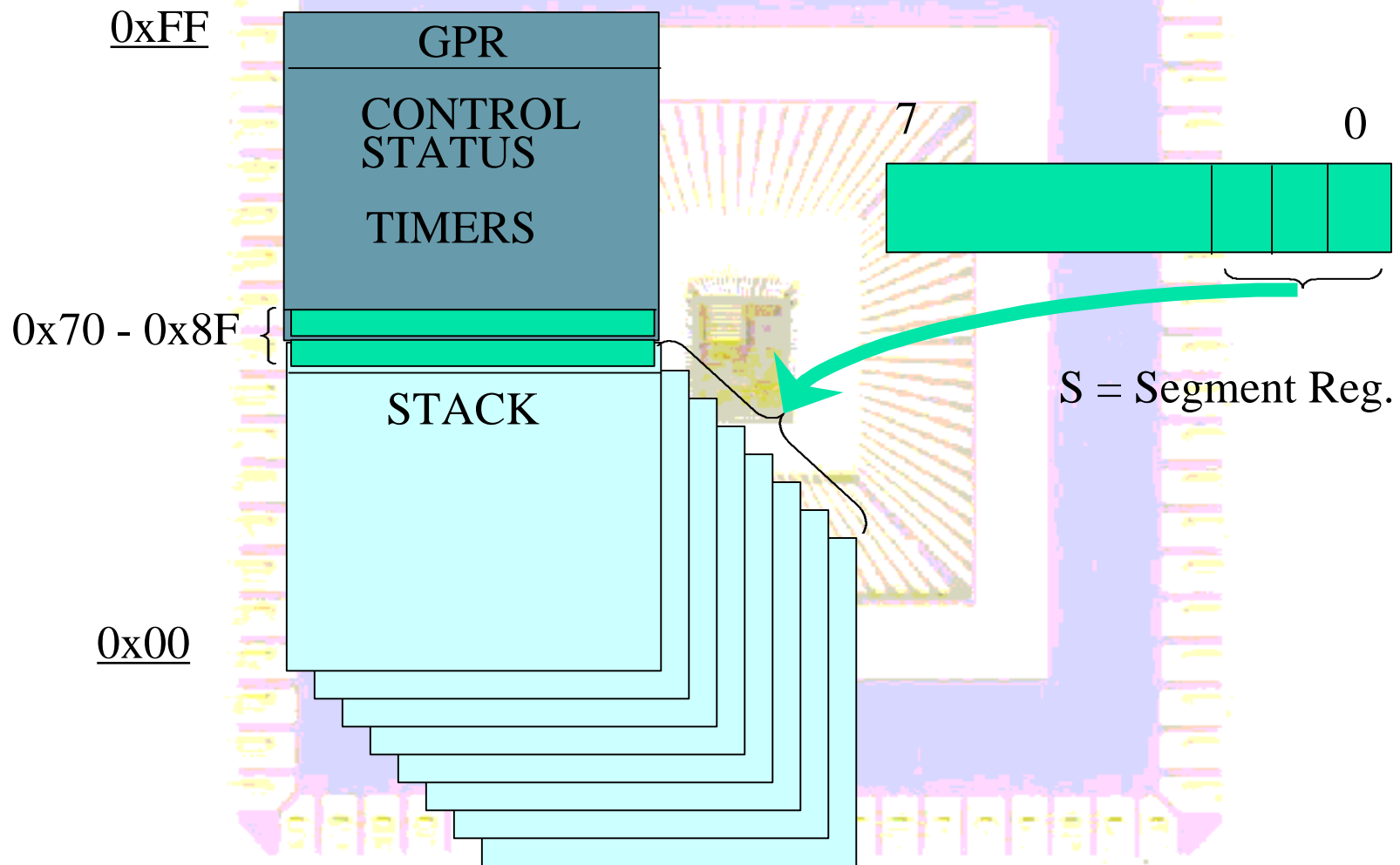


COP8SBR Block Diagram

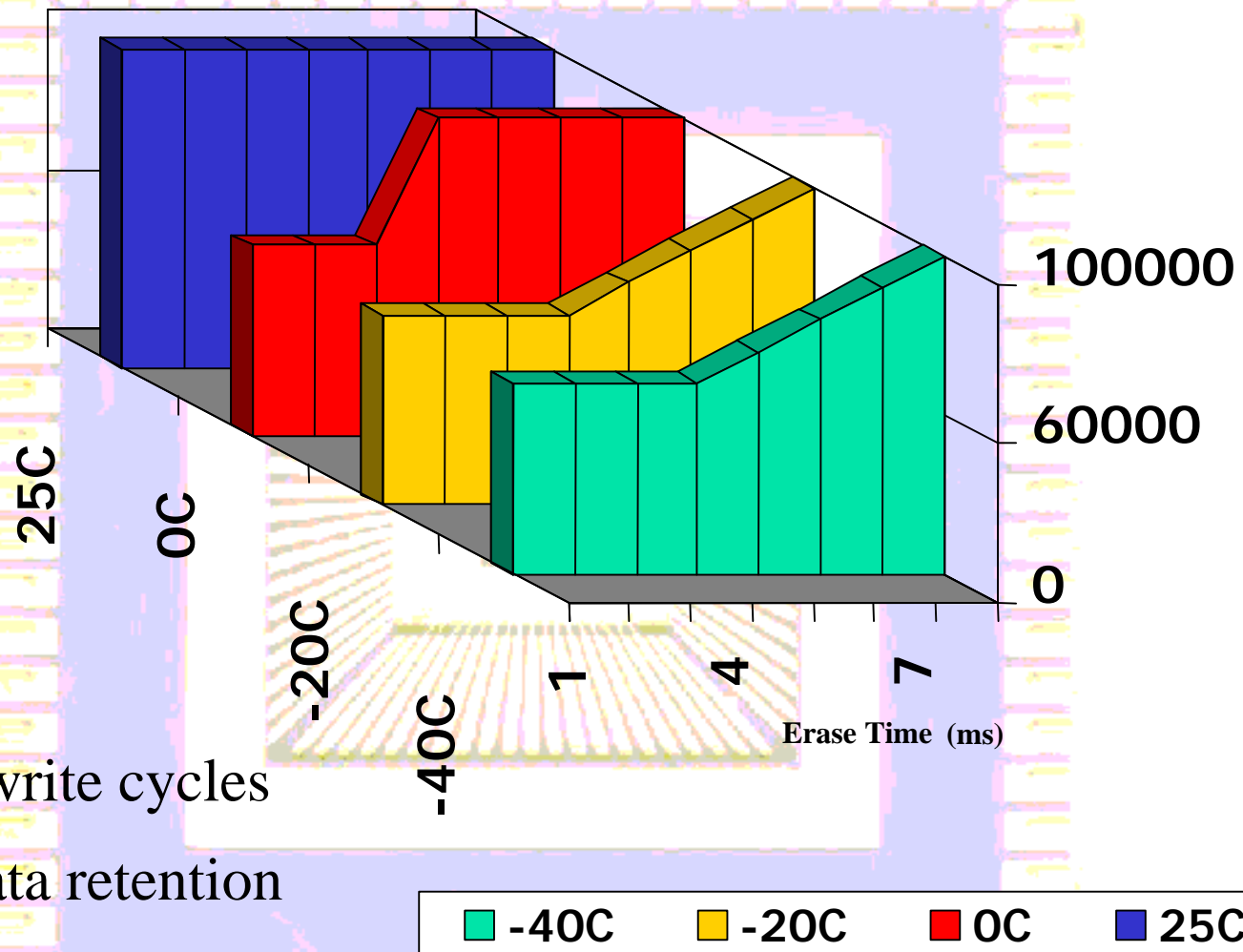


SRAM ORGANIZATION

- Bank Switched Memory

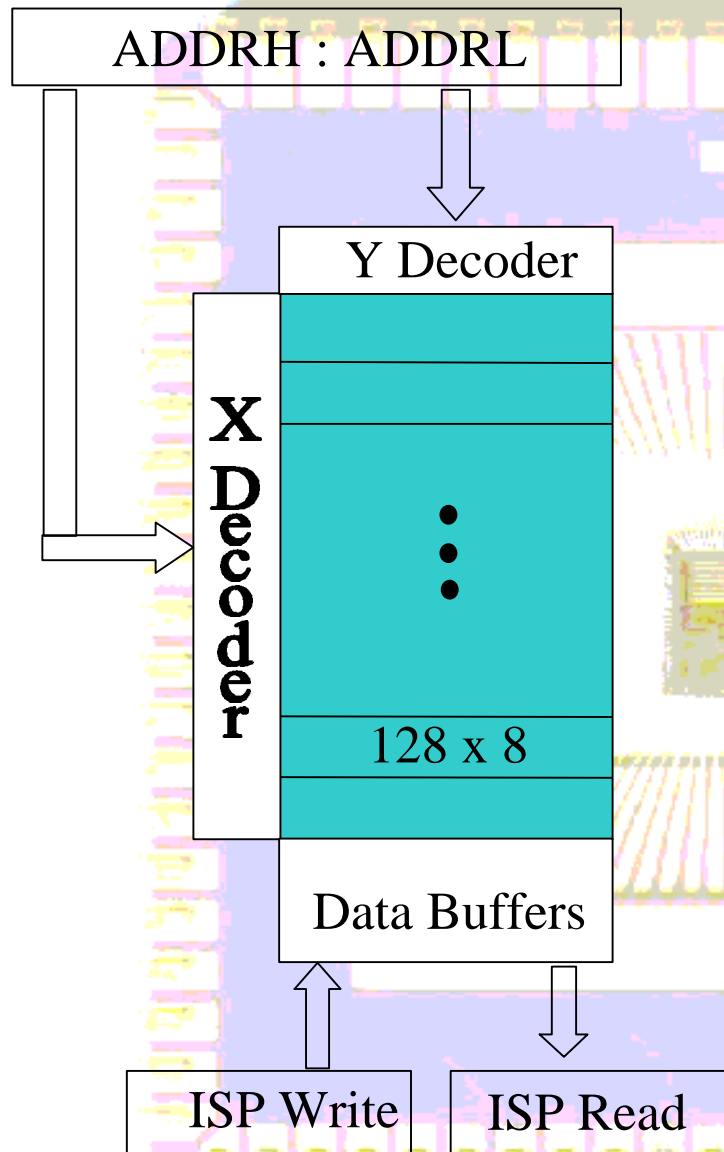


COP8FLASH MEMORY ENDURANCE



- 100k erase/write cycles
- 100 years data retention
- up to 125C operation

32k FLASH Memory Block



■ Features:

- Organized in 128 x 8 Blocks
- Internal High Voltage
- Self Timed, CPU clock independent programming
- Programmable via μ Wire, user ISP code, emulator or external, parallel 3rd party programmers
- Absolutely no external hardware, high voltage or Reset signals required.

COP8FLASH Boot ROM

■ Features:

- Factory default MICROWIRE ISP support
- Support for User's own FLASH based ISP routines via subroutine calls
- KEY Lock Register for added safety
- Zero Cost EEPROM support
 - Byte and block data transfers between RAM and FLASH
- Emulation support

ROM

μWire

ISP

Support for
User's ISP
routines

Emulation
Support

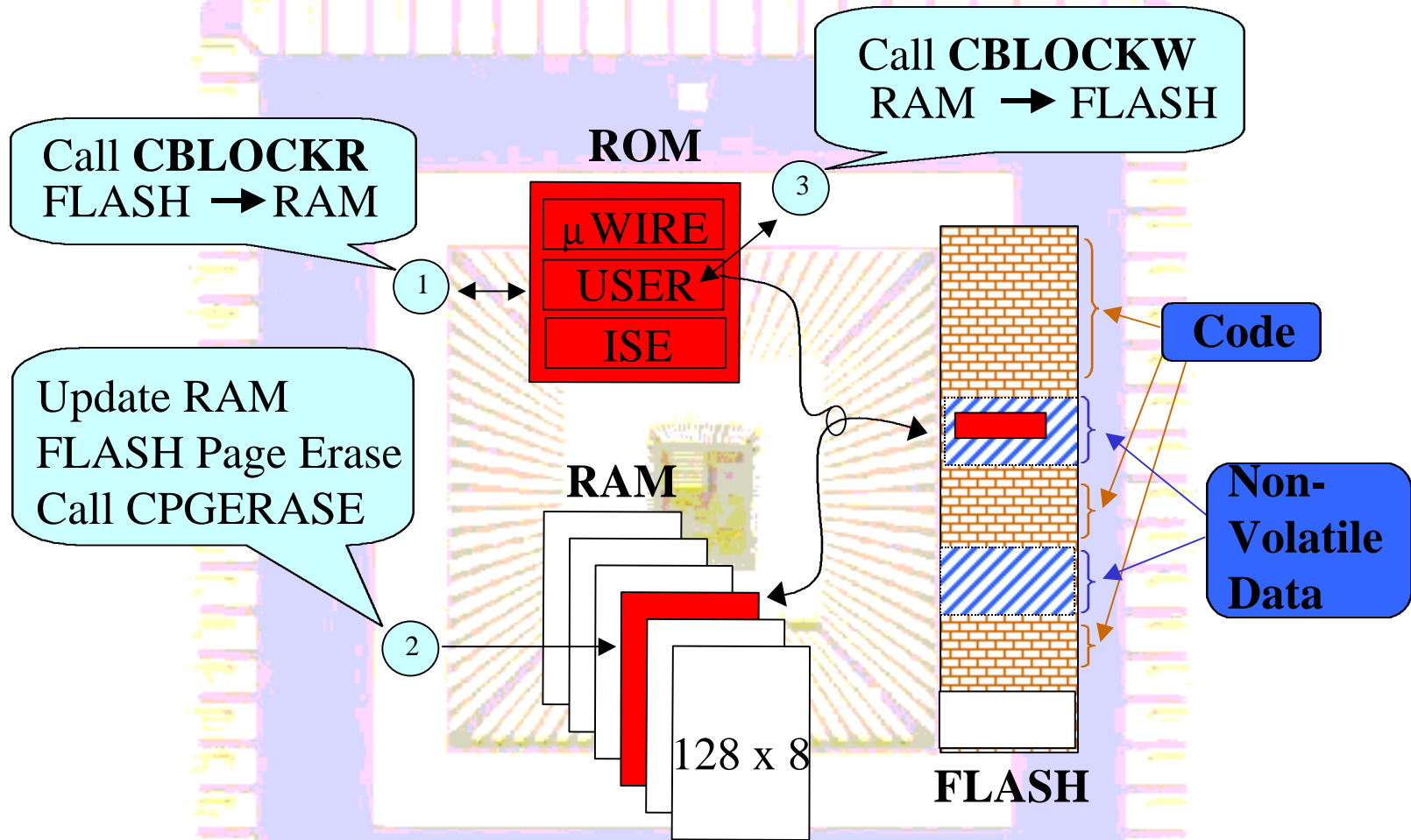
COP8FLASH Zero Cost EEPROM

- Zero Cost EEPROM
 - User can dedicate any amount of FLASH program memory as non-volatile data memory
 - single byte read/write and multiple byte read/write operations are supported through user callable Boot ROM routines
- Benefits
 - Eliminate external EEPROM or battery backed SRAM
 - Variable size EEPROM (up to entire FLASH memory available for EEPROM use)
 - Best of all: **It's free**

COP8FLASH Zero Cost EEPROM

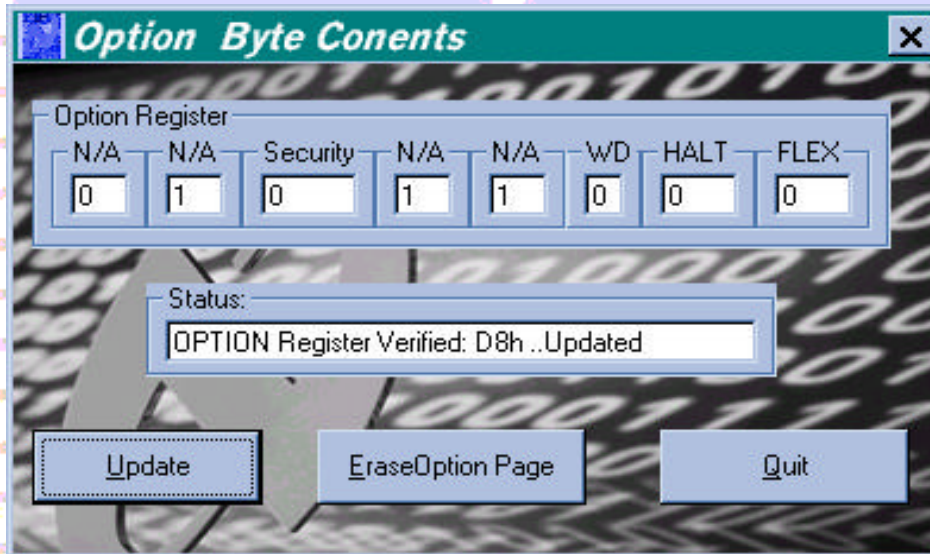
- 64/128 byte page has to be saved to RAM (1 subroutine call to ISP code).
 - COP8FLASH generous RAM sizes provide ample space for mirroring Virtual EEPROM data in RAM
- FLASH page is then erased (1ms independent of microcontroller clock)
- a single byte or multiple bytes can be written back at the user's convenience.
 - Writing a single byte (@10MHz) takes approx. 140us. Multiple bytes are slightly faster (approx. 120us/byte)
- During the time of a write to FLASH the microcontroller is blocked from executing code out of program memory.
 - Nevertheless any interrupts occurring are latched and can be processed after the write has been completed

Zero Cost E² Page Updates



OPTION REGISTER

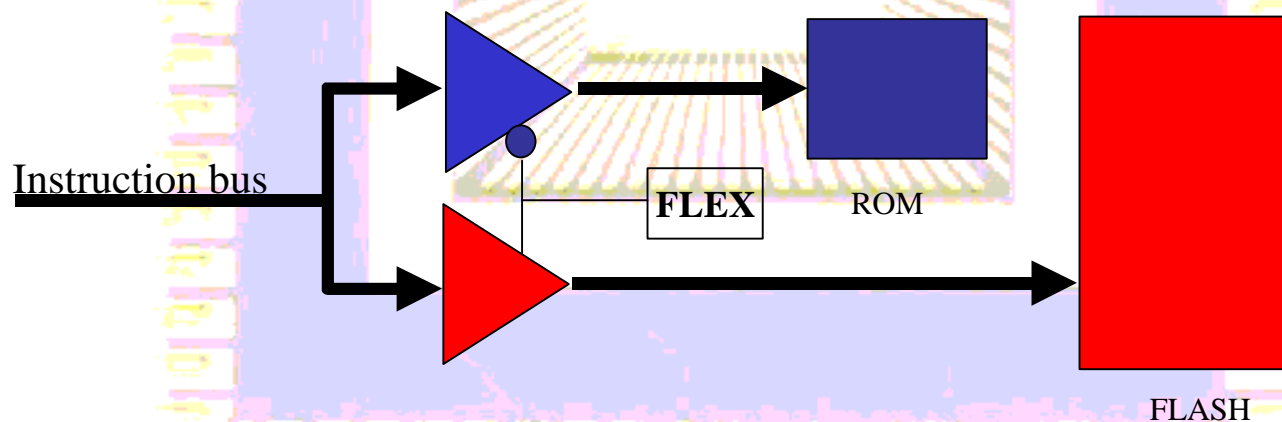
Nonvolatile Option Register (0x7fff) - (Default=0)



- Bit.0 FLEX : Execution from ROM/FLASH
- Bit.1 HALT : Disable/Enable
- Bit.2 WD : Watchdog Disable/Enable
- Bit.5 SEC : Secure Flash Memory against read/write/erase
- Bit.3/4/6/7 Reserved

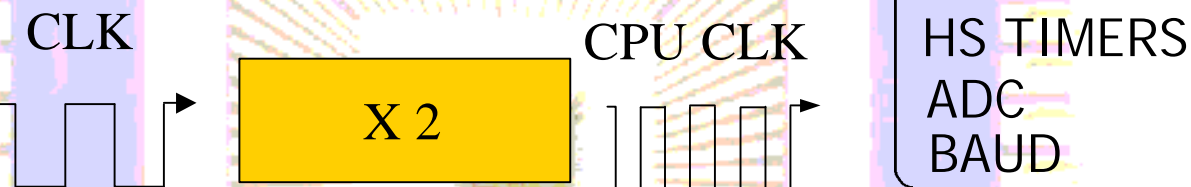
FLEX (Flash Execute) Bit

- COP8 use of FLEX bit: Upon exit from reset program is fetched:
 - FLEX = 0 BOOT ROM
 - FLEX = 1 FLASH MEMORY



COP8FLASH Clock Doubler

- Double Selected Clock Frequency
- Feeds the Core (CPU CLK)

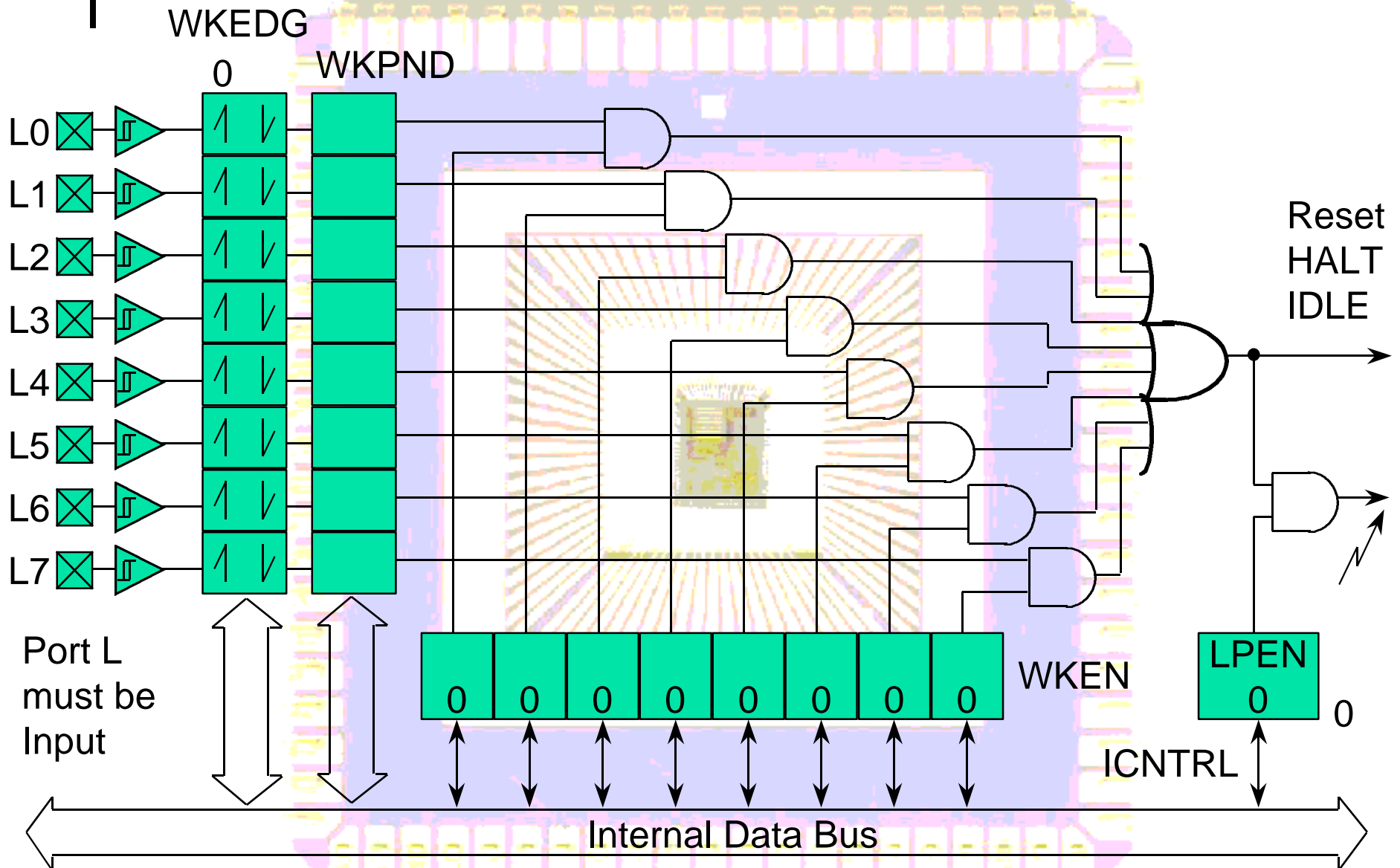


<i>CLOCK SOURCE</i>	<i>MAX CLK</i>	<i>MAX CPU CLK</i>
<i>HIGH SPEED</i>	10 MHz	20 MHz
<i>LOW SPEED</i>	32 KHz	64 KHz

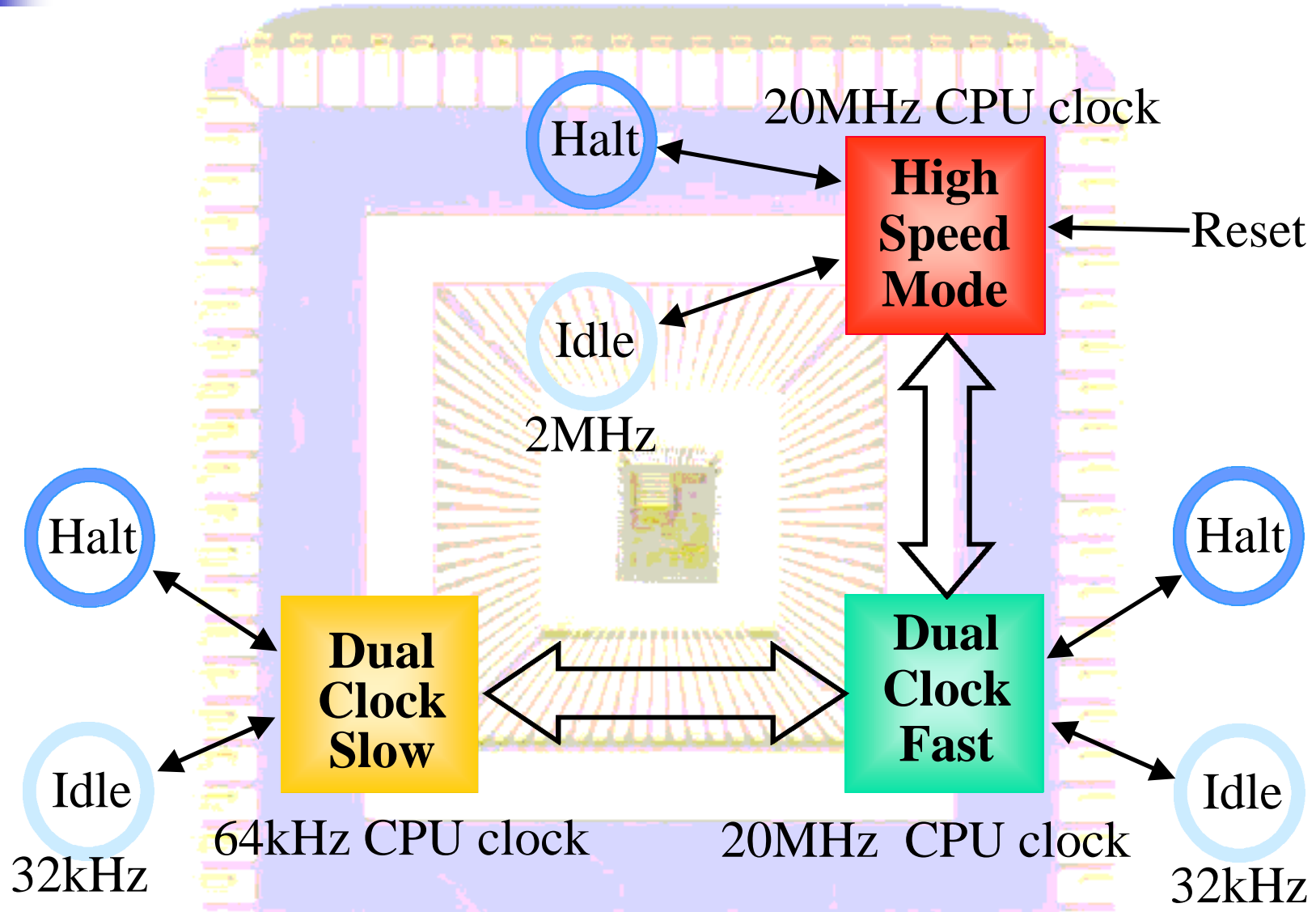
Power Save Modes

- Dual Oscillator support
- Halt Mode, high speed oscillator stopped
- Idle Mode, timer T0 and selected oscillator active
- Multi-Input Wakeup, to exit power save modes based on external events
- Operating Voltages down to 2.7V

Multi-Input Wakeup



COP8FLASH Oscillator modes



All frequency values assume 10MHz/32kHz external oscillators

COP8FLASH Clock Modes

Clock Mode	CKI	CPU CLK	T _C (μs)	T _{IDLE} (μs)	I _{CC} (mA) max./ (typ)	I _{IDLE} (mA) max./ (typ)	I _{HALT} (μA) typ.
High Speed	10MHz	20MHz	0.5	0.5	14.7	2.5	2
Dual Clock Fast	10MHz	20MHz	0.5	30.5	14.7	2.5	5
Dual Clock Slow	32.7K	64KHz	152.6	30.5	95/(50)(μA)	30/(15)(μA)	5

COP8SBR Peripherals

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COP8SBR Timers

- Timers:
 - T0 16-bit free-running Idle timer
 - T1 16-bit multifunction timer, clocked by instruction clock (500ns@10MHz oscillator)
 - T2, T3 16-bit high-speed multifunction timers, clocked at instruction clock or CPU clock (500ns/50ns)
- T1, T2, T3 Operating Modes:
 - Processor Independent PWM
 - Counter
 - Event Capture

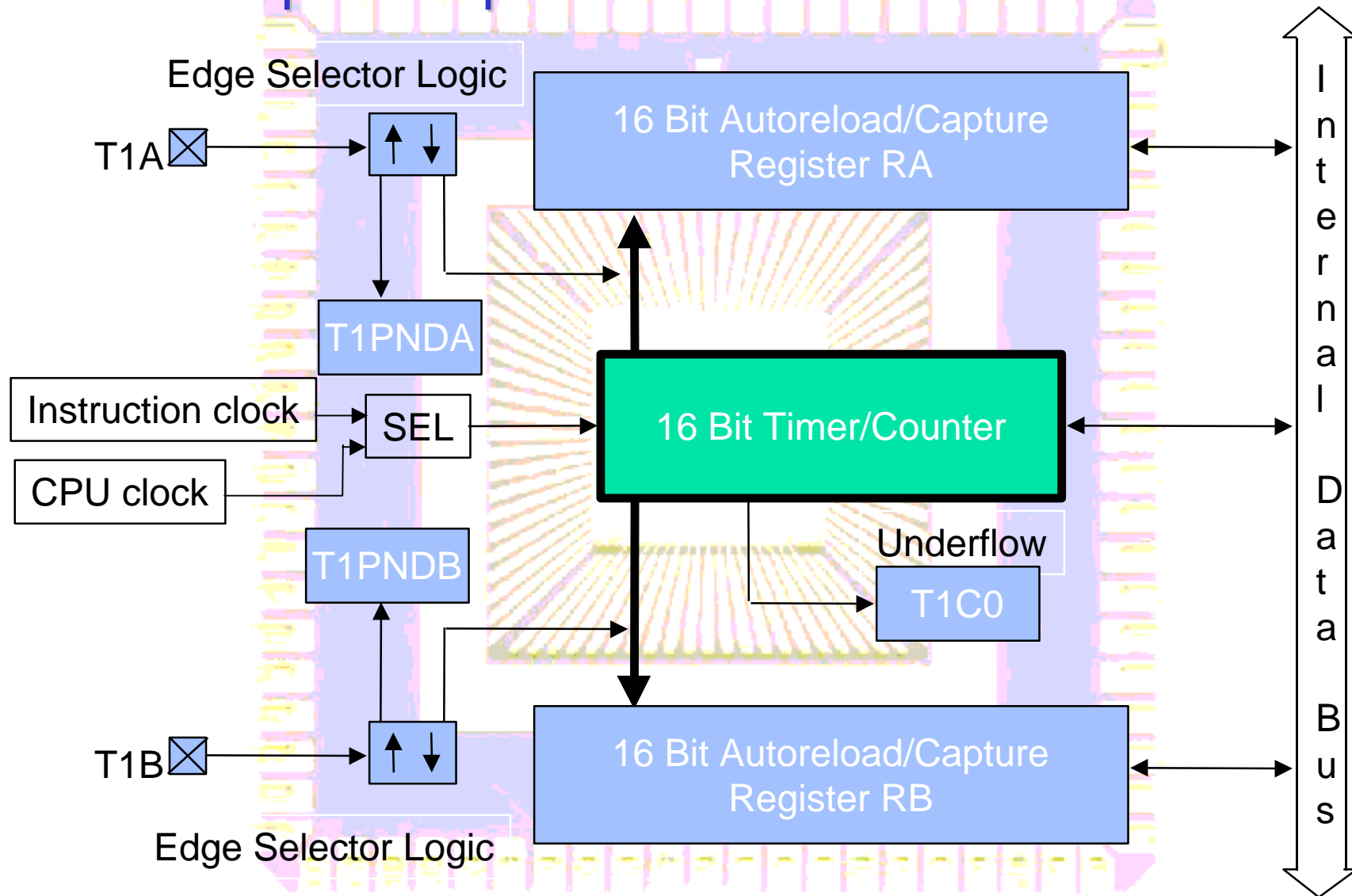
IDLE Timer T0

- Free running 16-bit timer
 - In High speed mode clocked by instruction cycle clock, in all other modes clocked by 32kHz oscillator
- Supports programmable underflow periods of 4k, 8k, 16k, 32k and 64k instruction cycles
- Underflow can generate interrupt and set a status bit
- Wake-up of the microcontroller after a pre-programmed time period from IDLE mode

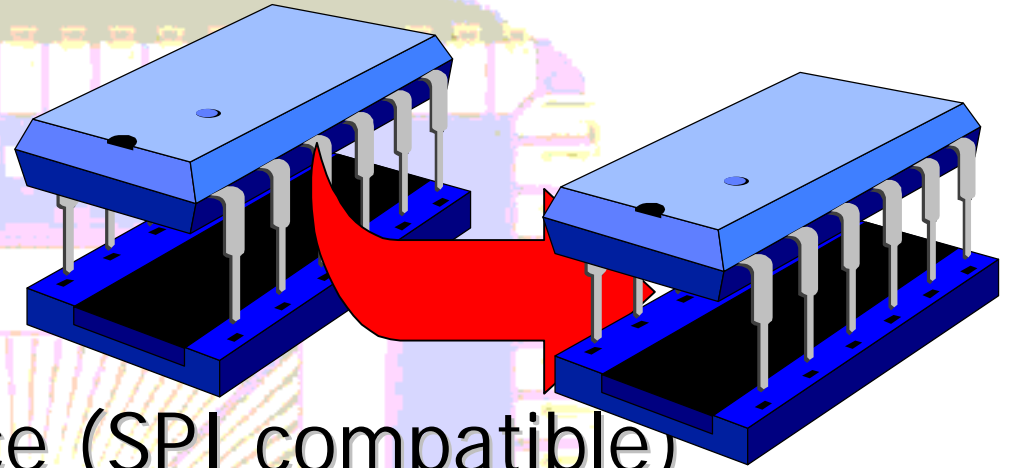


Multifunction Timer Block Diagram

Input Capture Mode

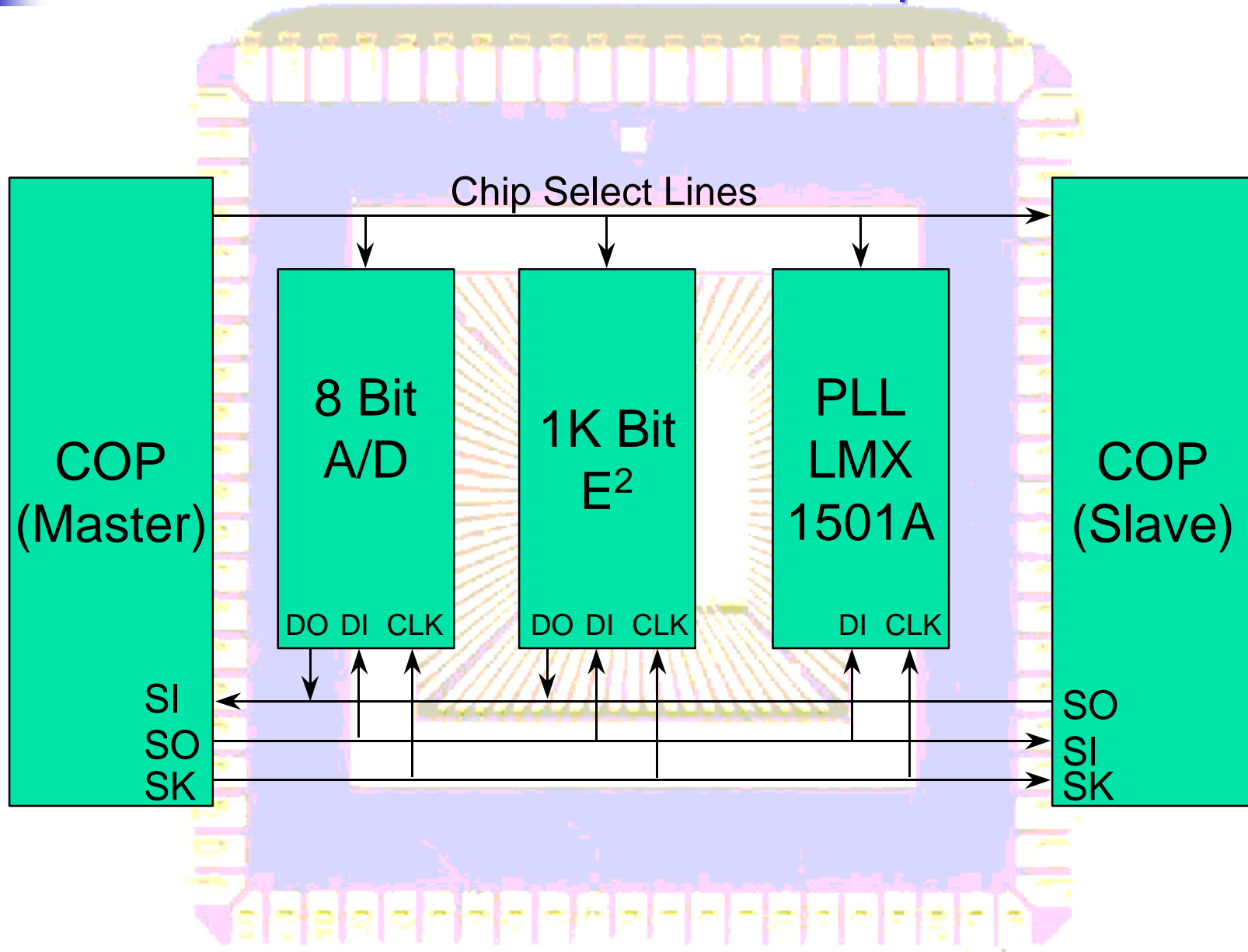


MICROWIRE/Plus™

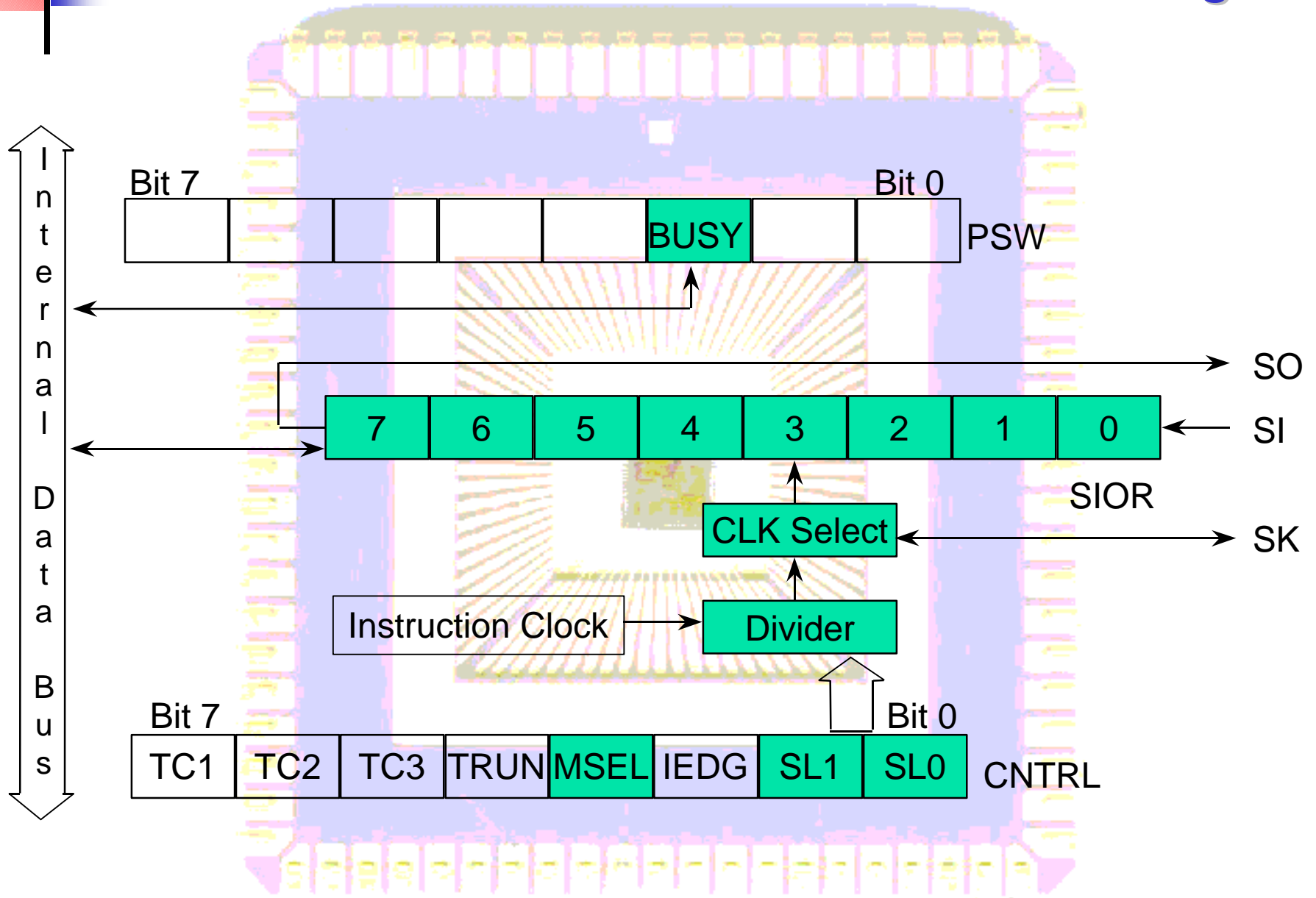


- Serial 3-wire interface (SPI compatible)
- Data rates up to 1Mbps
- Easy connection of external peripherals, like
 - USB I/F
 - EERAM
 - LCD drivers
 - National audio devices (equalizer, digital tone control, etc.)

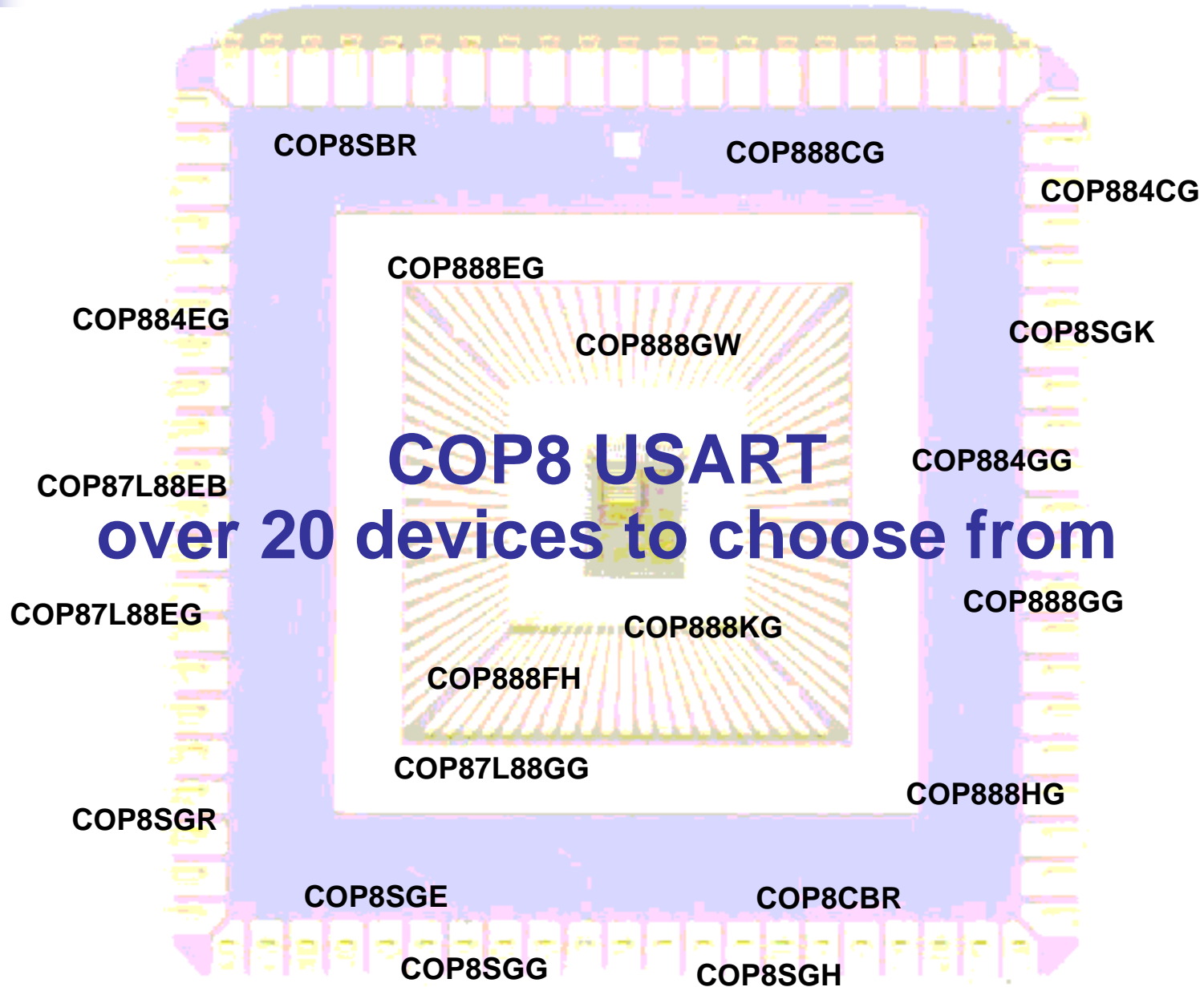
MICROWIRE/PLUS Example



MICROWIRE/PLUS Circuit Block Diagram



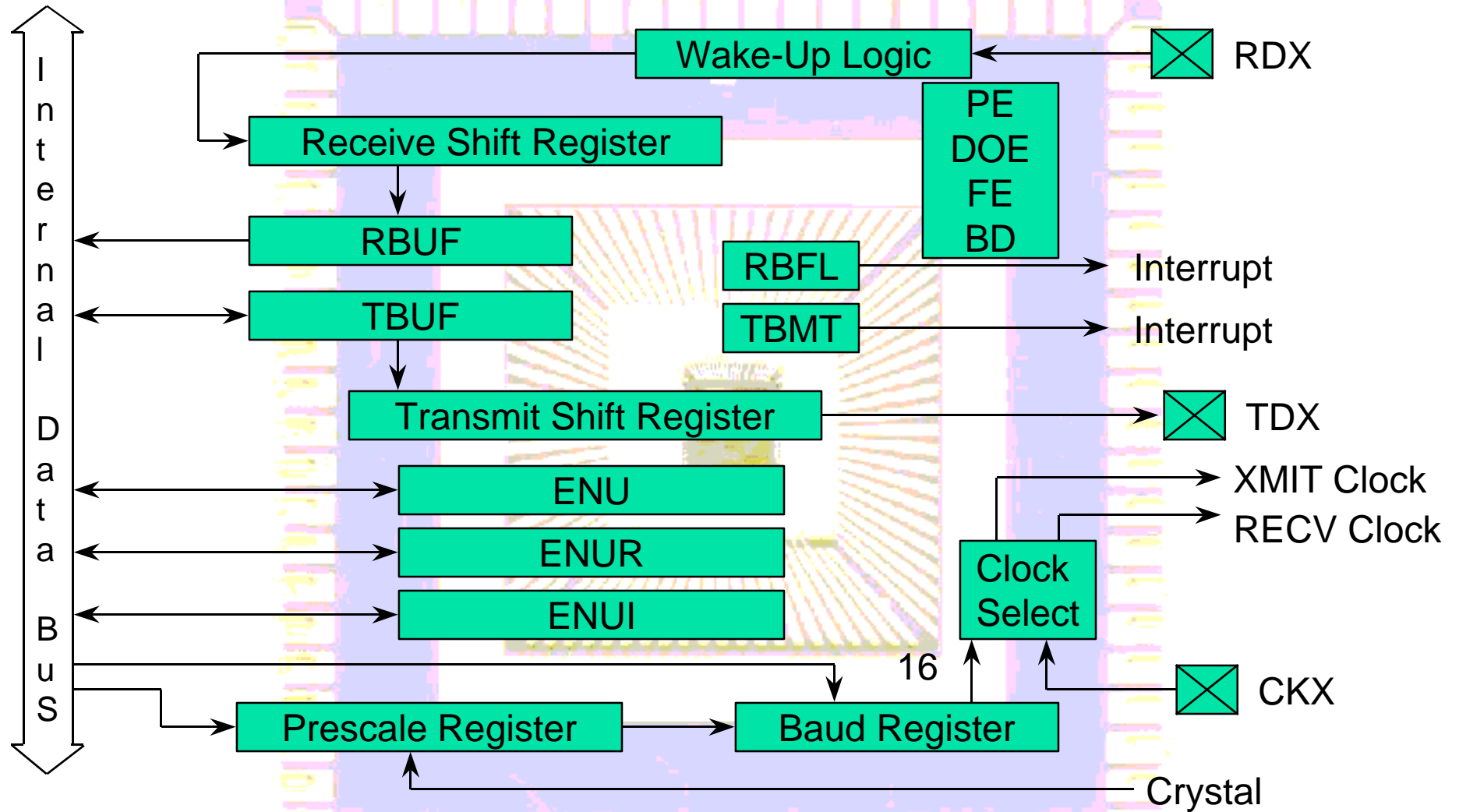
COP8 USART



COP8 USART
over 20 devices to choose from

- USART Features
 - Full Duplex
 - Fully programmable interface characteristics
 - 7, 8, or 9 bit word length
 - Even, Odd, Mark, Space, or No Parity
 - 1, or 2 Stop Bits
 - Two interrupt sources with independent vectors
 - Independent clock inputs for Tx and Rx
 - Asynchronous or Synchronous operation
 - Break Detection and Generation
 - Flexible Baud Rate Generator

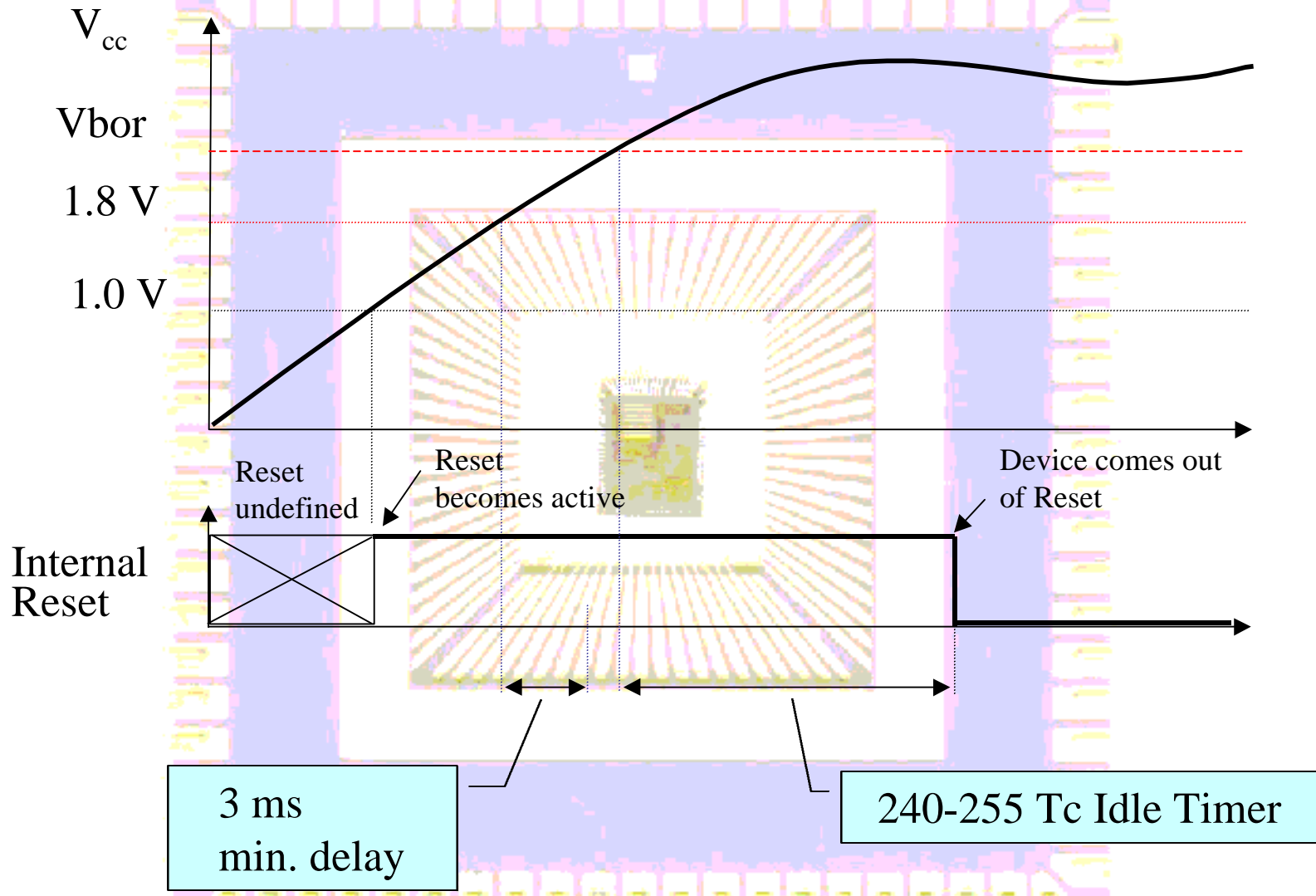
USART Block Diagram



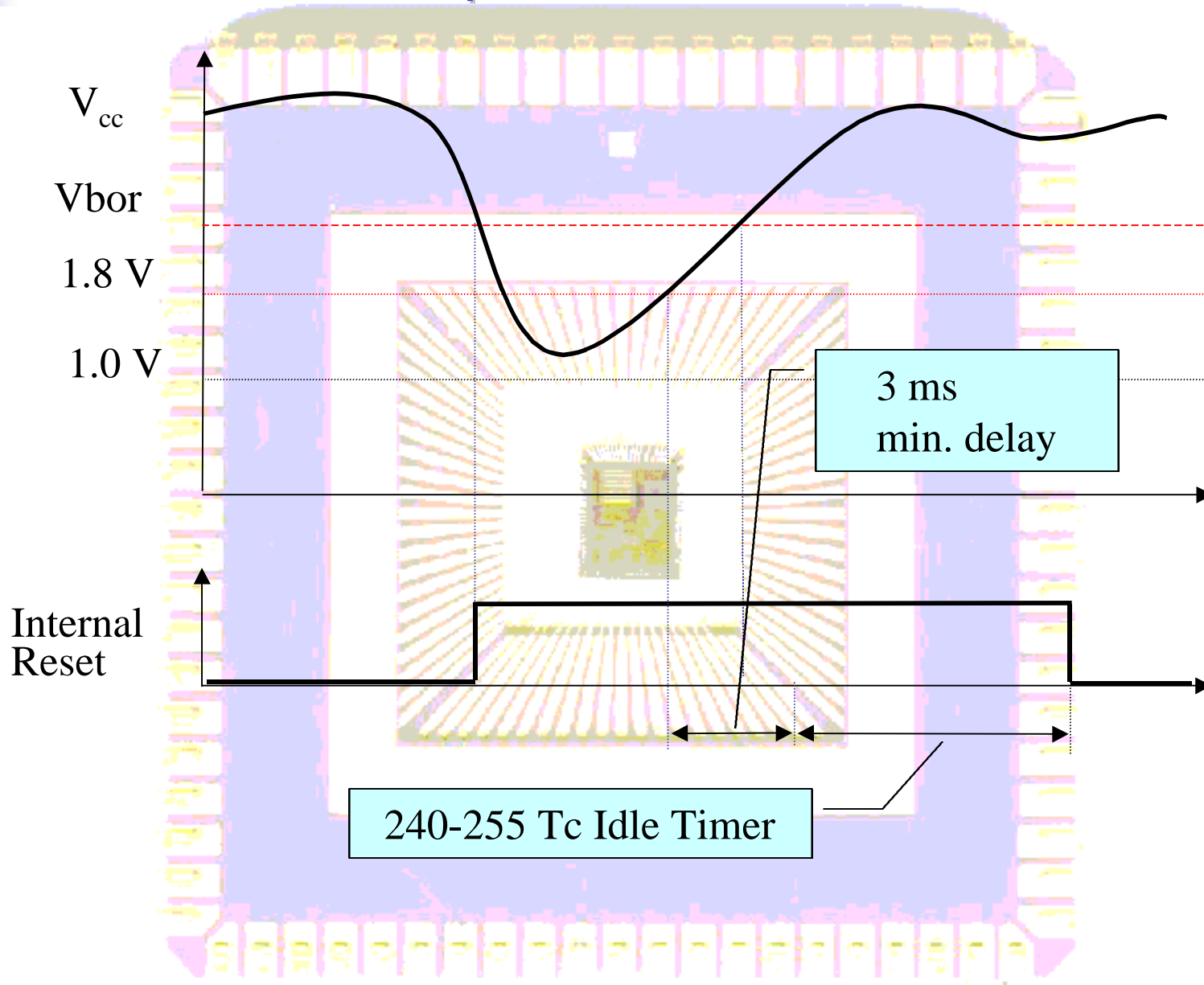
BROWNOUT

- Generates Reset and keeps device in Reset as long as Vcc is below the brownout trip voltage
 - Brownout trip voltage available in two settings:
 - COP8SBR 2.7-2.9V
 - COP8SCR 4.2-4.5V
 - COP8SDR No Brownout
- Generates Power-On Reset

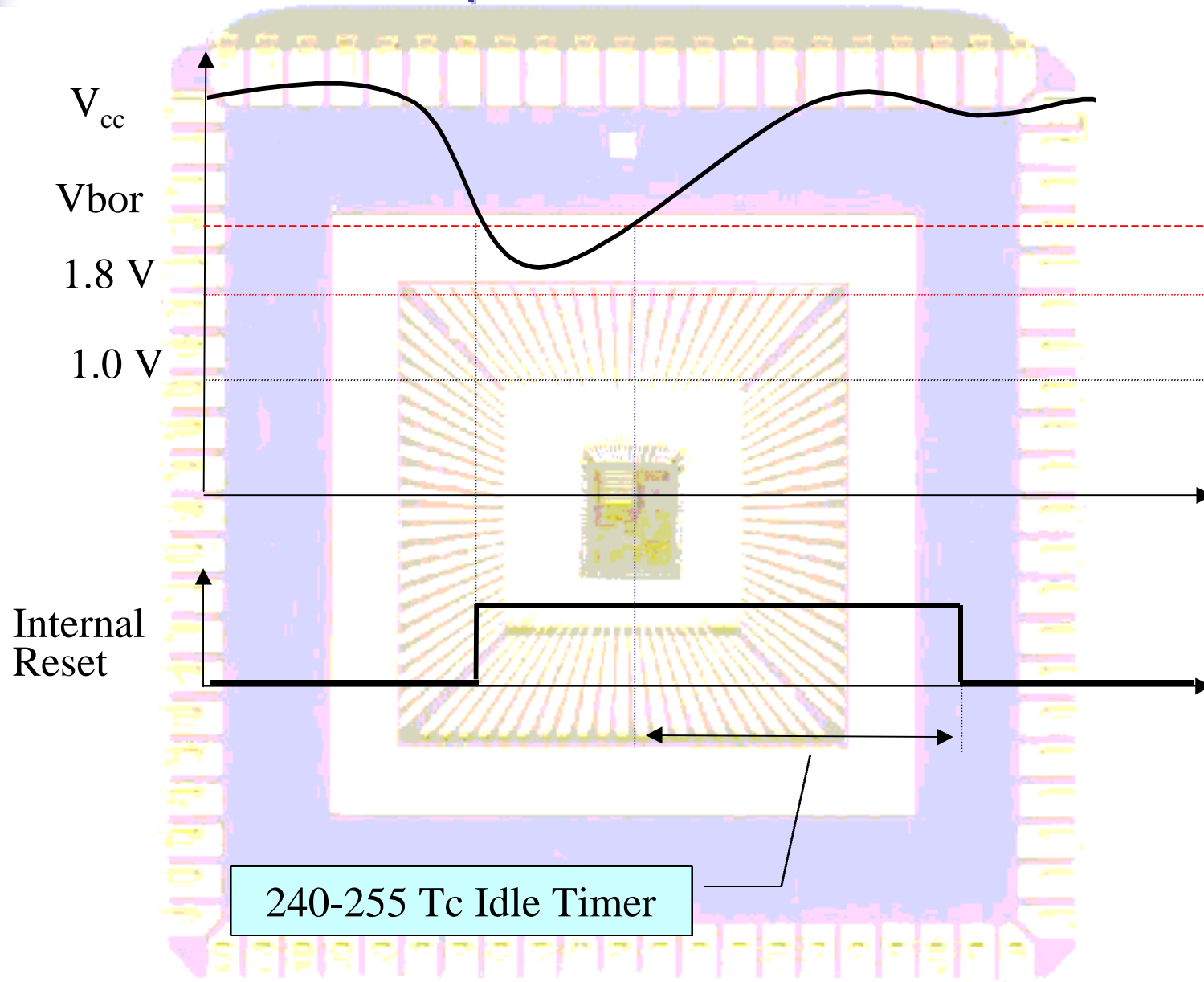
Brownout Operation - Power-On Reset



Brownout Operation - Vcc Brownout



Brownout Operation - Vcc Brownout

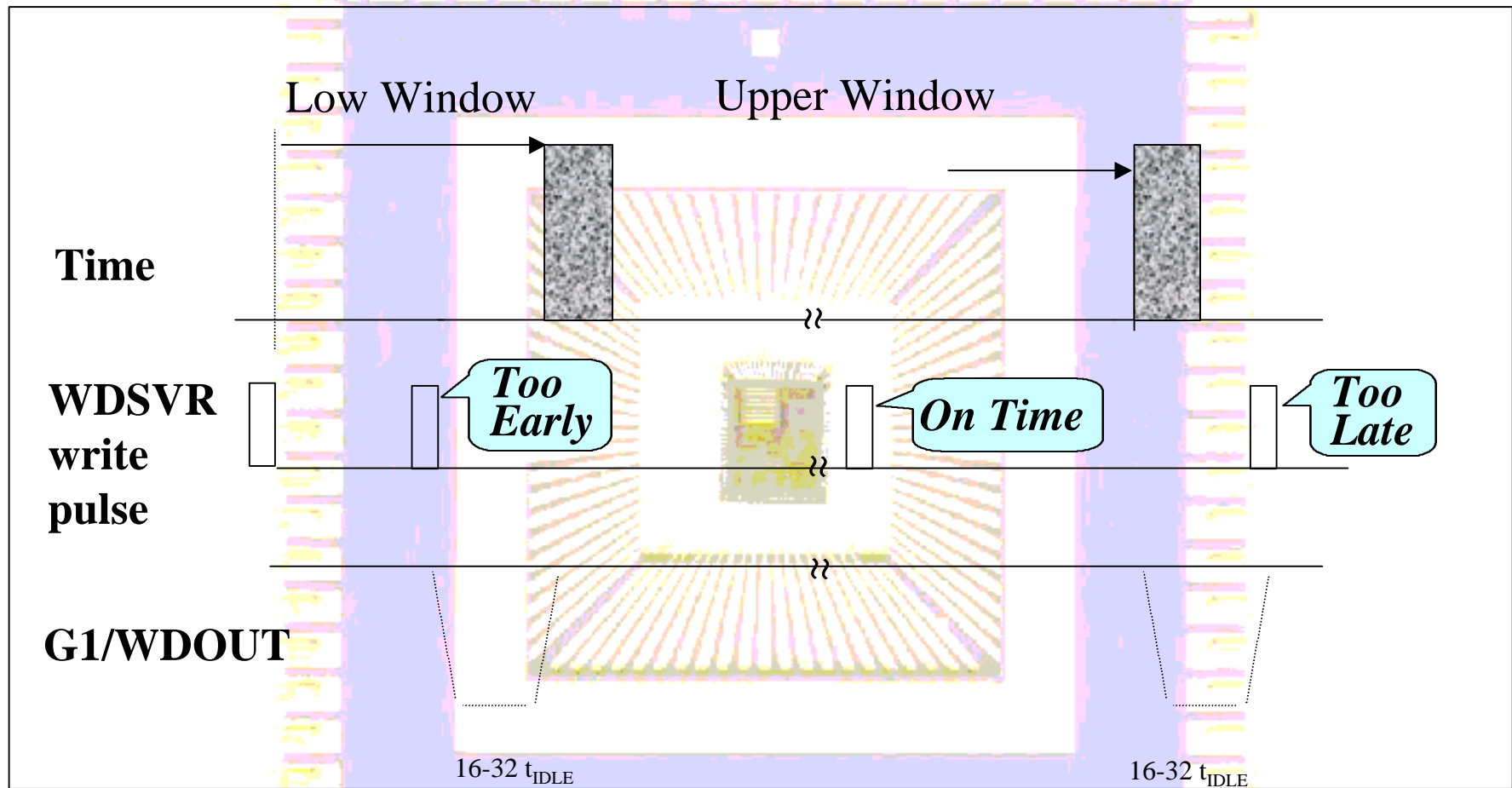


Windowed Watchdog

- Watchdog
 - Lower Limit = 2K IDLE Timer Tick
 - Service Register (WDSVR):
 - b7:6 = Upper Window Select (8K - 64K IDLE timer tick)
 - b5:1 = (01100) Key
 - b0 = Clock Monitor Enable/Disable

Upper Window Sel.		Key Data					Clock Monitor
MSB X	X	0	1	1	0	0	LSB y
7	6	5	4	3	2	1	0

Windowed Watchdog

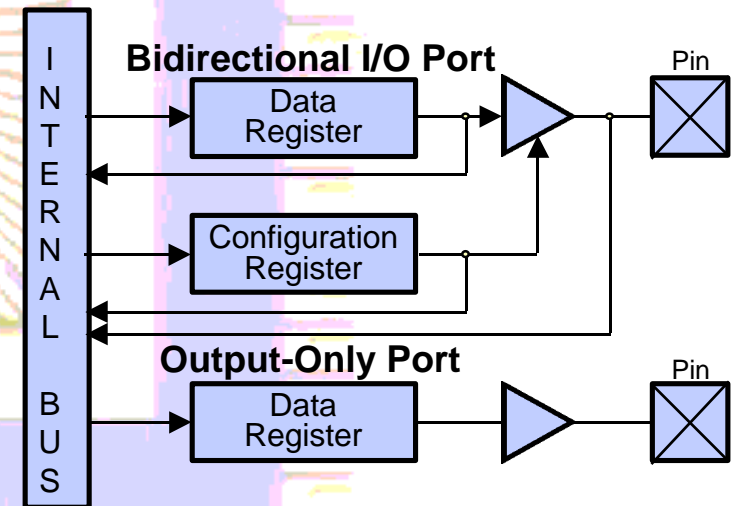


Clock Monitor

- Detects slow or stopped clocks to CPU
- Generates an error condition when selected CPU clock is below 25kHz
 - Provides same type of safety as a separate oscillator for the watchdog timer
- Pin G1 is held low while the clock input condition is not met

COP8FLASH I/Os

- All COP8FLASH I/Os have high sink/source capability (10mA/1.6mA)
- All I/O pins can be read back independent from any programmed I/O state (i.e., read the "true" external pin status)
- Individually software configurable I/O options for **each** pin
 - TRI-STATE Input (Open-Drain Output)
 - Weak Pull-Up Input
 - Push-Pull Output



COP8SBR Ordering Information

■ COP8S x R 9 H VA 8

Family Indicator

Temperature
8 = - 40 °C to + 85 °C

Package Type
VA = PLCC

Program Memory Size
R = 32 KB

Pin Count
H = 44
L = 68

x = Brownout Voltage Range Indicator

B	2.7-2.9V
C	4.2-4.5V
D	No Brownout

Program Memory Type
9 = Flash

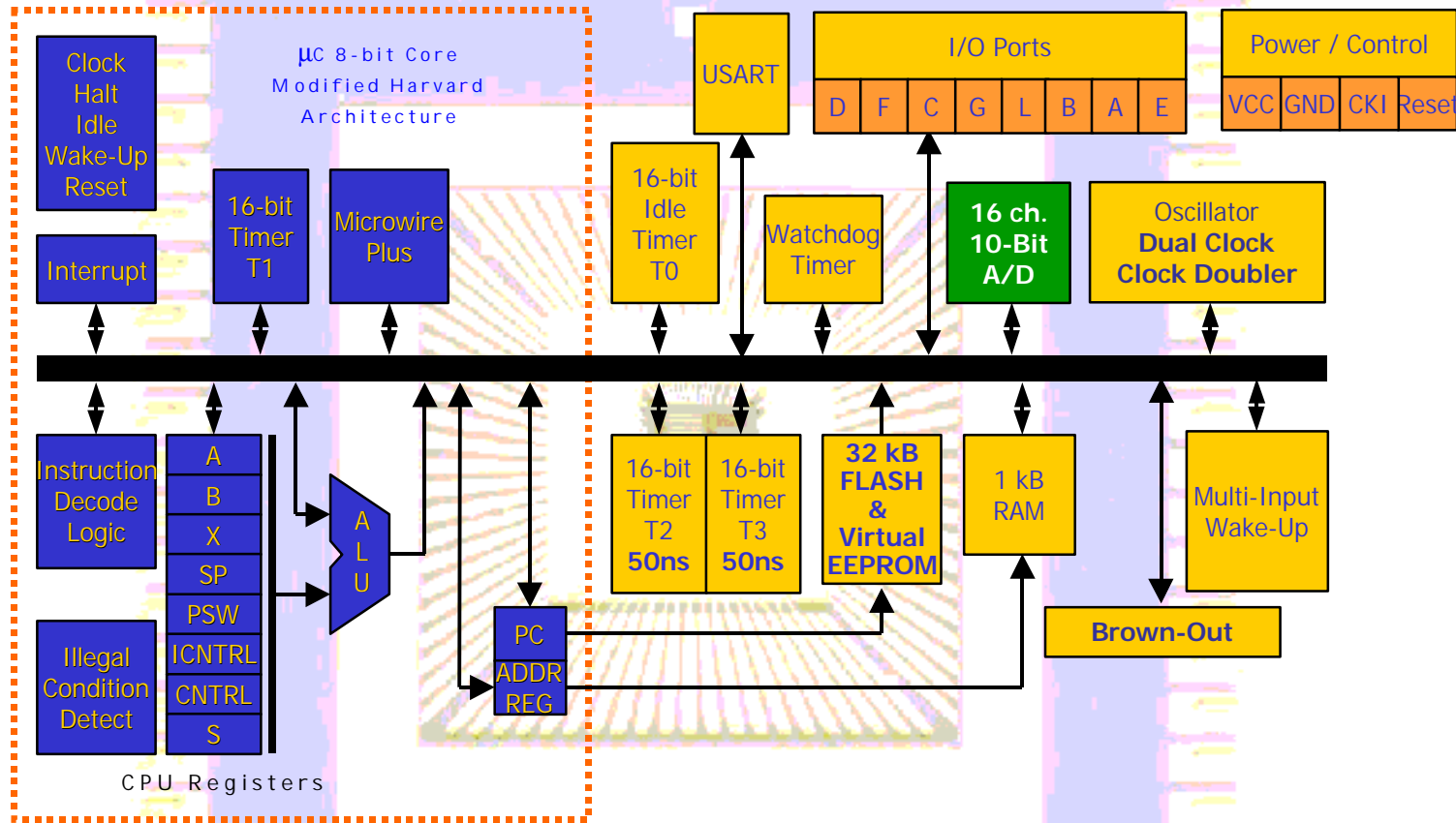
COP8FLASH



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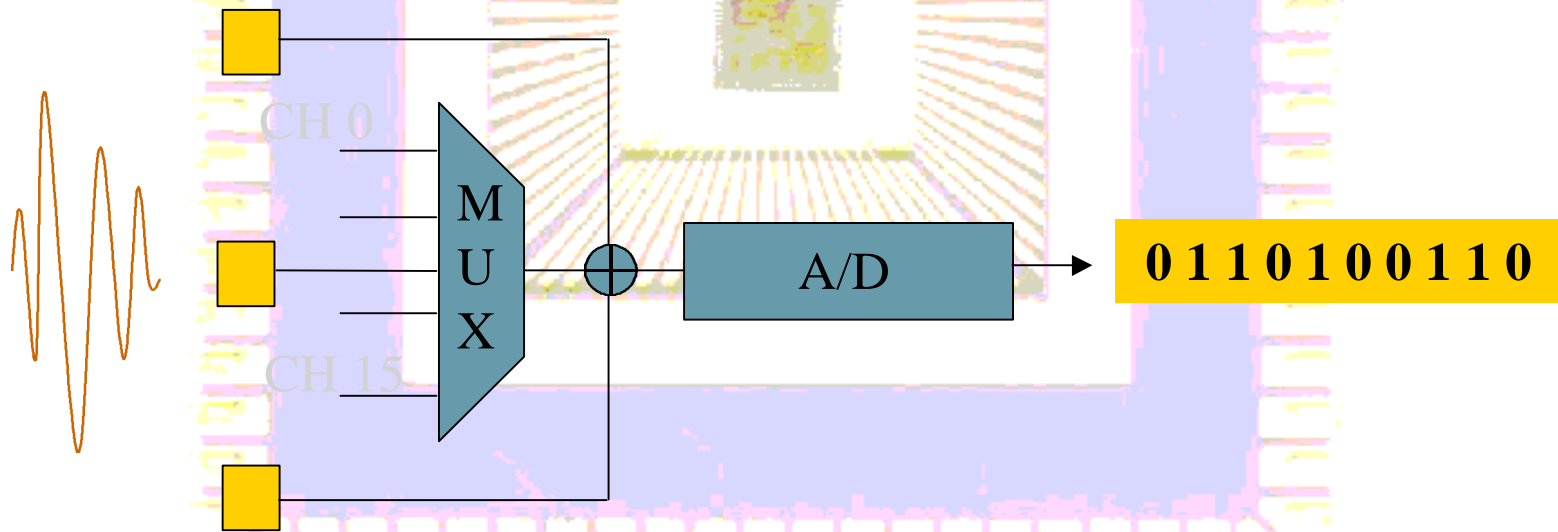
Higher Integration COP8FLASH

COP8CBR Block Diagram

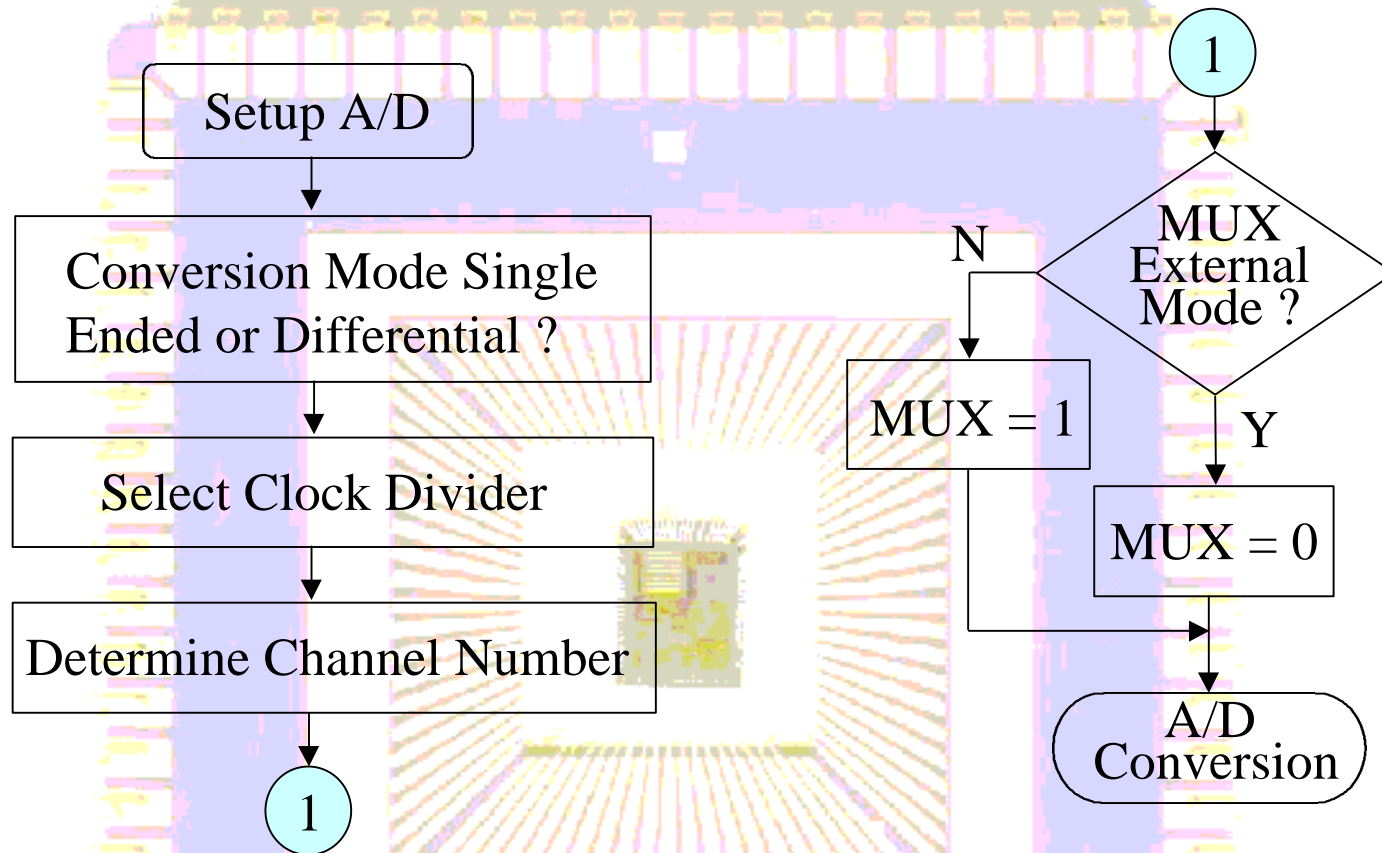


A/D Converter

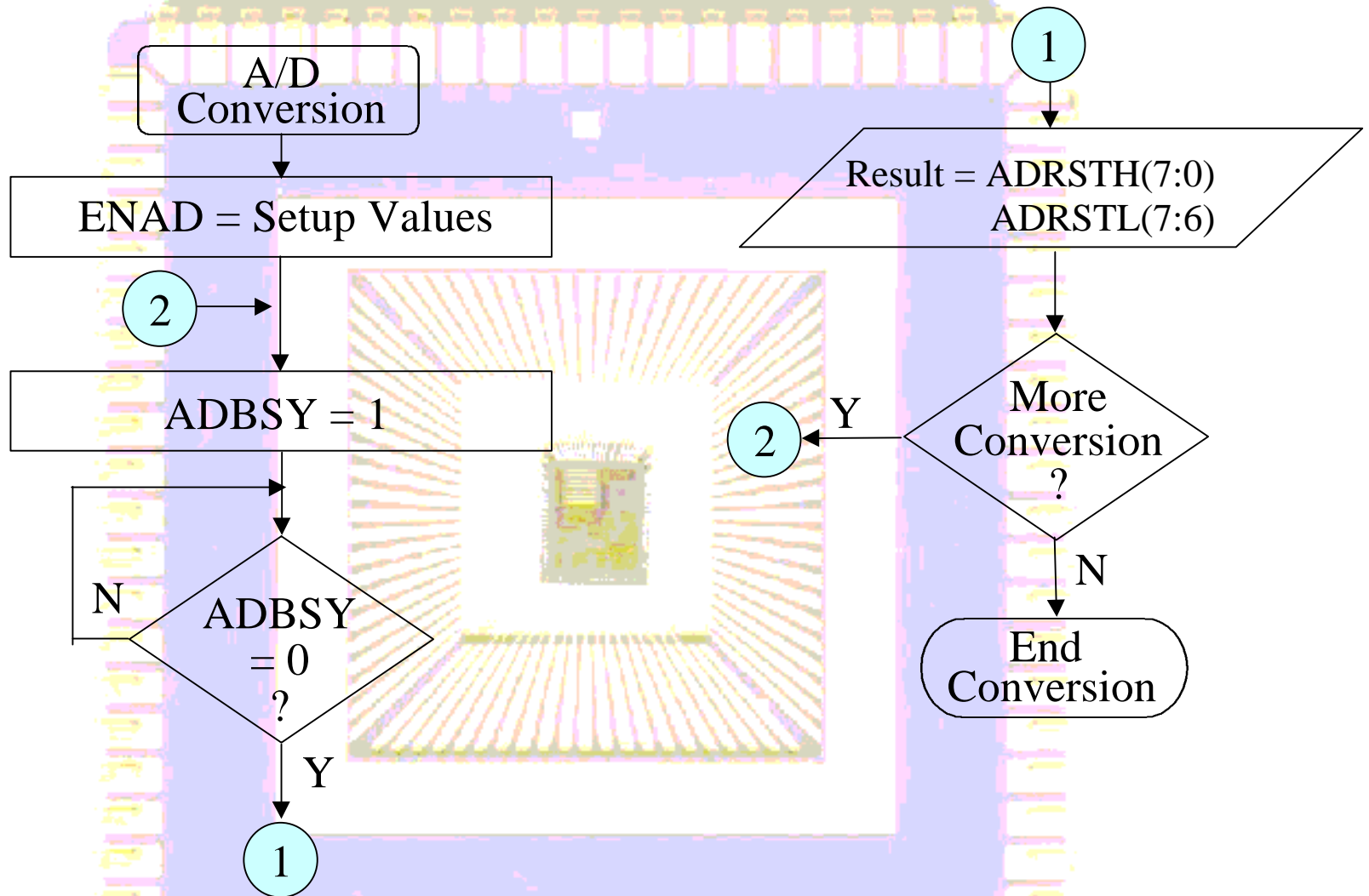
- 10-bit A/D
- Single Ended/Differential mode
- Versatile 16 Channel MUX
 - Internal connection to A/D
 - External I/O pad



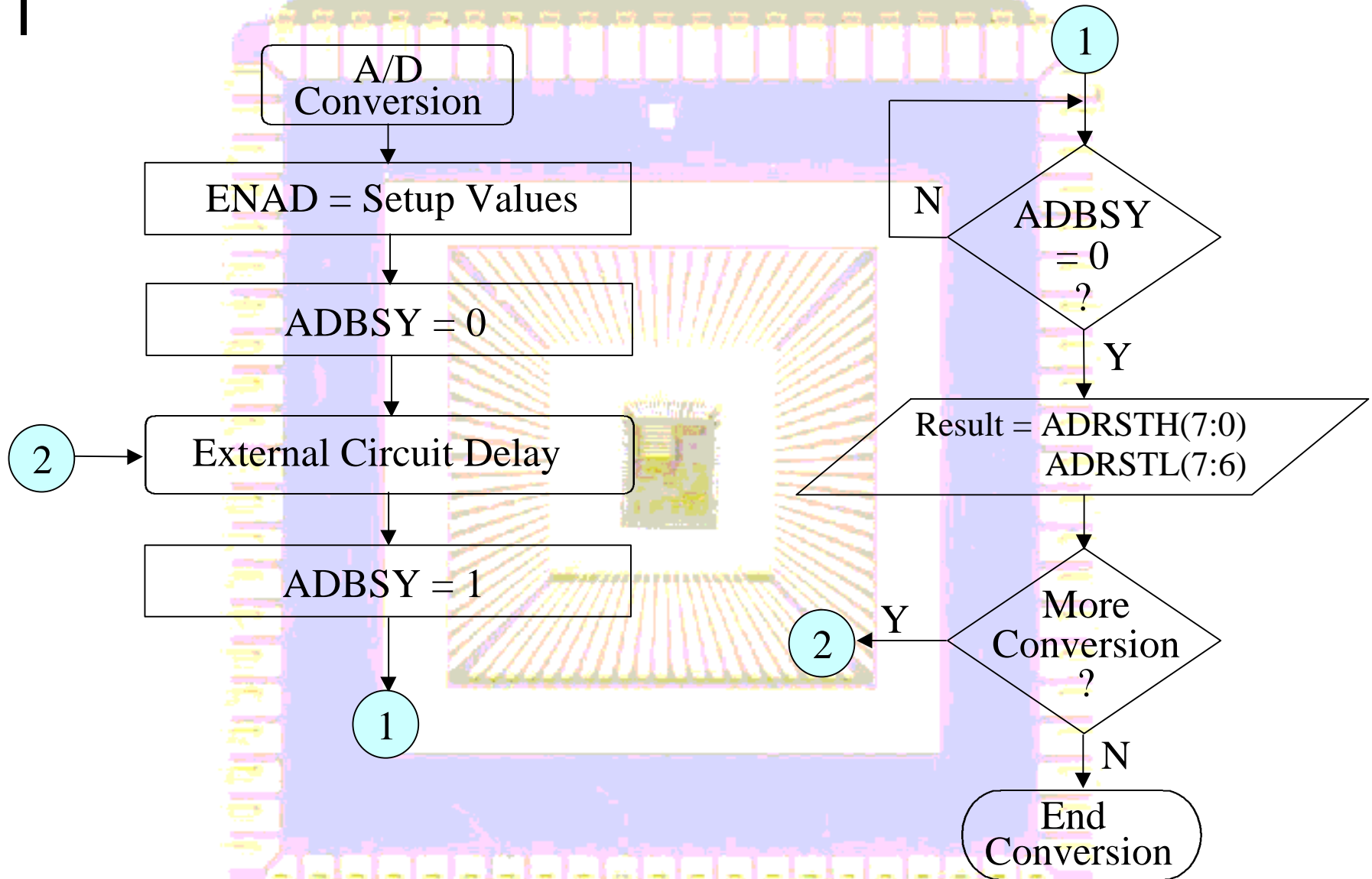
A/D Conversion - Setup



A/D Conversion - Internal Mode



A/D Conversion - External Mode



Single Ended MUX Out

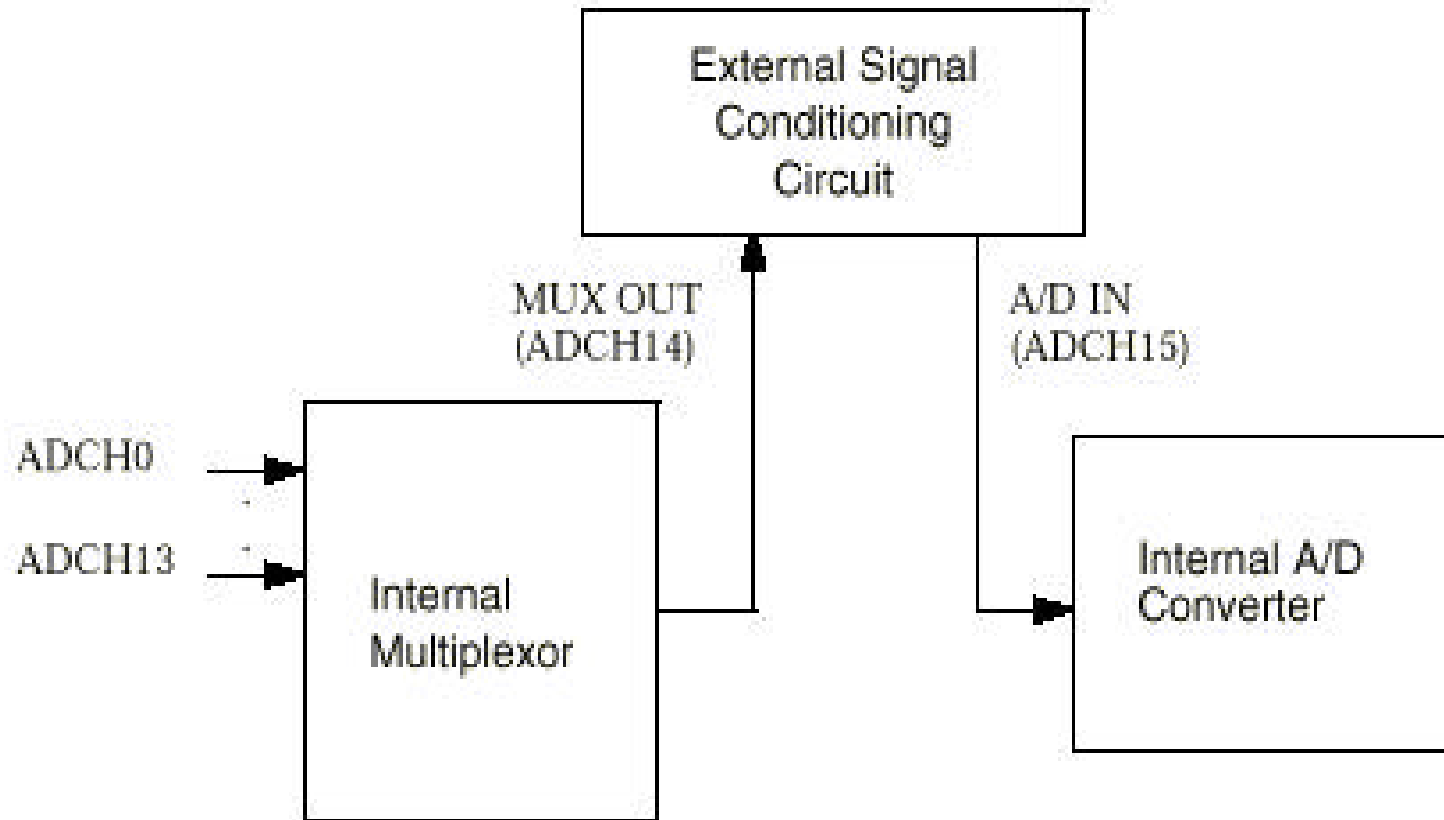


Figure 25. A/D with Single Ended Mux Output Feature Enabled

Differential MUX Out

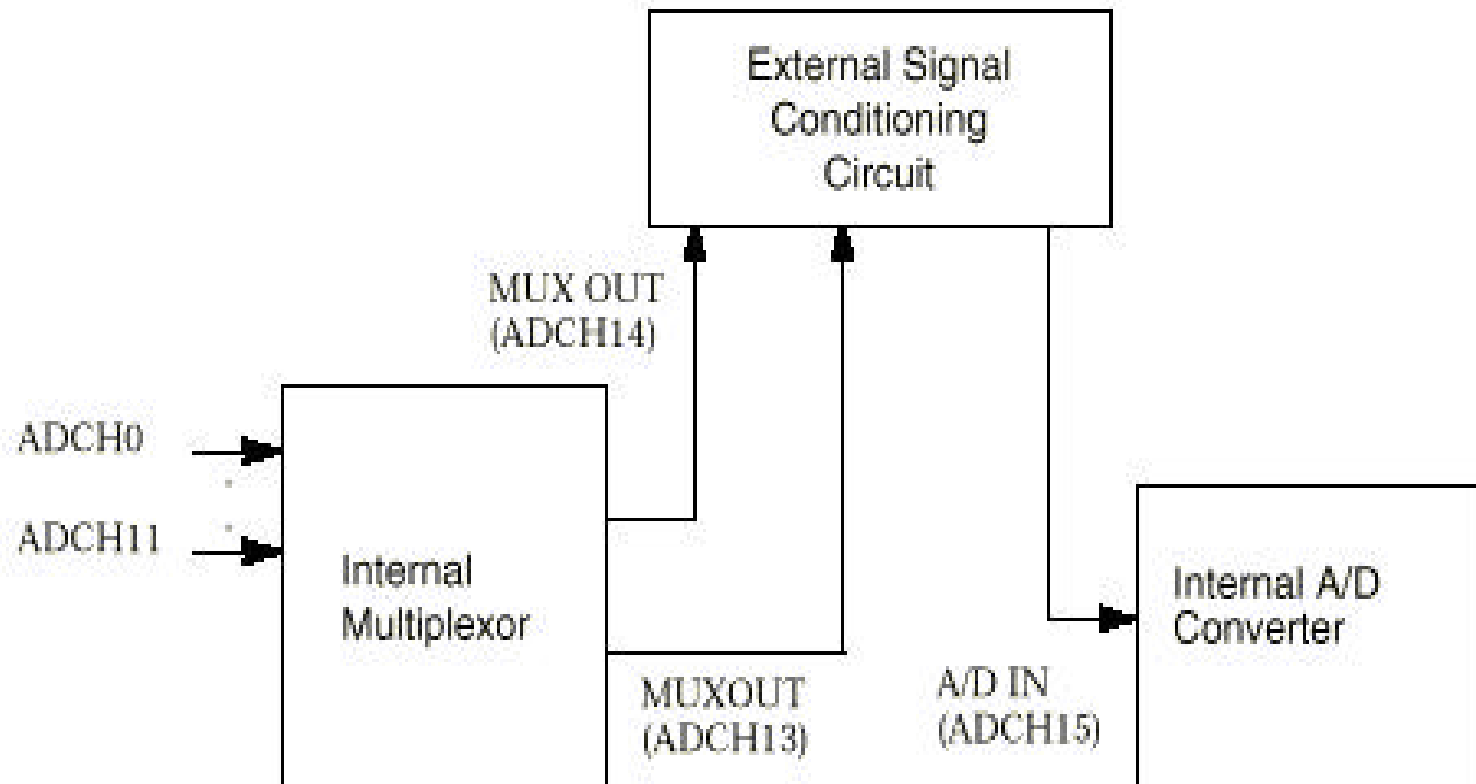
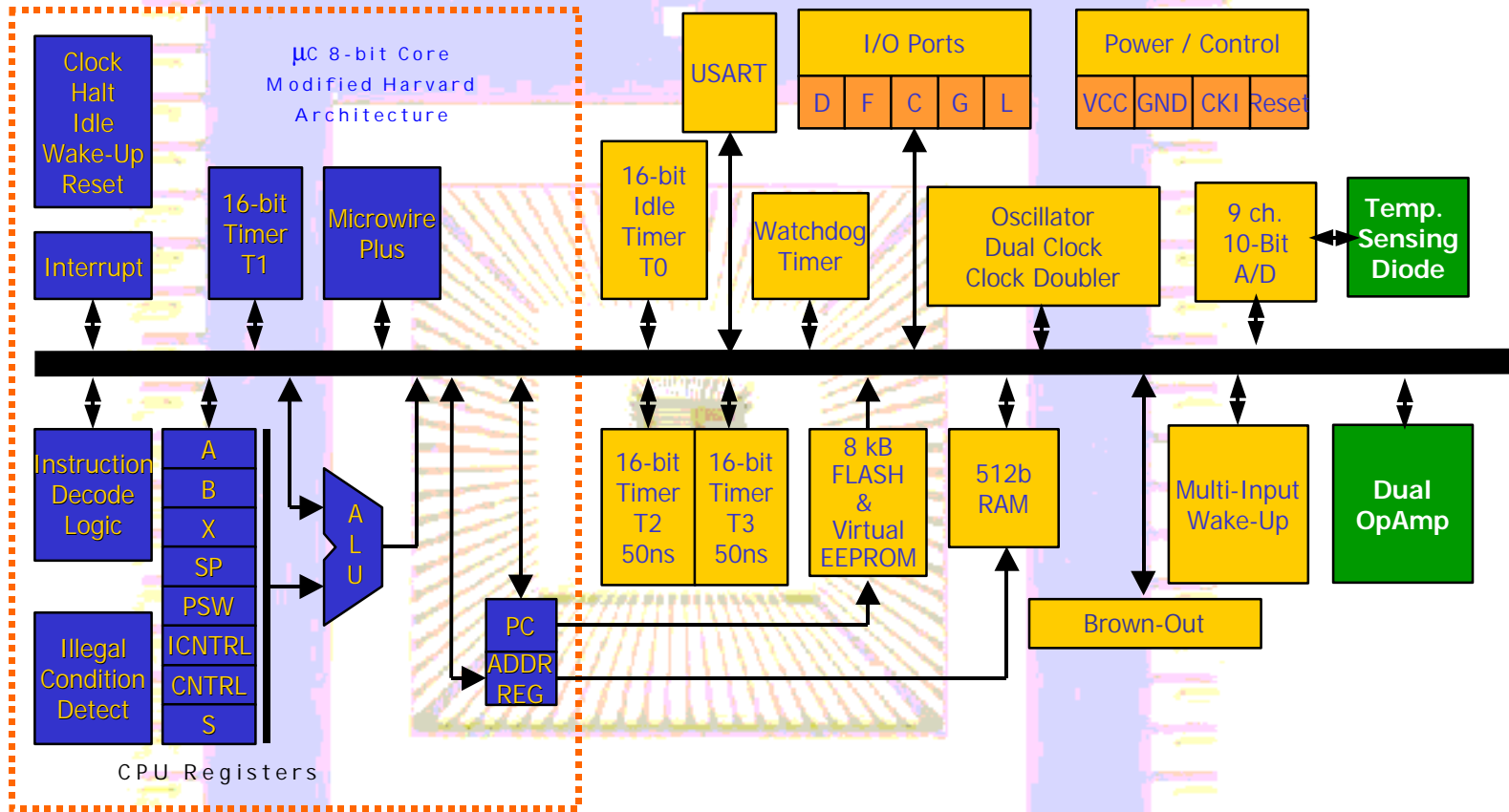


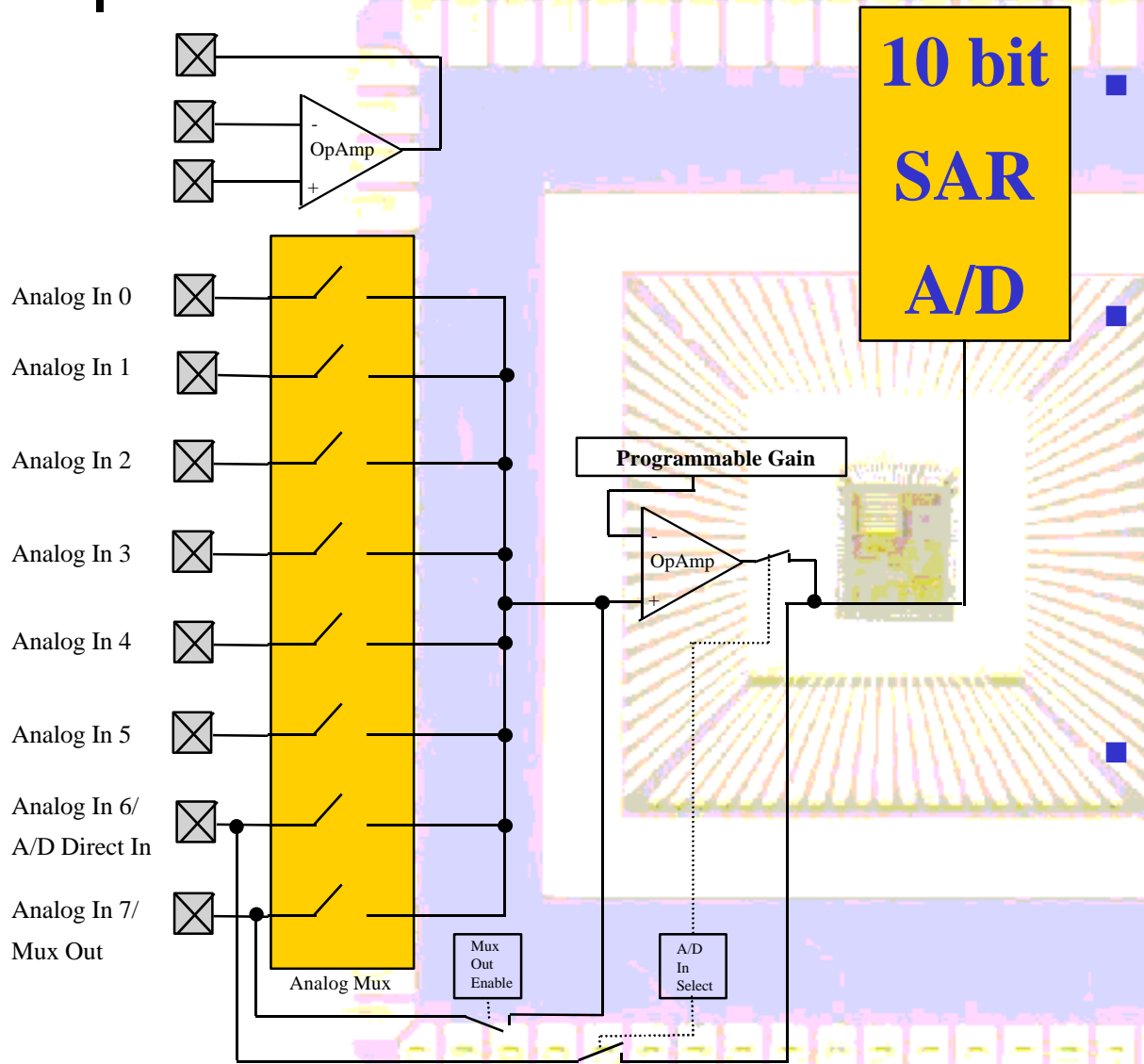
Figure 26. A/D with Differential Mux Output Feature Enabled



COP8AME Block Diagram



COP8AME A/D-OpAmp Block Diagram



- Saves up to 9 external OpAmps (1 per A/D input)
- Expandable through mux out - A/D input feature
 - Easily add additional A/D inputs
 - Filter functions
- Scale analog input signals to utilize full A/D resolution