

Reference schematic for redundant LVDS transmission

This schematic showcases an application for the following LVDS products by National Semiconductor: SCAN921821, SCAN90CP02, DS92LV18. Information and diagrams herein are provided for reference only. You may use it as whole or in part to create your own design.

This particular reference schematic has not been converted into a reference board. Please visit National Semiconductor's website www.national.com to obtain evaluation boards and related collateral material for each of the devices used (SCAN921821, SCAN90CP02, DS92LV18). For any designs based on this schematic always contact National Semiconductor Corporation BEFORE initiating PCB manufacturing and ask for your design to be reviewed.

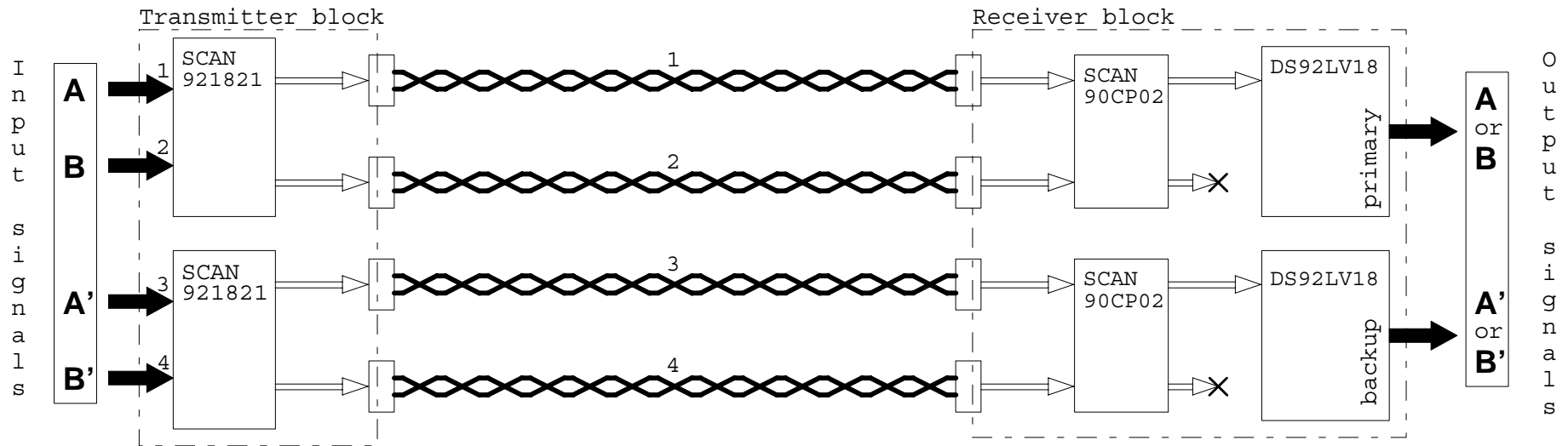
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NOTE: The performance (maximum throughput, cable reach and bit error rate) of this design depends in large on the cable and connectors used. Twisted pair cable may be used, but twin axial cable will generally yield the best results.

Please contact National Semiconductor for suggested cables, connectors and performance data.

Application Block Diagram



Application Overview

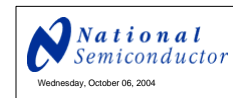
This application example features a dual channel transmission over a cable with redundancy towards failure of the transmitter side, receiver side, or transmission media.

The transmitter section takes two different 18-bit wide input busses (A and B) and serializes the data signals for transmission over a cable. For redundancy on the transmission side there are two dual transmitter chips that each require a copy of the two input signals.

The total of four serialized data streams are transmitted over four twisted pair cables to the receiver section. For each of the two signals there is a redundant data channel that carries an identical signal for immediate availability in case of a failure of the primary channel.

The receiver section features two crosspoint switch chips used to select one of its two incoming data streams and route them to a deserializer chip. The primary output resembles the original 18-bit wide data signal (either A or B).

If the active channel fails, the receiver can be switched manually to the backup of the selected channel (A' or B') at the backup output.

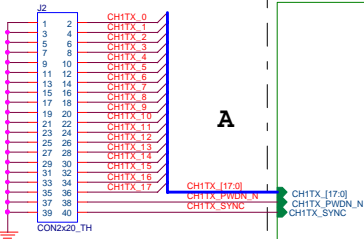


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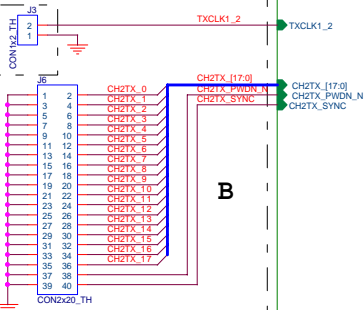
Size C	CAGE Code	DWG NO Redundant LVDS Reference Schematic	Rev I B
Scale	Block Diagram		Sheet 1 of 4

Feed TX input data on the headers below. SYNC input signal is used to ignore data and send a synchronization pattern instead.

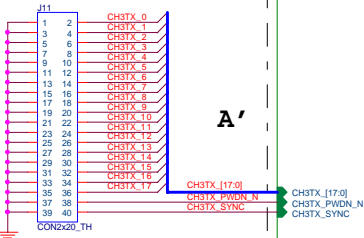
Primary



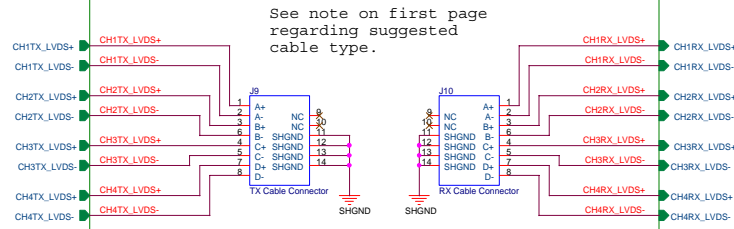
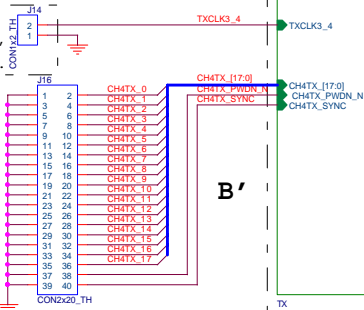
Feed reference clock for A and B here.



Backup

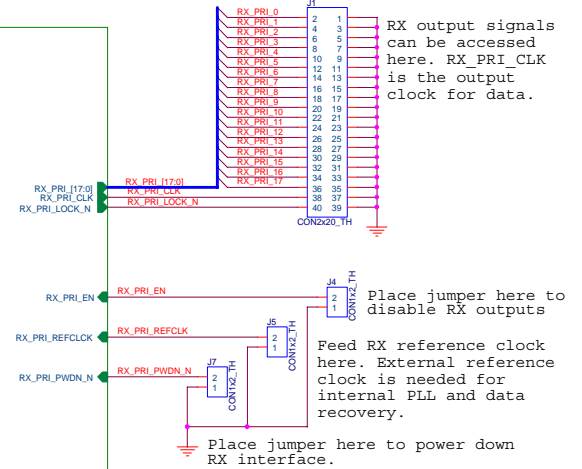


Feed reference clock for A' and B' here.



See note on first page regarding suggested cable type.

Primary



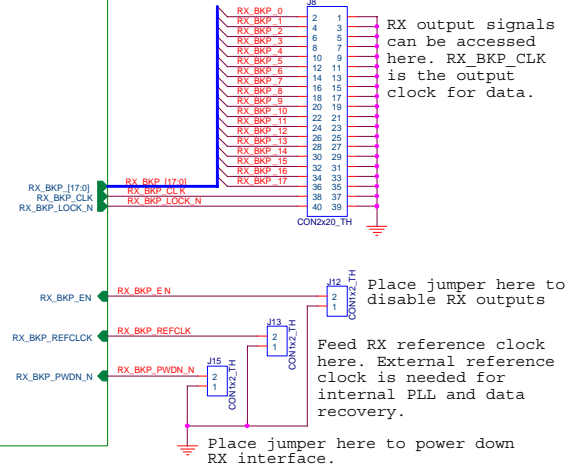
RX output signals can be accessed here. RX_PRI_CLK is the output clock for data.

Place jumper here to disable RX outputs

Feed RX reference clock here. External reference clock is needed for internal PLL and data recovery.

Place jumper here to power down RX interface.

Backup



RX output signals can be accessed here. RX_BKP_CLK is the output clock for data.

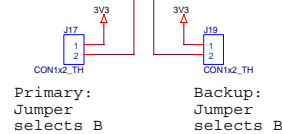
Place jumper here to disable RX outputs

Feed RX reference clock here. External reference clock is needed for internal PLL and data recovery.

Place jumper here to power down RX interface.

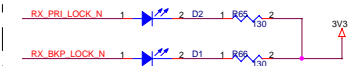
Manual channel selection.

Place jumper on these headers to activate channel B independently on primary and backup channels. Open header selects channel A. Jumper in place selects channel B.



RX PLL lock

LED will light if a PLL lock has been established.



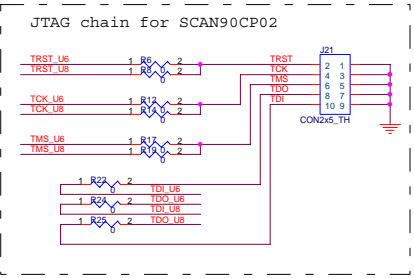
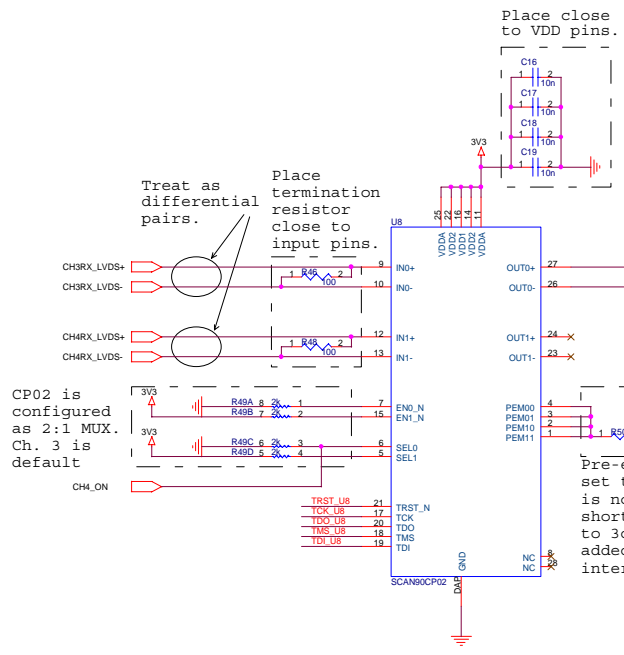
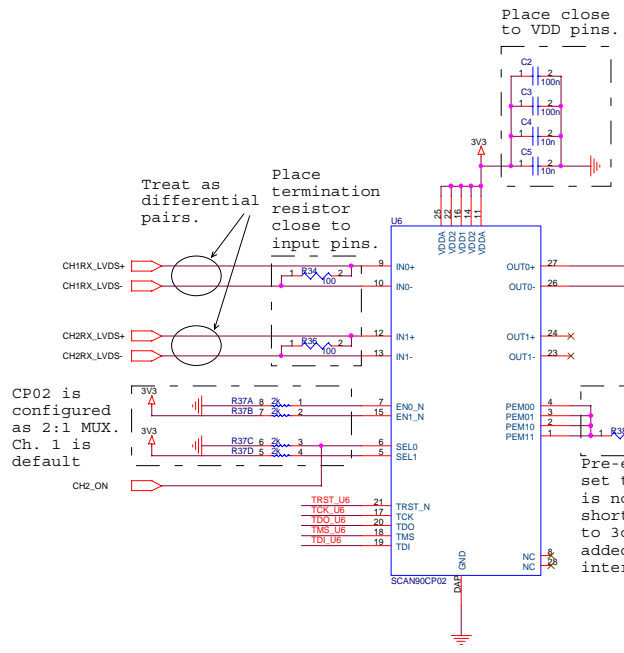
Note for low-active signals: Signal names for low-active signals are noted with the suffix _N.



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Scale	Top Level	Sheet 2 of 4	

Note for low-active signals: Signal names for low-active signals are noted with the suffix _N.

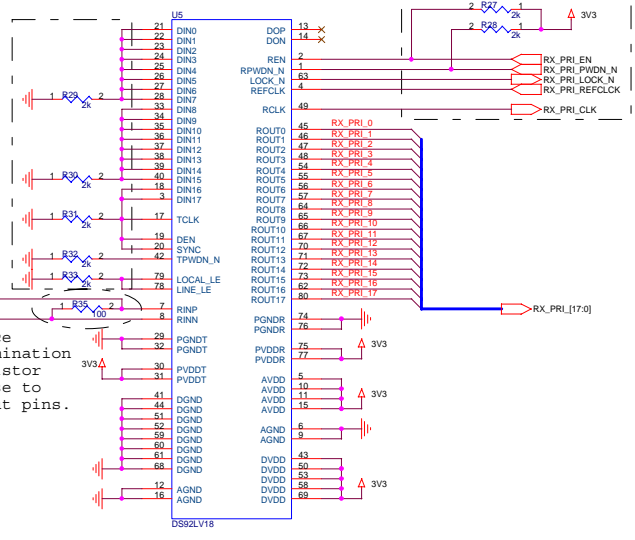


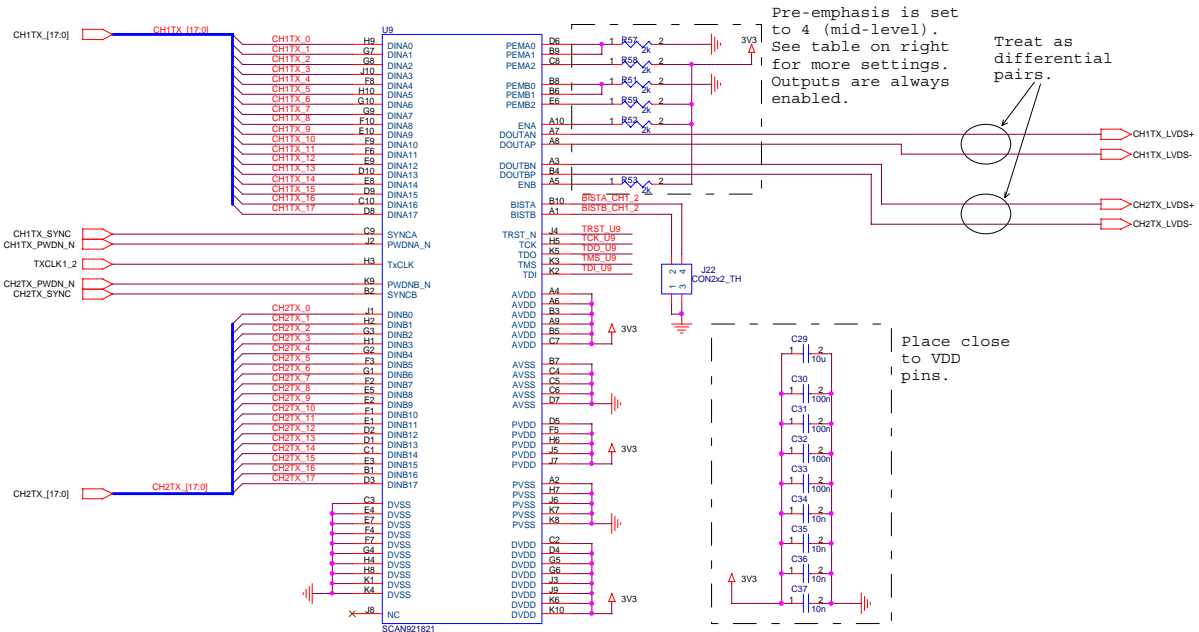
The TX interface is not used in this application and has been disabled.

Place termination resistor close to input pins.

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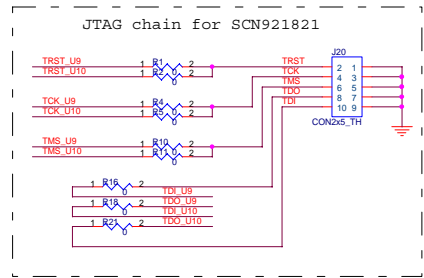
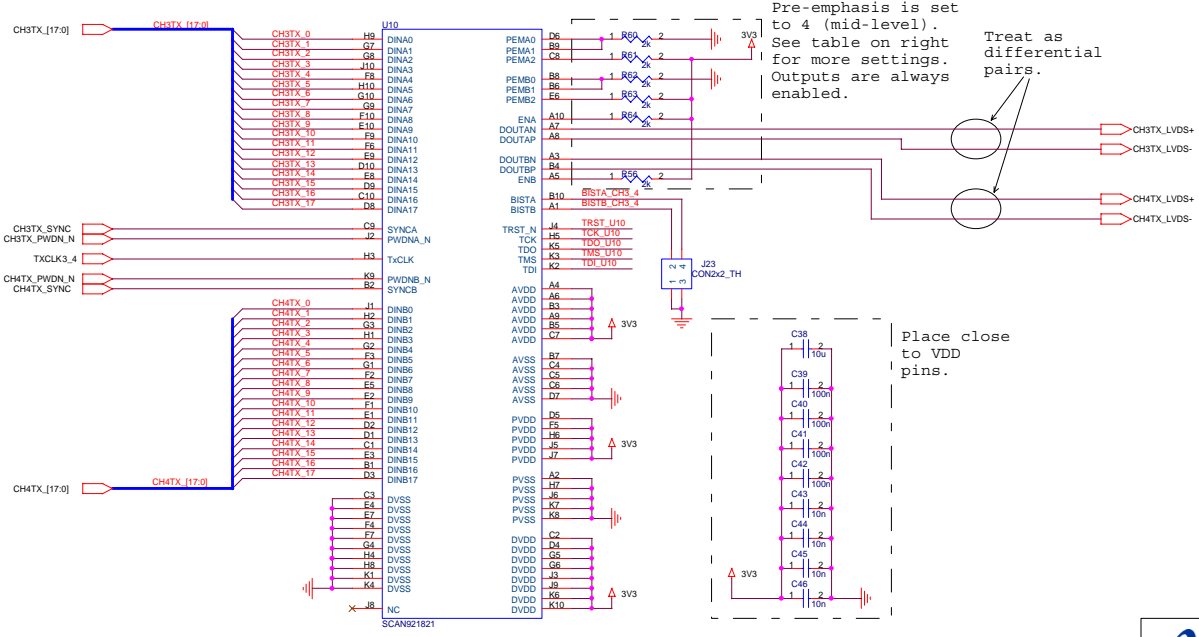
Place termination resistor close to input pins.



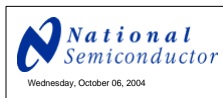


Suggested pre-emphasis settings for some cable type-length combinations for SCAN921821:

Cable Length	Cable Construction	Pre-Emphasis Level
15 meters	24 AWG Twin Ax	7
10 meters	28 AWG Twin Ax	7
5 meters	28 AWG Twin Ax	4
3 meters	28 AWG Twin Ax	2



Note for low-active signals: Signal names for low-active signals are noted with the suffix N.



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C		Redundant LVDS Reference Schematic	1 B
Scale	Transmitter		Sheet 4 of 4