9.3: WhisperBus™: An Advanced Interconnect Link For TFT Column Driver Data

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Abstract
Increasing video data rates to liquid crystal displays brought about by increasing display format sizes and increased grayscale content are placing very high demands on digital data busses. These higher data rates coupled with constraints on EMI levels, size, power and component count are rendering CMOS data busses inadequate for the connection between the timing controller and the column drivers. The operation and performance of a comprehensive solution using a current signaling method (WhisperBus™) is presented.

1. Introduction and Background
As display formats become larger, video rates to the display correspondingly increase. For example, UXGA (1200 x 1600 pixels) is the equivalent of four SVGA panels (600 x 800 pixels) tiled together and requires a corresponding four-fold increase in the video data rate compared with an SVGA display for the same refresh frequency. In addition, there is a trend toward 24-bit grayscale rather than 18-bit grayscale in the larger formats especially when they are used for monitor applications. This increased grayscale represents an additional 33 percent increase in data rates. At the same time, there is a strong market demand to minimize bezel width and panel thickness, reduce costs through reduced PCB layers and components and to do all this while improving the robustness of the electrical and mechanical design.

These factors combine to put demands on the traditional CMOS data bus connecting the timing controller and the column driver that it cannot meet. The most significant problem is EMI. Even the present day, mainstream panel, the XGA display (768 x 1024 pixels) requires substantial design effort to manage the EMI to acceptable limits. This paper describes a new interconnect signaling method, WhisperBus™, used in a point-to-point interconnect topology to eliminate the EMI problem for today's XGA designs as well as the larger formats and is extensible well into the future. The new interconnect method uses fewer PCB wires than the CMOS bus interconnect facilitating lower cost and thinner displays through the use of fewer layer PCBs. In addition, a number of other significant benefits arise from the use of this topology that will be discussed here.

Electro-magnetic interference (EMI) from the radio signals launched by the digital video data signaling to the display panel has been a serious problem for the LCD display industry for some time. The introduction of the XGA format into mass production, circa 1997, brought with it the need for new technology to solve the EMI and wire density issue at the hinge of the LCD notebook PC (NBPC) application. A number of technologies were experimented with but in the end, LVDS, low voltage differential signaling, developed by National Semiconductor, emerged as the defacto standard for this interconnect, particularly in NBPCs.

Within the display module, the video data link between the timing controller ASIC and the column drivers is a major source of EMI. In the SVGA display, with its 600 x 800 pixels format, the 18-bit color gray-scale video data is bussed directly as an 18-bit word to each column driver. This approach was impractical in the XGA display, with its 60 percent larger 768 x 1024 format and corresponding 60 percent higher digital video data rate compared with the SVA display. The EMI generated from the link between the timing controller and the column drivers is managed in part through the adoption of a dual bus system. In this convention, 18-bit video data is split into two 18-bit data paths, one for the even numbered columns and one for the odd numbered columns. Of course 24-bit color gray-scale is sent on dual 24 bit busses. This technique, while adding wires and thereby space to the link between the TCON and the column drivers, made the management of EMI practical for the XGA display.

The dual bus technique together with good PCB layout techniques, shielding and various other methods are the methods used to this point manage the EMI through the SXGA format (1024 x 1280 pixels) and it's bigger cousin the SXGA+ format (1050 x 1400). The UXGA format (1200 x 1600) forces a new level of response from the industry. The generally agreed upon solution is to replace the bus between the TCON and the column driver with a new, low EMI link and several companies have introduced technology to do this. National has two technologies, RSDS and WhisperBus™. RSDS is named for its description, Reduced Swing Differential Signaling (compared with LVDS). It replaces the CMOS data path with a differential pair operated at higher frequencies which allows fewer data lines than CMOS but due to its differential signaling reduces EMI to very low levels. The other solution, WhisperBus™ will be described in detail here.

2. WhisperBus™ Link Operation
WhisperBus™ uses singled-ended, low current signaling rather than differential signaling to transfer the digital video data without the EMI generated by conventional CMOS signaling. The key advantage of single-end drive over differential is of course the number of wires required for a channel of data. An 18-channel link for example requires 36 wires in differential mode transmission but only 18 wires plus ground in a single-ended mode transmission, CMOS TTL signaling being a common example of single-ended transmission.

2.1 Receiver Operation
The WhisperBus™ ability to signal in single-ended, low level currents is due to the nature of the receiver. Conventional differential signaling, also signals in current but receives in voltage. The differential current develops a voltage across a terminating resistor, which the receiver differentially amplifies in the voltage domain to convert it back to a CMOS level voltage signal. In this approach, the voltage across the terminating resistor must be well above the voltage noise floor to reliably recover the signal. The proper termination resistance of a typical PCB transmission line is approximately 50 Ohms per line or 100 Ohms differential. Since the resistance is quite low, the differential current must be on the order of milli-amps in order to produce the hundreds of milli-volts needed for a practical system. In RSDS for example, 2mA is typical (200mv differential).

The current to voltage conversion in the WhisperBus™ receiver is fundamentally different from conventional differential receivers. The WhisperBus™ receiver converts the signal current in the link directly to voltage using active circuitry that intrinsically provides the termination resistance. Figure 1 shows an equivalent circuit comparing both the differential mode receiver and the WhisperBus™ receiver. Notice that there are no external components required with WhisperBus™.

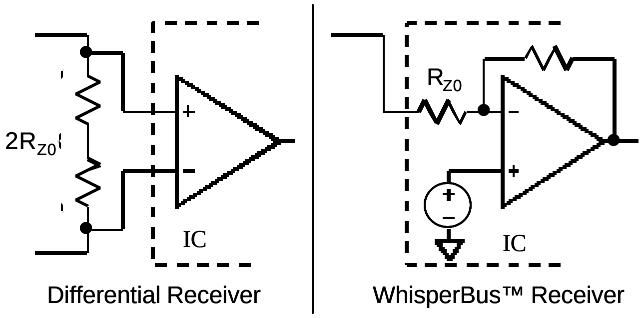

Figure 1. *Comparison of WhisperBus™ Receiver to a conventional, differential mode receiver.*

In the WhisperBus™ system, binary digital data is signaled as either a lower current or a higher current, on a single wire. Both current states flow in the same direction, always from the receiver to the transmitter. The transmitter transmits its binary information to the receiver by sinking one or another current from the receiver based on an incoming CMOS voltage level. The two currents can be considered to be an AC current riding on a DC bias current. Typically, the two currents would be 50µA and 150µA and considered to be +/- 50µA riding on a constant 100µA bias current. This 100µA is more than an order of magnitude smaller than the 2000µA typical of RSDS for example.

The voltage at the summing junction of the amplifier in the WhisperBus™ receiver shown in Figure 1 is maintained at approximately 1 volt by design. The actual value of the voltage is not critical to the operation of WhisperBus™ and is dependent on transistor thresholds in the receiver. From an operational standpoint, its purpose is simply to allow the transmitter to be able to sink current from the receiver without taking the node to a voltage below ground. From an AC perspective, the input to the WhisperBus™ receiver looks like a resistance of R_{Z0}, which is set to approximately 50 ohms to match the characteristic impedance of a typical PCB trace.

The DC component of the WhisperBus™ signal (100µA for example) flows through R_{Z0} an produces a DC voltage of 5mv across it which when subtracted from the approximate 1 volt bias at the summing junction (current flows from the receiver to the transmitter) is a DC voltage of approximately 0.995 volts on the WhisperBus™ line. The AC signal of +/- 50µA across the 50 ohm termination resistor produces a +/- 2.5mV signal riding on the 1 volt bias. This +/- 2.5mV AC component is 660 times smaller than a 3.3 volt CMOS TTL signal (+/- 1.65 volts). This reduction in signal swing over TTL is in large part responsible for the more than 225 times reduction in EMI achieved by WhisperBus™ over CMOS TTL.

2.2 Transmitter Operation

The WhisperBus™ transmitter functions as a two-state current sink, sinking one or another current from the receiver depending on the input CMOS TTL state. See Figure 2. Notice that the circuit doesn't determine the voltage on the output of the WhisperBus™ transmitter but rather the receiver sets the voltage. The transmitter can accommodate a wide range of receiver voltages and in practice can operate to as low as a few hundred milli-volts above ground. This is important because it allows the transmitter and receiver to be fabricated in different processes and even to be powered by different supply voltages. Notice also, that the current into ground is constant and not data dependent. This is important to other circuitry, especially analog circuits, because steady substrate currents allow the ground reference voltages to remain stable.

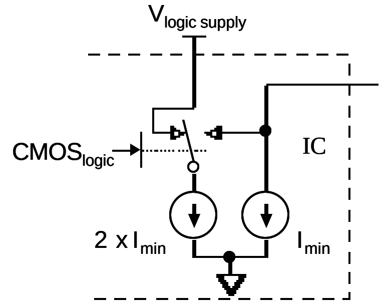

Figure 2. *WhisperBus™ Transmitter equivalent circuit.*

2.3 The WhisperBus™ Link

Figure 3 illustrates two WhisperBus™ channels communicating between two ICs as an example. The actual number of channels in the application will depend on the total data transfer rate required. Note the signal ground return path, common to all the channels. This ground is isolated from the power ground points on the substrate by several ohms. This feature assures that the receiver and transmitter are referenced to the same electrical node and that high currents do not pass through the ground path between the transmitter and the receiver creating a voltage difference between the two ends of the link.

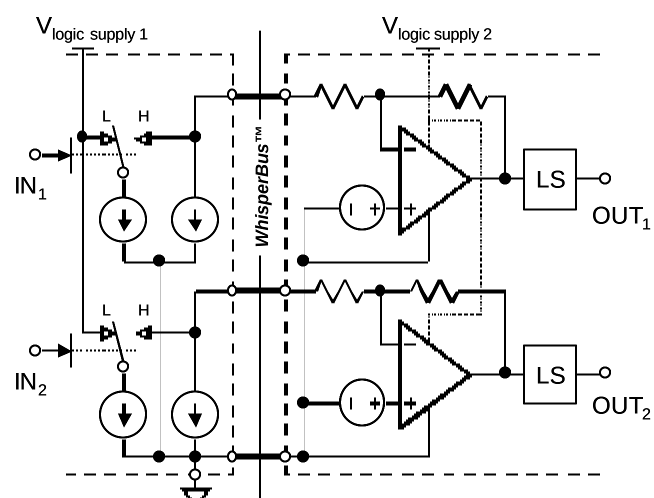

Figure 3. *Two channel, chip-to-chip, WhisperBus™ link with potentially independent logic supplies and IC process geometries.*

The bandwidth of the link is not limited by the WhisperBus™ transmitter or receiver circuit but by the speed of the CMOS logic on either end. The WhisperBus™ link itself is a very high bandwidth circuit with a relatively small signal amplitude compared with the rail-to-rail CMOS logic. The limiting speed of the link then outside of the CMOS logic speed constraints is the signal to noise ratio on the link itself. The signal current can be programmed higher or lower with the +/- 50µA working well in the typical column driver environment.

3. Point-To-Point Topology

WhisperBus™ forms an important base on which the topology of the TCON and column driver system is built. There are a number of significant features this topology/link provides including: ultra low EMI, reduced power, reduced component and signal trace count, reduced column driver die size, 6 or 8 bit grayscale with no additional cost and support for independent RGB gamma for color temperature control without graylevel reduction. Each of these features will be discussed here.

3.1 Benefits to Point-to-Point

Figure 4 shows an XGA example using WhisperBus™. There are several important features illustrated in this example. First is the point-to-point topology, which allows each column driver to receive data simultaneously throughout a line time. The multi-drop bus topology requires a column driver to receive its data in short bursts since the bus is shared among other column drivers. In the point-to-point topology each column driver is receiving data simultaneously, which allows the data rate to each driver to be reduced by a factor of at least eight (in the XGA case with its eight drivers). In addition, the TCON buffers the incoming data at the dot clock rate but re-transmits it to the column driver at a rate that uses the whole line time and thus can further minimize the data rate to column driver. While the TCON does require a full line buffer in the point-to-point topology, we have designed a special memory cell that makes the memory size so small as to not be a significant size and cost factor. Any small size increase in the TCON is more than offset by the reduction in CD die size multiplied across the 8 or 10 or more column drivers per system.

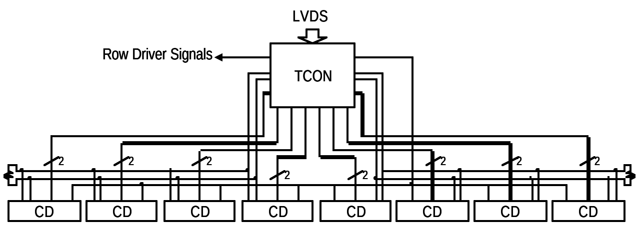

Figure 4. *18-bit or 24-bit XGA example showing point-to-point topology in "T" configuration, differential clock, and 2 wire WhisperBus™ data link per driver.*

3.1.1 Few Data Lines, Small TCON

The 2 wire WhisperBus™ data link between each column driver (CD) and the timing controller (TCON) is sufficient for either 18-bit or 24-bit color data rates. The XGA solution only requires a total of 16 data pins from the TCON (and just 2 per column driver). This small data pin count in the TCON coupled with an LVDS input for example, allows the TCON to be packaged in an 80 pin TQFP.

3.1.2 "T" or "L" Configuration Supported

Only one differential clock is needed to drive all the column drivers. The differential clock allows multi-drop bussing to all the drivers and clocking is on both edges to minimize frequency. Dual clock sources on the TCON facilitate the "T" configuration layout with having to drive a transmission line from the center with a long stub. The "L" configuration is also supported using just one of the two clock sources. Outside of any power supply decoupling capacitors, the column driver PCB is free of any additional components except for the termination resistor(s) for the differential clock. This is in contrast to differential busses, which require external termination of each data channel. (WhisperBus™ is self-terminating).

3.1.3 Data & Control Supported on WhisperBus™

The WhisperBus™ link is used to support both data transfers and column driver control protocols to the column drivers. One of the features of this protocol is the clock de-skew function. Each driver has a slightly different data path length between it and the TCON. In addition, the clock path length also varies from driver to driver. At the start of each row, the WhisperBus™ data link sends a special sync pulse, which the receivers use to adjust the clock delay to provide the best clock to recover the data. This dynamic adjustment assures robustness of the design.

3.1.4 Minimal PCB Signals, CD I/O

The control protocol also provides the transmission of the polarity signal to the column driver. The data shift direction is determined by the TCON and not by the column driver so that no shift direction signal is needed, eliminating a column driver input and a column driver PCB signal trace. The point-to-point topology eliminates the need for a data shift in pulse and a data shift out pulse between drivers. Each driver receives its data simultaneously and so two input signals to the column driver and a PCB trace between column drivers is eliminated. A data invert signal is not needed. In fact, aside from the WhisperBus™ data lines and clock, the only other control signal from the TCON sent to the column driver is the load data signal which determines when the outputs transition to new data on each row. Even the column driver output current can be programmed through this control interface across WhisperBus™ and additional features can be added in the future.

3.1.5 Small CD Die Size

By far the greatest advantage of the point-to-point topology with its slow data rate to the column driver is the ability to take a new approach to the column driver architecture. Virtually all column drivers in use today use the RDAC architecture in which a single resistor ladder produces a set of internal reference busses, each one being a different gray level. Each output stores a digital word that is applied to an analog switch decoder to select the correct graylevel to drive from that output. Each output requires the decoder and the voltage reference bus. These two features typically account for about 50% of the column driver die area.

In the point-to-point topology, the slower data rate to each column driver allows for a flash D-to-A conversion. In principal, only one decoder is required and the incoming digital word is converted and stored in the analog domain immediately. This saves a large amount of die space. It should be pointed out that the industry experimented with a sample and hold architecture in the past with poor results and efforts were quickly abandoned. In that case the topology was a capacitive-DAC (C-DAC) that was prone to capturing noise from digital signals in the sample and hold voltage. Here the WhisperBus™ plays an important and groundbreaking role. Because the WhisperBus™ switching is very quiet from a substrate noise perspective, the sample and hold (S&H) architecture is made practical. The S&H architecture reduces die size significantly. Moreover, there is virtually no die size difference between a 6-bit grayscale driver and an 8-bit grayscale driver. In other words, one die design serves both applications and is smaller than a conventional 6-bit die.

3.1.6 Color Temperature Control

The key reason that there is virtually no die size penalty for 8-bit over 6-bit grayscale using the S&H architecture is that there is in principal, one decoder and no busing of the RDAC reference voltages. In practice, the flash DAC rate can be made more practical by having a few DACs operating simultaneously. Still this area is small compared with the 384, 402, 420, 480 or 516 decoders for example required in the RDAC approach and is not a barrier to the architecture. On the contrary, having at least three separate RDACs allows an unprecedented feature in a column driver, independent RGB gamma control. A separate RDAC and flash decoder can be applied to each the red, green and blue channels allowing independent gamma correction of each color. This facilitates color temperature control of the LCD without a loss of grayscale or the addition of other complex backlighting methods.

It is impractical to have independent RGB using the RDAC architecture. The die size would be prohibitively large. Even if this weren't true, there isn't enough room on the input side of a conventional RDAC to support separate RGB gamma reference supplies. The ability to support independent RGB gamma across the driver interface in the point-to-point architecture is made practical by the reduction in the number of inputs to the column driver through WhisperBus™.

3.1.7 Dual Function 18- or 24-Bit Color Grayscale

The fact that the column driver is in reality an 8-bit column driver means the same chipset illustrated in Figure 4 can be used in both 18-bit and 24-bit color applications. The TCON is programmed to accept 18-bit or 24 bit data input with a pin selection and when operating in 18-bit mode the 6-bit data is scaled to 8-bits before being sent to the column driver. This scaling assures the column driver extends across the full dynamic range.

3.1.8. Growth Path

Perhaps the most important feature of WhisperBus™ and the point-to-point topology is its upward growth path. The UXGA and QXGA formats require only four data lines per CD (480 outputs) for a total of 40 data pins from the TCON. In addition the platform provides the base for additional features, including several gamma control features, which will become baseline requirements in the near future.

6. Evaluation Results

Several companies have evaluated WhisperBus™ and the point-to-point architecture successfully, in both XGA and SXGA applications. Production designs are now well underway. Naturally, one of the larger purposes for the on panel evaluation was to verify the system's EMI performance. Figure 5 is a side-by-side comparison of EMI from a conventional 6-bit XGA NBPC panel (without shielding for EMI) and the EMI signature from a 15-inch, XGA monitor panel using WhisperBus™ and the point-to-point topology with 24-bit color.

The reduced EMI is obvious when comparing these graphs. The EMI limits are shown as the thick horizontal lines in the above graphs and are well above the WhisperBus™ panel signature. The EMI from the conventional panel is significantly over the limit. Without substantial EMI filtering and shielding the conventional panel could not be brought into tolerance. However, without any additional effort, the WhisperBus™ panel performed as shown above, the first time. The baseline signature is primarily due to the LVDS residual. Further testing showed that the spikes riding on the baseline were from the clock, not the WhisperBus™ data lines. Furthermore, the clock was broadcasted not from the PCB but rather from inside the TCON. Additional effort is being made in the subsequent TCON designs to reduce clock radiation.

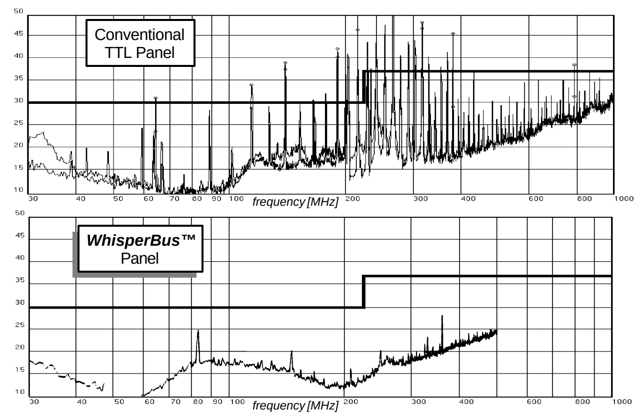

Figure 5. *Comparison of EMI signature from two XGA panels. The upper graph shows conventional TTL data busses with untreated EMI and the lo wer graph shows the results from a panel using WhisperBus™.*

The evaluations also confirmed the reduced power using the WhisperBus™ link verses a conventional, dual TTL data bus. It is a little difficult to compare power in that a TTL data bus draws no power when the image is a solid white or black field for example since power is only consumed when video data bits are transitioning. However, for practical images typical of a display, power reductions on the order of 5 to 10 times were observed. A typical TTL bus will consume about 700mW of power so a 5 to 10 times reduction in power is significant.

7. Summary

WhisperBus™ is an enabling technology to the point-to-point topology that features many improvements for the TFT display panel including reduced column driver die size, smaller PCBs, low EMI, low power and advanced features such as independent RGB gamma correction. WhisperBus™ is a unique signaling solution that allows both data and control features and demonstrates many advantages over the differential bus topologies.

8. References

[1] Kim, E. G. and Martin, R. A compact LCD Driver and Timing Controller System. SID 00 Digest, 6.3, pp. 46-49 (May 2000).

[2] Amemiya, T. Characterization of Column Driver for TFT LCD, SID 98 Digest, 45.5, pp. 1161-1164