6.2: Integrated TFT- LCD Timing Controllers With RSDS Column Driver interface

A. Lee, D.W. Lee
Interface Products, National Semiconductor Corporation

Abstract
A new generation of TFT LCD Timing controllers (TCON) are developed. This TCON offers higher levels of integration by integrating the industry de facto FPD Interface standard, LVDS receiver. In addition, This TCON provides support for multiple LCD Panel Design. This Timing Controller also features a new Column Driver interface, RSDS™, Reduce Swing Differential Signaling. Through the implementation of this high speed interface, higher resolutions at reduced EMI can be achieved. This paper will review the technical features of this new TCON, FPD87310.

Introduction
TCON (Timing Controllers) are a key element in the "make-up" of LCD modules. They are essentially the "brains", control center and the heart of a TFT LCD module. In the past and in the current generation, TCONs have been implemented through the use of fully custom ASIC devices. These custom ASICs can rarely be re-used in other LCD panel designs. Along with TCONs, discrete LVDS devices are also required for interface and control of the LCD module. A new family of highly functional (programmable) and highly integrated TCONs have now been developed which can be used on multiple LCD panel designs. They can support non-standard resolutions and different LCD panel configurations from various LCD manufacturers. These TCON offer higher levels of integration resulting in smaller PCBs outlines and lower power consumption. This higher level of integration has been achieved by integrating an on chip LVDS Receiver. In addition to the higher levels of integration, a new high speed low voltage differential interface between the TCON and CD (Column Driver) has also been developed. This new development, RSDS™ (Reduced Swing Differential Signaling) offers higher data transfer rates, enabling higher display resolutions at lower EMI.

By providing a flexible and integrated TCON platform, LCD manufacturers can use the same device on multiple LCD Panel designs, resulting in shorter develop cycles and shorter TTM (Time To Market) cycles .

Conventional TFT LCD Architecture
Typical input to a conventional TFT LCD module is through a LVDS interface. The LVDS interface is normally implemented through a discrete LVDS receiver that translates the incoming LVDS RGB data and control signals (H_{SYNC},V_{SYNC}, DE) from a Graphics controller into a TTL signal to the on board TCON. The TCON then routes and re-formats the data to Column Drivers on the TFT LCD module. From the TTL control signals, the TCON then re-generates specific control signals internal to the TFT LCD. These internal control signals are normally generated based on custom core logic within the ASIC TCON.

Data from the TCON to the Column Driver is routed via a TTL type bus. The bus, depending on the display architecture and color depth (6 or 8 bits/color) can be a single or dual bus of 18 or 24 conductors each. In conventional TFT XGA LCD architecture, the predominate bus architecture is a dual 18 conductor (36 total conductors). Since this bus utilizes TTL signals, data transfer rates for EMI and power consumption reasons, have been limited to 65 MHz or less. This limitation has been a barrier for LCD manufacturers in achieving higher resolution displays.

FPD 87310 Timing Controller
In figure 1, the major functional blocks of the National Semiconductor FPD 87310 are illustrated.

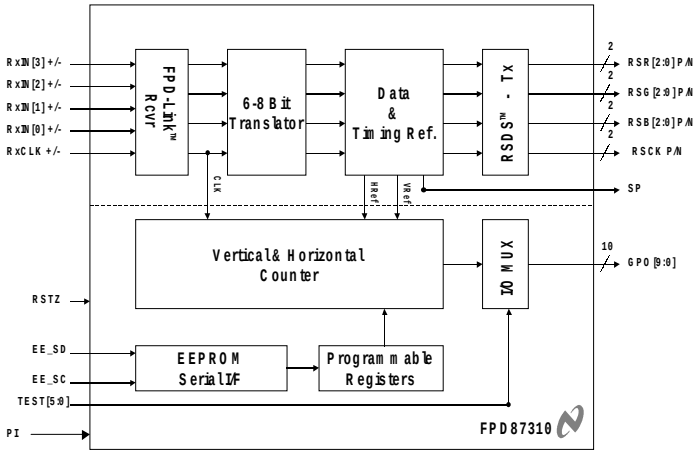

Figure 1. FPD87310 Block Diagram

Integrated LVDS Interface
The FPD87310 has an integrated FPD-Link™ LVDS Interface receiver. The LVDS receiver is capable of receiving serialized 24 bits (8 bits/color) of RGB data, Clock and control signals from a host graphics controller. The typical rated input Clock frequency is 65 MHz for XGA resolutions and higher. The LVDS receiver core will translate the incoming serialized LVDS input to a TTL signal. The TTL signals are then routed to the TCON core logic. The integrated LVDS receiver results in reduced components, small foot print and thereby resulting in the reduction of component cost and power consumption.

Timing Controller Logic Core

The TCON core consists of a programmable logic blocks for receiving and further processing the TTL Data and control signals. Several types of input control signal formats can be selected:

1. Fixed Vertical/ Fixed Horizontal
2. Data Enable Only
3. Vertical/Horizontal/Data Enable

For inputs consisting of 8 bits/color data, a 8-6 bit Translator core will truncate the color depth down to 6 bits/color by one of two user selectable methods;

1. Truncation of the 2 LSBs
2. Time Multiplexed Dithering technique for generating pseudo 8 bits of color.

The 6 bits/color data is then sent to a RSDS transmitter core which then serializes and converts the TTL level data to a differential level stream for receipt by a RSDS compatible Column Driver such as a Samsung KS066 or a Sharp LH168M.

Internal Control Signals such as GCLK (Gate Driver Clock), Rev, POL (CD Polarity control), LS (CD Latch input) can be generated through 10 programmable GPO (General Purpose Outputs). The GPO's are programmed through 4 register values:

1. Vertical Start : line increments
2. Vertical Duration: line increments
3. Horizontal Start: pixel or clock increments
4. Horizontal Duration: pixel or clock increments

Through the use of these 4 parameters, control signals can be generated anywhere within one frame time of the incoming video/graphics input.

During system design and development, these register values can be altered and verified through the use of an external EEPROM and through an integrated I^2C serial interface. This serial interface is also compliant to VESA DDC(Display Data Channel) and is capable of supplying VESA EDID or Parametric Display interface information.

By it's programmable nature, the FPD87310 TCON offers display manufacturers a unique flexibility. The FPD87310 supports today's standard XGA format. In addition, it can also support newer and non-standard display formats such as Half-XGA (1024 x 480), SVGAW (1024 x 600), XGAW (1280 x 768) and WXGA (1152 x 768).

What is RSDS ?

Reduced Swing Differential Signaling, like it's predecessor LVDS (Low Voltage Differential Signal), originated from the LCD Manufacturer's unique need for on glass interface with higher speeds, reduced interconnect, lower power, and a lower EMI. Thus RSDS and LVDS are similar except in their intended application.

Since this new technology also uses a low voltage differential swing (+/-200 mV), lower EMI, and lower power consumption can also be realized. Unlike LVDS (see Table 1), which utilizes a 7:1 serialization scheme, RSDS instead uses a 2:1 serialization scheme, which results in a less complex and lower power consumption receiver architecture.

Table 1. RSDS and LVDS

Characteristics	RSDS	LVDS
V_{OD} , Output Voltage Swing	+/- 200 mV	+/- 350 mV
R_{TERM}, Termination	100 Ω	100 Ω
I_{OD}, Output Drive Current	2 mA	3.5 mA
Data Mux	2:1	7:1
Content	RGB Data	RGB Data and Control
Application	Intra-system interface	System-System interface

.

Due to it's low voltage swing (versus TTL), faster clock rates can be achieved and thereby enabling higher resolution TFT LCDs in the future. At present clock rates of 65 MHz have been EMI qualified in pre-production TFT LCD modules with relative ease when compared to their TTL counter parts. In the near future, we can expect higher clock rates in excess of 85 MHz or even 100 MHz plus.

Since this interface is a serial interface, overall bus width is also reduced by half of the conventional TTL bus architecture. In a TTL 6 bit/color dual bus architecture, a total of 36 data lines plus 2 clock signals are required, for a total of 38 conductors. In an equivalent RSDS architecture, only one bus consisting of a total of 9 differential pairs of data lines plus a differential clock pair are required, for a total of 20 conductors. When implementing the same system with RSDS, an overall reduction of 47 % in bus conductors are achieved thereby enabling a small outline PCBs within the TFT LCD module.

Conclusion

The FPD87310 with the enabling RSDS™ technology (figure 2) offers a complete display solution for tackling the challenge for higher resolutions with lower EMI. The FPD 87310 is the first of a new family of "Off the shelf" and highly Functional TCONs that offers a compelling solution to all LCD manufacturers in their frantic pace to develop multiple new products in the ever shortening "Time To Market" window.

References

[1] National Semiconductor FPD 87310 Data Sheet.

[2] T. Blankenship, C. Ludden, "Reducing EMI and Power in Flat Panel Display Systems" SID 96 Applications Digest, Volume XXVII, p.81 – p.83

[3] Samsung Semiconductor KS0666, RSDS Column Driver Data Sheet, Rev. 0.0, August 1999.

[4] Sharp Corporation LH168M, RSDS Column Driver Data Sheet.

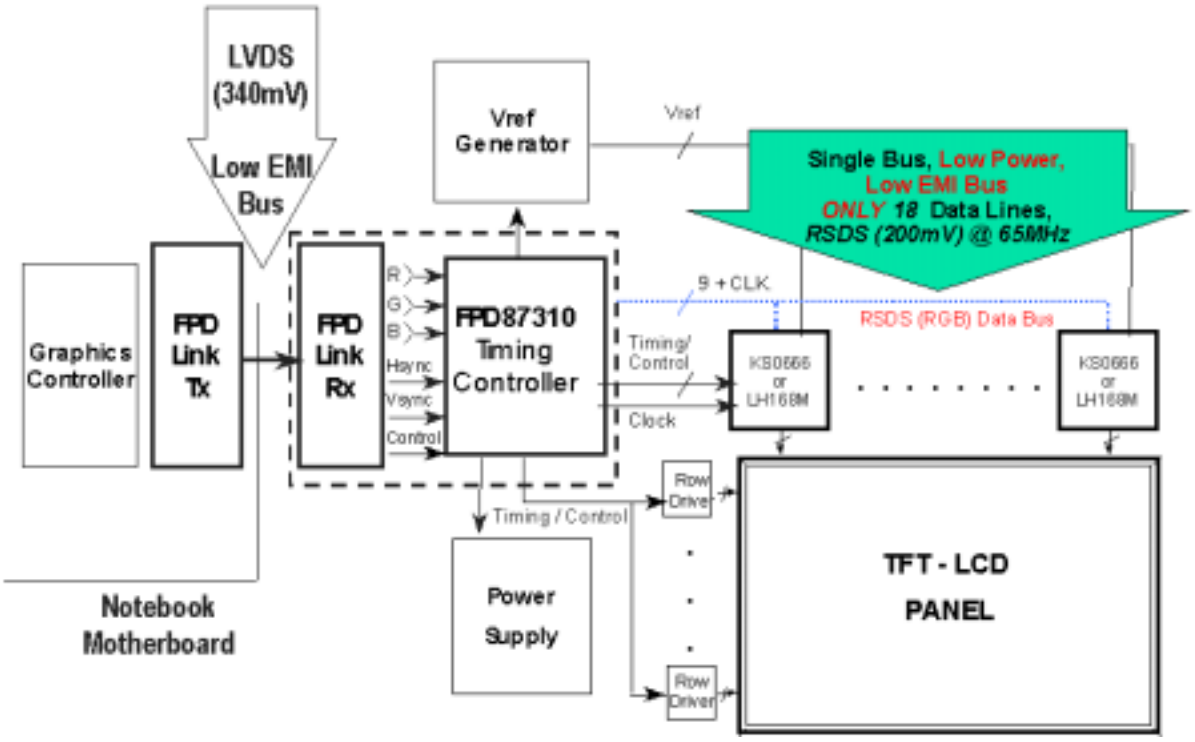

Figure 2. Typical RSDS Architecture