September 2000
Die Products Business Unit

Die Products Applications Note
Chip-on-Board and Flip Chip Assembly

Contents

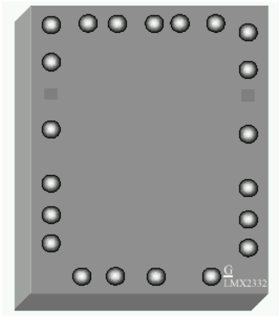
Introduction to Die Products

A die product is the unpackaged silicon die utilized in lieu of the package product version. The most frequently mentioned reasons for die product design-ins are to achieve improved miniaturization, better device performance and a higher level of functional integration. Each of these reasons create added value in the end product application utilizing die product. These applications include those with single die such as watches, calculators and smart cards as well as leading edge multiple die applications like cellular handsets and digital cameras. Better device performance utilizing die show up in processor modules for computers, workstations and servers as well as switcher/routers and telecommunications infrastructure. Functional integration of die products most commonly shows up where conflicting device processes such as analog, high frequency or clock rate combine with complex digital and/or memory to create innovative product capabilities.

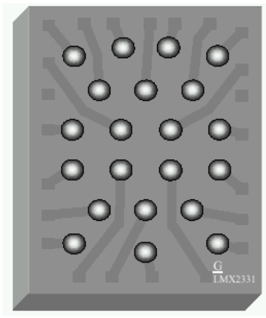
Regardless of design motivation, whether manufacturing, product compatibility, time to market or cost savings, die products provide the fundamental value and justification for use. Consumers buy electronics products today so they can be more productive and increase the quality of their lives. The mantra of the electronics industry resounds with “smaller, lighter, faster, smarter” at continuously decreasing cost with reliability matched to application life expectancy. This makes portability and functionality the first measure of convenience and value. Die products provide the ultimate opportunity for size and weight reduction, speed and functionality increases in portable applications.

With complex silicon and “system on chip” design cycles averaging 14 to 18 months or more and coupled with the needed 6 to 9 month design cycle for consumer products, die is a design avenue to bridge the gap. Die utilization accelerates the time-to-market while taking advantage of chip performance

Die Product Layout Configuration



Peripheral Pads



Area Array Pads

enhancements. The higher available margins resulting from early time to market is frequently increased even further through the cost savings resulting from PWB simplification. Using die product modules to displace high density interconnection demands on the whole PWB further benefits the design and cost.

National Semiconductor offers die products in several formats for various methods of assembly interconnect to the substrate. Die products are available with standard bond pads for wirebond implementation in Chip-on-Board (COB) applications and with eutectic solder bumps for reflow implementation in Flipchip applications. Wirebondable die are available with peripheral bond pad layout, bumped die are available in both peripheral and array layouts. The use of either COB or Flipchip is dictated based on a variety design, manufacturing and application specific variables.

Layout Variations

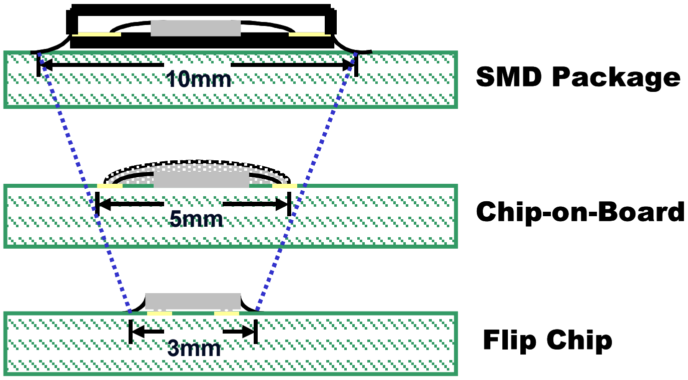
Traditionally die products have been designed with a peripheral bond pad configuration. This layout provides easy access for wire bonding of the die to the substrate. This is the preferred configuration for Chip-on-Board assemblies. The bond pad pitch can vary from die to die in the peripheral configuration. The pitch on the die is determined based on optimum die area required for the function and the number of I/O pads needed to access the functions external connections.

Die products are also available in array formats. These formats also allow for function size optimization but provide greater pad pitch or distance between the pads. This provides benefits for flip chip attachment applications but usually proves more problematic in wire bond applications due to the staggering of the pads.

The use of peripheral or array layout format must be analyzed for each application based on assembly, design, substrate materials and processing constraints. Interconnect methods for wirebonding include gold-ball bonding and aluminum wedge bonding. Gold-ball bonding is a high throughput, high strength technology that allows for bonding of fine pitch bond pads. It does require an elevated temperature to bond and the gold wire results in higher material costs than aluminum wedge. Process consideration must be given to the set up conditions, wire diameter, wire length, metallurgy and surface conditions. Aluminum wedge bonding can be processed at room temperature and utilizes lower cost wire. Lower bond strength and lower throughput should be expected. Additional process consideration should be given to wire bond angles and forward/reverse bonding effects.

National Semiconductor die products are available with eutectic solder bumps for flip chip applications. Flip chip implementation provides lowest weight, the smallest footprint possible and maximizes electrical performance. High density substrates are required to take full advantage of flip chip assembly. Flip chip can improve system reliability and increase manufacturing throughput. Consideration should be given to the need for underfill, thermal hierarchy, reflow profile, die placement accuracy, metallurgy of the bump/UBM structure and all material CTE matching.

Footprint Comparison of Assembly Options



Implementation Formats

Chip-on-Board (COB)

Chip-on-board or chip-on-substrate assembly technology relies on widely available die attach and wire bond infrastructure to ensure highly reliable interconnection between the die and substrate. Assembly yields near 100% combined with the relative ease of rework and repair enhance designer confidence in both manufacturability and cost predictability. Software based programmable tooling of the chip and wire process simplifies engineering changes, particularly in wiring patterns, and provides relative immunity to redesign due to die design shrinks. COB provides the capability to perform direct chip to chip wiring that facilitates improved performance and strong functional integration in many modern high speed applications.

The variety of substrates available for COB applications allows for a wide selection of electrical, thermal and mechanical properties tailored to specific circuit requirements. Ceramic and glass ceramic substrates offer stable dielectric constant, low dielectric loss tangent and good thermal dissipation. Organic substrates can provide low dielectric constant, lighter weight and in many cases, lower cost. Ease of design, technology availability and time to market make COB the preferred choice for a high proportion of today's integration and performance module applications.

The COB assembly process flow consists of three essential steps; die attach, wire bond and encapsulation. Die attach provides mechanical adhesion of the chip to the intended substrate and requires an adhesive application followed by precision chip placement then curing of the adhesive. Once firmly in place the wire bond processing electrically connects the die bond pads to the associated wiring pattern on the substrate. The wire bond machine welds fine wires, typically of Al or Au, between each pad on the chip and the appropriate pad on the substrate. Wire bonding demands clean pads on both the chip and the substrate to ensure strong bonds as well as high production yields. Finally, encapsulation protects the die and bond wires from mechanical damage during handling and additional processing. In some cases, particularly for system in package applications, the encapsulation also provides the finished surface for component marking. Encapsulation employs either liquid dispensing or transfer molding depending on the specific application.

Designing a COB assembly process sequence can be critical, particularly for applications where die products and surface mount (SMT) components are combined on a single substrate. In principle, the COB process may either precede or follow the SMT assembly process. Generally however, SMT processing first provides a simpler process flow particularly if the COB process employs a good cleaning process. A process step such as plasma cleaning to prepare the bonding surfaces is recommended. Process characteristics and considerations for COB assembly are detailed below and provide specific information for understanding, selecting and specifying the COB process.

Die Attachment

Die attach adhesive provides both the thermal and mechanical interface between the die and the substrate. Although the adhesive is applicable to either the substrate or the back of the die, most manufacturers employ paste adhesives applied to the substrate. Dispensing, stencil printing or pin transfer may be used depending on die size. Most utilize dispensing except for film type adhesive. Dispense patterns depend on die size and shape but all must ensure a void free bond line. For high thermal transfer applications, a thin bond line combined with silver (Ag) filled epoxies can meet the need.

Die Placement

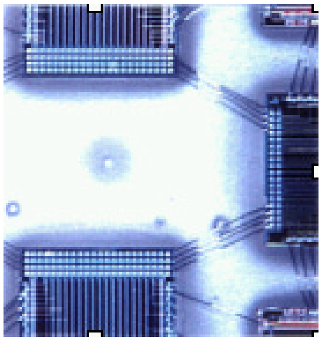
Die placement into the dispensed adhesive demands accuracy as well as proper orientation and planarity control. Over pressure to set the die into the adhesive will ensure good adhesion and establishes the bond line thickness. Orientation and accuracy of placement directly impact the bond pad to substrate wire length and the "keep out" or die spacing requirements.

Clean

Following die placement, adhesive curing exposes bond pads on both the die and the substrate to organic contamination by plasticizers and curing agents in the adhesive; this is particularly true when employing organic substrates. Plasma cleaning provides the best alternative, although solvent cleaning with ultrasonic assist and CO_2 snow blasting find application as well. Removal of any organic contamination from the bond pad surfaces ensures high wire bond yield and strength as well as process stability and reliability.

Wire Bond

Thermo-sonic Au or Cu ball bonding or thermo-compression Al wedge bonding may be employed. Au ball bonding provides the highest throughput and excellent wire loop flexibility. A process temperature of 170°C for Au ball bonding may be a disadvantage when die I/O counts on a substrate exceed 600 - 700, particularly for temperature sensitive die. However, low pressure and time requirements reduce the exposure to potential die passivation damage when using Au ball bonding. Combined with plasma cleaning after die attach, Au ball bonding minimizes ultrasonic energy and provides very consistent bond strength.



Die to die wire bonding

Al thermo-compression wedge bonding offers room temperature bonding capability and minimal bond wire loop height. This low loop capability gives Al wedge bonding an advantage in direct die to die bonding. Bonding at room temperature requires higher pressures and ultrasonic energy levels, which can cause problems with mechanically sensitive die. Alumina (Al_2O_3) scrubbing of the bonding surfaces reduces Al wedge bonding sensitivity to organic contamination in comparison to Au ball bonding.

Encapsulation

Either liquid encapsulation or transfer molding may provide the physical protection for the die. For high volume applications as well as those that can be fit into standardized mold cavities, transfer molding provides the lower cost alternative. Transfer molding also ensures consistent surfaces for marking. Larger modules and die mounted to large, mixed technology substrates generally demand liquid encapsulation. Liquid encapsulants come in two types, silicone or epoxy based. Silicone systems offer excellent moisture resistance and high compliance, but remain difficult to mark and difficult to handle. Epoxy systems provide improved adhesion and marking relative to silicone as well as more consistent appearance and require smaller “keep outs” or die spacing specifications.

Marking

Laser, ink jet, stencil or stamp marking techniques may be employed although laser and ink jet simplify serialization of parts. Key factors include permanence, visibility and contrast. For silicone based liquid encapsulants laser marking works best. With epoxy liquid encapsulants and mold compounds ink based marking with either ink jets or pin printing provide maximum clarity and contrast.

Key Process and Design Issues

In COB assembly various design, process and manufacturing issues play a key role in guaranteeing high yielding, high reliability product. During implementation and processing many problems can be avoided by giving attention upfront to some common pitfalls. This section describes some simplistic but important sources of manufacturing difficulties that can be easily avoided.

- Thick die result in tall wire loops in COB applications. This increases component spacing requirements and “keep out” size.

Solution: Use die thinned to 400 microns or less.

- Failure to perform a thorough clean following die attach cure not only reduces yields, but significantly reduces mechanical reliability of wire bonds.
  Solution: Incorporate a clean step or use suppliers with post die attach cleaning capability. Plasma cleaning methods are preferred.
- Liquid encapsulation increases risk of wire loop exposure.
  Solution: Specify epoxy based materials when liquid encapsulation is required.
- High I/O counts can force long wire bonds (> 2500 microns) increasing susceptibility to wire wash or wire sag during encapsulation.
  Solution: Use higher strength wire alloys when bond wires exceed 2500 microns in length.

Design Guidelines

Many design rules depend on the manufacturer's equipment and process capabilities. Those presented here represent nominal capabilities industry wide. If there is a need to violate any of these guidelines be certain you work with your assembler as early in the design phase as possible to avoid major cost and quality implications.

- Keep Outs
  Function of die geometry, I/O count and substrate pitch limitations.
- Escape Routing
  Since bond pads are peripheral, only fan out required.
- Bond Line
  10 - 75 microns typical. Die attach cured adhesive thickness specification impacts thermal transfer as well as attachment strength.
- Pad Size/Geometry
  Width = 100 microns (typical)
  Length = 100 - 150 microns (typical), function of I/O count, die size and rework requirements.
  Rounded corners may enhance reliability (pad adhesion to substrate).
- Pad Finish
  Au ball bond: >50 micro-inch Ni, >40 micro-inch Au
  Al wedge bond: >50 micro-inch Ni, 8-10 micro-inch Au
  Pd or Ag may replace Au in certain situations
- Electrical Properties (typical values)
  Au
  R = 0.03 Ohms
  C = 0.006 pF
  L = 0.65nH
  Al
  R = 0.035 Ohms
  C = 0.0006pF
  L = 0.65nH
- Wire Length

	Au	Al
Wire bond length (max)	2500 microns	3000 microns
Bond diameter (ball)	2 - 4x wire diameter	N/A
Bond length (wedge)	3 - 5x wire diameter	2x wire diameter
Bond width (wedge)	1.5 - 2.5x wire diameter	1.2 - 2x wire diameter
Wire diameter (typical)	25 microns	25 microns
Pitch (typical min)	100 microns	140 microns

Substrates

Substrate selection, particularly for system in package applications, control a great many aspects of a successful COB design. These include thermal management options, electrical performance, mechanical integrity and long term reliability. The table below presents several important properties of various substrate alternatives, most of which demand consideration in the design phase and have important impacts on cost and manufacturability as well.

Substrate Properties	FR-4	Polyimide	Ceramic/Glass
Dielectric Constant (1 MHz)	4.0 – 5.5	4.0 – 5.0	5.0 – 9.5
Dielectric Loss Tangent (1 MHz)	0.02 – 0.03	0.01 – 0.015	0.00015 – 0.0002
Coefficient of Thermal Expansion (ppm/°K)	17 - 22	14 - 16	3.0 – 6.6
Thermal Conductivity (W/m °K)	0.2	0.2	18 - 20
Moisture Absorption (%)	0.3	0.15 – 0.4	~0
Line/Space Geometries (microns, typical)	100/100	75/75	100/100

Implementation Formats

Flip Chip

Flip chip assembly offers optimized electrical performance in addition to optimized miniaturization. Die in flip chip format also demonstrates extremely high assembly yields, resulting mostly from the self alignment properties of the reflow process. However, the opportunity to control signal integrity from the die through the substrate to other die on the substrate or even packaged die on the substrate may provide the most significant benefit of flip chip assemblies.

The variety of substrates available for Flip Chip applications allows a wide selection of electrical, thermal, CTE and mechanical properties tailored to specific application requirements. Ceramics and glass ceramics offer stable dielectric constant, low dielectric loss tangent and good thermal dissipation. Organic substrates can provide low dielectric constant and light weight as well as, in many cases, low cost.

The Flip Chip assembly process flow consists of four essential steps; die bumping, die attach, interconnect and underfill. Bumping is generally provided by either the die supplier or a contract bumping house. Die attach and interconnect provides the mechanical and electrical connection of the die to the substrate and wiring pattern on the substrate simultaneously. The surface tension of molten solder wetting the pad on the substrate provides self alignment between the bumps on the die and the land pads on the substrate. The die placement must ensure at least 30 – 50 % overlap of the appropriate substrate pad by the correct bump on the die. Flip Chip bonding requires a flux application to pads on the substrate in order to ensure strong bonds as well as high production yields. Particular process characteristics and considerations for Flip Chip assembly detailed below should prove helpful in understanding how to select and specify product applications.

Solder Flux

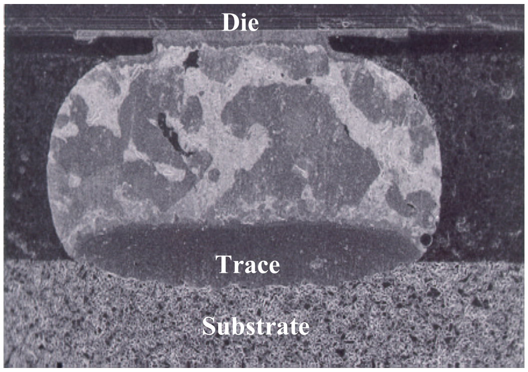
The variety of techniques for fluxing include dipping the solder bumps into the flux as well as stencil printing, pin transfer and flood or spray coating of the substrate. Precision application (dip, stencil, pin transfer) are preferred to minimize residue and cleaning challenges.

Die Placement

Due to the self alignment characteristics of solder, a bump pitch of 200-225 microns only demands placement accuracy of ± 75-125 microns and ± 1 degree rotation. This compares to a placement accuracy requirement of ± 40 microns for 0.4 mm pitch QFPs or ± 50 microns for 0.5 mm pitch CSPs.

Reflow

Conduction or vapor phase reflow provides optimum process control and ultimate solder joint consistency and reliability. However, more commonly available infrared and convection reflow equipment leads to more widespread application of these techniques. As with surface mount reflow, even temperature distribution and controlled temperature ramping, both up and down are critical to yield and quality.



Flip chip eutectic solder bump reflow to substrate

Underfill

Underfill enhances thermal and mechanical vibration fatigue reliability as well as mechanical shock resistance of the flip chip solder joints. Most underfill application relies on capillary flow demanding well controlled materials properties including viscosity and adhesion as well as the cured state properties of thermal transfer, coefficient of thermal expansion and mechanical strength.

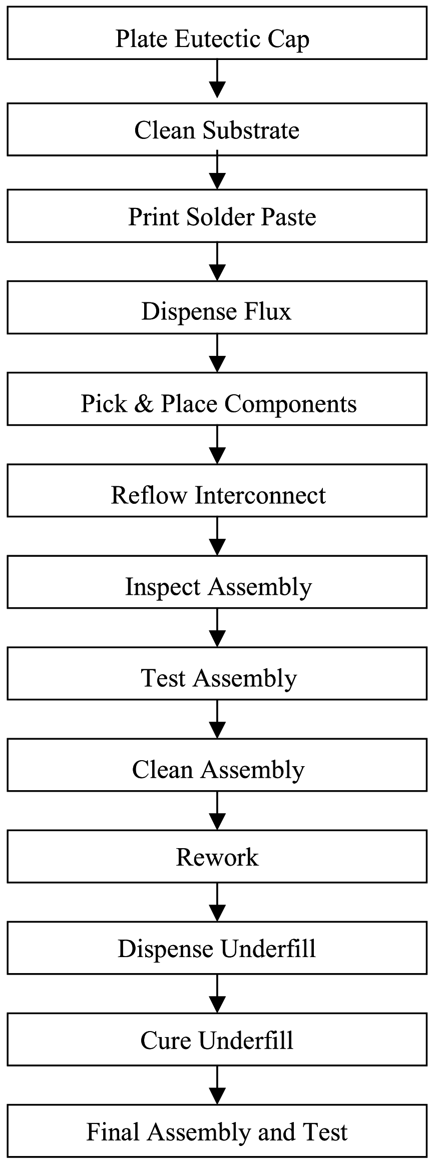
Encapsulation
Either liquid encapsulation or transfer molding may provide the physical protection for the die. For high volume applications as well as those which can be fit into standardized mold cavities, transfer molding provides the lower cost alternative. Transfer molding also ensures consistent surfaces for marking. Larger modules and die mounted to large, mixed technology substrates generally demand liquid encapsulation. Liquid encapsulants come in two types, silicone or epoxy based. Silicone systems offer excellent moisture resistance and high compliance, but remain difficult to mark and difficult to handle. Epoxy systems provide improved adhesion and marking relative to silicone as well as more consistent appearance and smaller "keep outs" or die spacing specifications.

Marking
Laser, ink jet, stencil or stamp marking techniques may be employed although laser and ink jet simplify serialization of parts. Key factors include permanence, visibility and contrast. For silicone based liquid encapsulants laser marking works best. With epoxy liquid encapsulants and mold compounds ink based marking with either ink jets or pin printing provide maximum clarity and contrast.

Key Process and Design Issues
In Flip Chip assembly various design, process and manufacturing issues play a key role in guaranteeing high yield, high reliability product. During implementation and processing many problems can be avoided by giving attention to some common pitfalls. This section describes some simplistic but important sources of manufacturing difficulties that can easily be avoided.

- Smaller bumps provide tighter pitch and routing density but provide less stress relief due to mechanical stress and CTE mismatch.
Solution: Utilize underfills that match the die standoff height and bump to bump spacing to maximize flow rate and coverage.

Typical Flip Chip Attach Process Flow



- During initial manufacture of the substrate assembly opens and shorts testing is difficult to manage with live die causing debug difficulties.
Solution: Utilize die daisychains to debug manufacturing process.

- All eutectic solder bumps are not the same. Variations may cause yield and reliability problems.
Solution: Work with the supplier to understand the UBM, materials and solder bump buildup.

- Substrates utilizing eutectic bumped die and other SMT devices require various thermal processing.
Solution: Understand and design a process flow that considers the thermal hierarchy of the total substrate solution to guarantee yields and reliability.

- All components used in an application typically do not have uniform placement tolerances or I/O density, therefore requirements may vary.
Solution: Understand variants and partition the system accordingly.

Design Guidelines
Many design rules depend on the specific equipment and process capabilities utilized. The guidelines presented here represent what we feel are nominal capabilities industry wide. If these guidelines are violated be certain to work with your assembler and suppliers as early in the design phase as possible to avoid major manufacturing, cost and quality implications.

Keep Outs
2500 microns typical.

Escape Routing
Peripheral or peripheral array layouts simplify escape routing reducing internal redistribution and routing through vias or through holes on other layers in the substrate. The number of routing layers may increase significantly with area array layouts.

Bond Line
Generally controlled by bump height following reflow. 125-250 microns typical.

Pad Size/Geometry
Width/Length = 75-100 microns (typical)

Pad Finish
8-10 micro-inch Au for most applications
Electrical Properties (typical values)
R = 0.002 ohms
C = 0.001 pF
L = 0.2 nH

Substrates
Substrate selection, particularly for system in package applications, control a great many aspects of a successful Flip Chip design. These include thermal management options, electrical performance, mechanical integrity and long term reliability. The table below presents several important properties of various substrate alternatives, most of which demand consideration in the design phase and have important impacts on cost and manufacturability as well.

Substrate Properties	FR-4	Polyimide	Ceramic/Glass
Dielectric Constant (1 MHz)	4.0 – 5.5	4.0 – 5.0	5.0 – 9.5
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Thermal Conductivity (W/m ^{o}K)	0.2	0.2	18 - 20
Moisture Absorption (%)	0.3	0.15 – 0.4	~0
Line/Space Geometries (microns, typical)	100/100	75/75	100/100

Die Product Assembly Options

A wide variety of die assembly methods are available for implementation into high yeild, high reliability systems. Some of the options are reviewed here for comparison.

Die Attach Methods for COB

- Thermoset Adhesive
  - ⇒ Advantages: low cure temperature, low modulus of elasticity, high strength, relatively inexpensive, wide process window (bondline, curetime)
  - ⇒ Disadvantages: resin bleed, level of thermal/electrical conductivity, limited reworkability, limited internal wafer vapor (RGA) performance
  - ⇒ Process Considerations: cure profile, bleedout evaluation, material compatibility, design rules, pot life and storage, dispensing considerations/patterns/voiding, bondline control, placement accuracy/planarity

- Thermoplastic Adhesive
  - ⇒ Advantages: low cure temperature, low modulus of elasticity, relatively inexpensive, reworkable
  - ⇒ Disadvantages: limited strength, electrical/thermal conductivity, limited internal water vapor (RGA) performance, manufacturing logistics in handling
  - ⇒ Process Considerations: force, time, pressure, placement accuracy/planarity/bondline, thermal heirarchy

- Metal-Filled Glass
  - ⇒ Advantages: high thermal/electrical conductivity, high temperature tolerance, excellent internal water vapor performance (RGA), strength, mid-range modulus of elasticity
  - ⇒ Disadvantages: bond line control, cost, non-reworkable, fillet control, die size limitations, high temperature organic burn-out
  - ⇒ Process Considerations: bond line control, OBO profile, dispense control/voiding, placement accuracy, die size, metallurgy of die backside

- Au-Si Eutectic
  - ⇒ Advantages: high thermal/electrical performance, strength, RGA, temperature tolerance, reworkable
  - ⇒ Disadvantages: cost, high modulus of elasticity, limited die size, potential for chip damage, high process temperature, narrow process window
  - ⇒ Process Considerations: process profile, environment (N_2, forming gas), die size, metallurgy(type & oxidation), voiding, collet size/design

- Soft Solder
  - ⇒ Advantages: good thermal/electrical performance, reworkable, good matching for dissimilar CTE's
  - ⇒ Disadvantages: special backside metalization required, typically need forming gas and nitrogen atmosphere, die placement issues
  - ⇒ Process Considerations: level of O_2 in atmosphere, oxidation on surfaces, solder splash during placement, voiding

Interconnect Methods for COB

- Gold-Ball Bond
  - ⇒ Advantages: high throughput, high strength, omni-directional, fine pitch
  - ⇒ Disadvantages: elevated temperature, increased material cost, intermetallic potential
  - ⇒ Process Considerations: temperature, power, force, time, wire diameter, wire length, metallurgy, pitch, bonding surface conditions, bonding area

- Aluminum Wedge Bond
  - ⇒ Advantages: room temperature processing, lower material cost (wire), fine pitch
  - ⇒ Disadvantages: Strength, throughput, not optimum for non-hermetric applications
  - ⇒ Process Considerations: power, force, time, wire diameter, wire length, metallurgy, pitch, bond angle, forward/reverse bonding, bonding surface conditions, bonding area

Interconnect Methods for Flip Chip

- Eutectic Solder
  - ⇒ Advantages: electrical performance, smallest footprint, reworkable, reliability
  - ⇒ Disadvantages: underfill, high density PWB required, infrastructure
  - ⇒ Process Considerations: reflow profile, underfill approach, placement accuracy, bump/UBM metallurgy, substrate design and materials, CTE, thermal hierarchy

Seal and Encapsulation Methods

- Hermetic – Seam Seal
  - ⇒ Advantages: hermetic, low temperature, large seal area, low profile, minimal floor space requirements
  - ⇒ Disadvantages: low throughput
  - ⇒ Process Considerations: dry box environment, electrode design, lid design

- Non-Hermetic – Glob Top

⇒ Advantages: flexible, low temperature, low stress, low profile

⇒ Disadvantages: non-hermetic, limited protection, spread, wire wash potential

⇒ Process Considerations: dispensing parameters, viscosity, dams, cure

Reduce Switching Noise with Direct Chip Attach (DCA) Technologies of COB and Flip Chip

In a high speed digital system the ability to reduce "switching noise" is critical for the proper functioning of the system. Switching noise can be thought of as any disturbance that erodes either the logic "1" or logic "0" levels. Digital devices are designed with built in noise margins. Noise margin is the difference between worst case output signal level from a driver and the minimum signal necessary to insure that an input always makes a correct determination of the logic state being transmitted. Since all the signals on a device are referenced to the device/system ground potential, it is critical that this ground potential be maintained. Two factors that influence the stability of the ground potential are the amount of current per unit time flowing into ground and the inductance of the device ground lead(s). While the amount of current per unit time flowing into ground is determined by the design of the device, lead inductance is a function of the packaging technology. Direct Chip Attach (Flip-Chip and Chip-On-Board) provides system designers with a low inductance option.

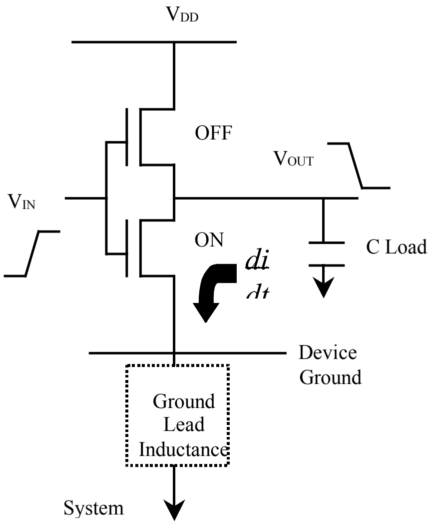


Fig 1. Simple CMOS Driver

Inductance is a characteristic of a storage device that resists a change in current. In this case, the storage device is the ground lead of the IC. The unit for inductance is a Henry. Inductances associated with the digital IC world are usually in the nano-Henry (10^{-9} Henry) range. The interaction between the current flowing per unit time and the inductance of the device ground lead results in a voltage being developed. This noise voltage potential (V_N) developed across the inductance (L) due to the current per unit time (di/dt) flowing through the inductance can be calculated by:

$$V_N = L\ di/dt \quad \text{(Eq. 1.)}$$

A simple analysis of a CMOS output driver (Fig. 1) will illustrate this effect. With the output, V_{OUT}, switching from HIGH to LOW (V_{IN} switching LOW to HIGH) the pulldown transistor would be ON and sinking current to system ground through the device ground lead. Assuming a large capacitive load (100pF) and a fast edge rate (1ns) on V_{IN} for this output driver, V_{OUT} would equal V_{DD} (5V) during the transition time.

Rewriting Eq. 1:

$$V_N = L * (I_{MAX}/T) \quad \text{Eq. 2}$$

where

$$I_{MAX} = K(V_{IN}-V_T)^2/2 \quad \text{Eq. 3,}$$

V_T is threshold voltage and K is a function of the device geometry and fabrication process. Letting $K = 21.4 \times 10^{-3}$ Amps/V^2, $V_{IN} = 5V$, and $V_T = 1V$, and substituting into Eq. 3, $I_{MAX} = 0.171$ amps. Substituting I_{MAX} into Eq. 2 and assuming T = 1 nanosecond:

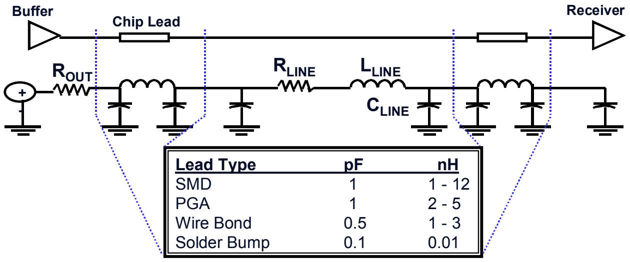
$$V_N = L\ (0.171\ \text{Amps/1ns}) \quad \text{Eq. 4.}$$

Table 1. Calculated V_N by Package

Package	L (nH)	V_N (Volt)
DIP	12.0	2.05
QFP	7.0	1.19
BGA	5.0	0.86
COB	2.6	0.44
µBGA	2.1	0.36
Flip-Chip	<0.1	0.01

From Eq. 4 it can be seen that the noise generated is directly proportional to the inductance L. Table 1 lists lead inductances and calculated (per Eq. 4) noise voltages for some common packages and Direct Chip Attach (COB, Flip-Chip) technologies. Keep in mind that Eq. 4 is for one driver only. If multiple drivers are switching resulting in more current flowing through the device ground lead(s), the resulting noise voltage will increase. Since Flip-Chip has the shortest device lead (bump) and thus the lowest lead inductance versus other package technologies, one will get better system performance regarding switching noise by using this method of DCA versus other packaging options.

Lump Interconnect Equivalent Model



Lead Type	pF	nH
SMD	1	1 - 12
PGA	1	2 - 5
Wire Bond	0.5	1 - 3
Solder Bump	0.1	0.01

Handling and Use of Die Products

Die Products have been singulated and assembled into individual packages for over 35 years. During this time standardized and formalized processes have been developed to insure that highly reliable product was assembled. The use of die products in applications previously populated by packaged product requires that consideration be given to the die product since its format is different than the typical packaged product. While die products are robust in the proper assembly environment, improper handling can result in unreliable assemblies. In utilizing die products consideration must be given to:

- **Foreign Material**: among the most common are skin, hair, spittle, cosmetics, dust, dirt, fingerprints, airborne particles, machine oils and friction by-products
    - ⇒ Impact of foreign material: among the effects observed are electrical leakage, electrical shorts, latent failures, visual defects and corrosion.
    - ⇒ Techniques for control during processing include: air filtration, cleanroom smocks, face masks, gloves, hairnets, work area hoods, equipment maintenance, housekeeping and employee training.

- **ESD**: electrostatic discharge can have the same effects on die products as those experienced with packaged devices.
    - ⇒ Typical failure modes: state or level upset effects, immediate device breakdown, cumulative degradation from repeated exposure and latent damage causing subsequent failure.
    - ⇒ Techniques for control during processing: humidity of 30% to 60%, use of conductive or static dissipative materials, use of ionizers, conductive paths to ground for personnel and work surfaces, and employee training.

- **Die Product Packaging**: The various packaging options utilized are based on their ability to protect die during transit.
    - ⇒ The consideration that should be given when selecting from the various shipping mediums include: cost of use, level of automation, die orientation requirements, contamination potential, processing ease, multiple supplier commonality, equipment interface capability, inventory and storage control, resealibility and mechanical protection.

- **Specific Product Related Information**: this information is available from individual Die Product datasheets.

Die Tape on Reel Format

The continued growth of the bare die (COB) and bumped die (flip-chip) market has included an increasing segment of high volume applications (e.g. telecommunications, automotive, computers). Because of tape on reel's proven characteristics of low cost and high-speed manufacturing, National Semiconductor's Die Products customers in these markets are increasingly requesting die products to be packed in tape on reel.

Customers are given a competitive advantage through the speed and efficiency that tape on reel provides. Carrier tape offers the electrical and mechanical protection of our other shipping media and additionally provides the customer with large die quantities on a single reel for greater efficiency. In fact, a single 13 inch reel may hold up to 24,000 die. Tape on reel also offers the advantage of quickly presenting to the assembly machine a die that is always oriented and in position. No need for the machine to waste time searching for the part or determining proper orientation. Reels, when used in a cassette format, may be plugged into or removed from an assembly machine in banks allowing quick reconfigurations.

All die products are available in tape on reel and customers have the option of 7 inch or 13 inch diameter reels. There are two types of carrier tape available; embossed tape (figure 1), and adhesive assisted tape (figure 2). Both carrier tapes are available in 8mm, 12mm, 16mm, and 32mm widths (the tape width used is determined by die size). Embossed tape utilizes a close tolerance pocket to protect the die and maintain position. To keep the die in the pocket, a continuous strip of clear cover tape is applied to the top of the carrier tape as the die is placed. The cover tape is held in position by a pressure sensitive adhesive along the edges.

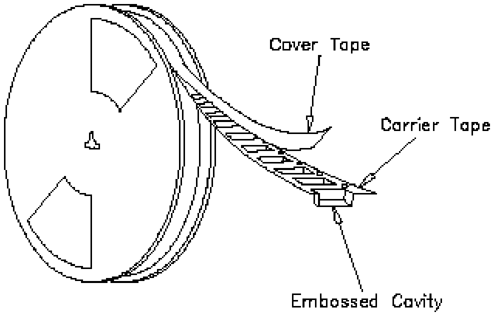


Figure 1

The adhesive assisted carrier tape utilizes a punched cavity opening with pressure sensitive adhesive at the bottom to hold the die in place. The pressure sensitive adhesive is actually a strip on each side of the cavity bottom, which provides a gap for push pin removal of the die.

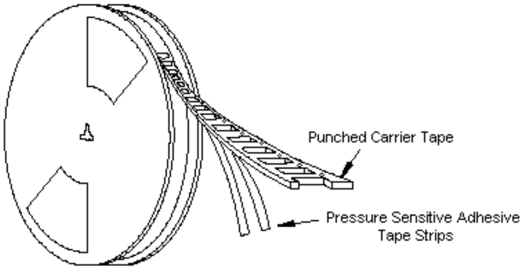


Figure 2

Glossary of Terms & Abbreviations

AOI	automated optical inspection
Ag	silver
Al	aluminum
Au	gold
BGA	ball grid array
C	capacitance
COB	chip-on-board
Cu	copper
CSP	chip scale package
CTE	coefficient of thermal expansion
DCA	direct chip attach
DIP	dual inline package
EMI	electromagnetic interference
ESD	electrostatic discharge
FCIP	flip chip in package
FCP	few-chip package
HDI	high density interconnect
IC	integrated circuit
I/O	input/output
L	inductance
MCP	multichip package
Ni	nickel
PBGA	plastic ball grid array
Pb	lead
Pd	palladium
PWB	printed wiring board
QFP	quad flat pack
R	resistance
RF	radio frequency
RGA	residual gas analysis
SIP	system in package
SMD	surface mount device
Sn	tin
SOC	system on chip
Tg	glass transition temperature
UBM	under bump metallurgy
µBGA	micro ball grid array

References

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- "Electronic Packaging and Interconnection Handbook", Charles Harper, McGraw-Hill, 2000
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