The LM49370 I^2C/SPI INTERFACE SOFTWARE MANUAL

National Semiconductor Audio

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INTRODUCTION:

The LM49370 I^2C/SPI Control Software allows easy read/write access to the data registers of the LM49370 audio subsystem through a user friendly graphic user interface. This document will provide instructions on how to use this software with the LM49370 Demonstration Board and associating USB Subsystem Motherboard.

INSTALLATION:

The LM49370 software is built on a new Microsoft® .NET Framework. It may require that *Microsoft® .NET Framework Software Development Kit (SDK) version 1.1* be installed in your computer, which is downloadable through the Microsoft® website[1]. The LM49370 software setup file will automatically install *Microsoft® .NET Framework Software Development Kit (SDK) version 1.1* if your PC requires it. An internet connection is not required since *Microsoft® .NET Framework Software Development Kit (SDK) version 1.1* is already included in the LM49370 software package. Installation of the SDK may take a few minutes. Once that is completed the rest of the installation process is fast.

The following steps should be followed:

Step 1: Uninstall any existing version of the LM49370 software from Control Panel/Add Remove Program/ LM49370 I2C SPI interface.

Step 2: Extract all of the files from LM49370.zip to a single directory.

Step 3: Run the Setup.exe file.

Step 4: The LM49370.exe file will be installed to your desktop as well as the folder you specified during the installation process.

Step 5: Please make sure that the LM49370 Demoboard and USB Subsystem Motherboard are properly connected to your PC and that proper power is applied to the LM49370 Demoboard. Please refer to the LM49370 Evaluation Package Instructions for details on how to accomplish this.

Step 6: Run the LM49370.exe file. The LM49370 software will run properly only if Step 5 is completed.

OVERVIEW:

The LM49370 Software is divided up into three main sections: Menu Bar, Tab Control, and Status Register and Bar. (please refer to Figure 1)

1) The Menu Bar contains File, Control, Settings and Help Options:

File: This provides an option to exit the program
Control: This provides the option to switch between I^2C and SPI control modes. Switching between I^2C and SPI mode will initialize all of the data registers back to their default settings of zero.
Settings: This sets the USB interface board's regulated output voltage to 3V or 3.8V. The Disable Polling option can be activated to disable continuous polling on the I^2C /SPI interface bus. Continuous polling is desirable whenever constant feedback from the Status Register is required. Enabling the Disable Polling option increases the efficiency of the LM49370 software program. Note: If Disable Polling is activated the Status Register can still be read in by clicking the Read button located in the Status Register section.
Help: This contains the About box, which is used to identify the version number of the software.

2) Tab Controls are divided up into the following:

BASIC: This tab accesses the main functions of the LM49370.
HEADSET/MIC: This tab contains the headset and microphone options.
DAC DSP: This tab contains the DAC DSP functions.
ADC DSP: This tab contains the ADC and AGC functions.
BRIDGE: This tab contains the PCM/I^2S Bridge control options.
INTERFACE: This tab contains the I^2S and PCM interface settings.
CLOCKS: This tab contains the clock divider and PLL control settings.
ADVANCED: This tab provides read/write access to any register using brute force.

3) The Status Register and Bar provide feedback on the communication status between the USB Subsystem Motherboard / LM49370 Demoboard to the LM49370 software. The Status Bar is used to indicate proper I^2C/SPI control interface operation.

Status Messages (please refer to Figure 1):
1) If there is a proper connection between the PC's USB port and the LM49370 Demoboard/USB interface card, the message 'USB Connected' will appear. If there is no proper connection than 'USB I/O error' will appear.
2) For I^2C mode, an 'All ACK' message indicates a successful I2C read/write. An 'I2C ACK missing' message indicates an erroneous I^2C transaction. The message 'SPI Mode' indicates that the control interface is operating in SPI mode.

3) Two hex numbers are displayed here. The first hex number shows the data register address (0xFh) and the second hex number shows the data byte (0x00h). (Figure1)

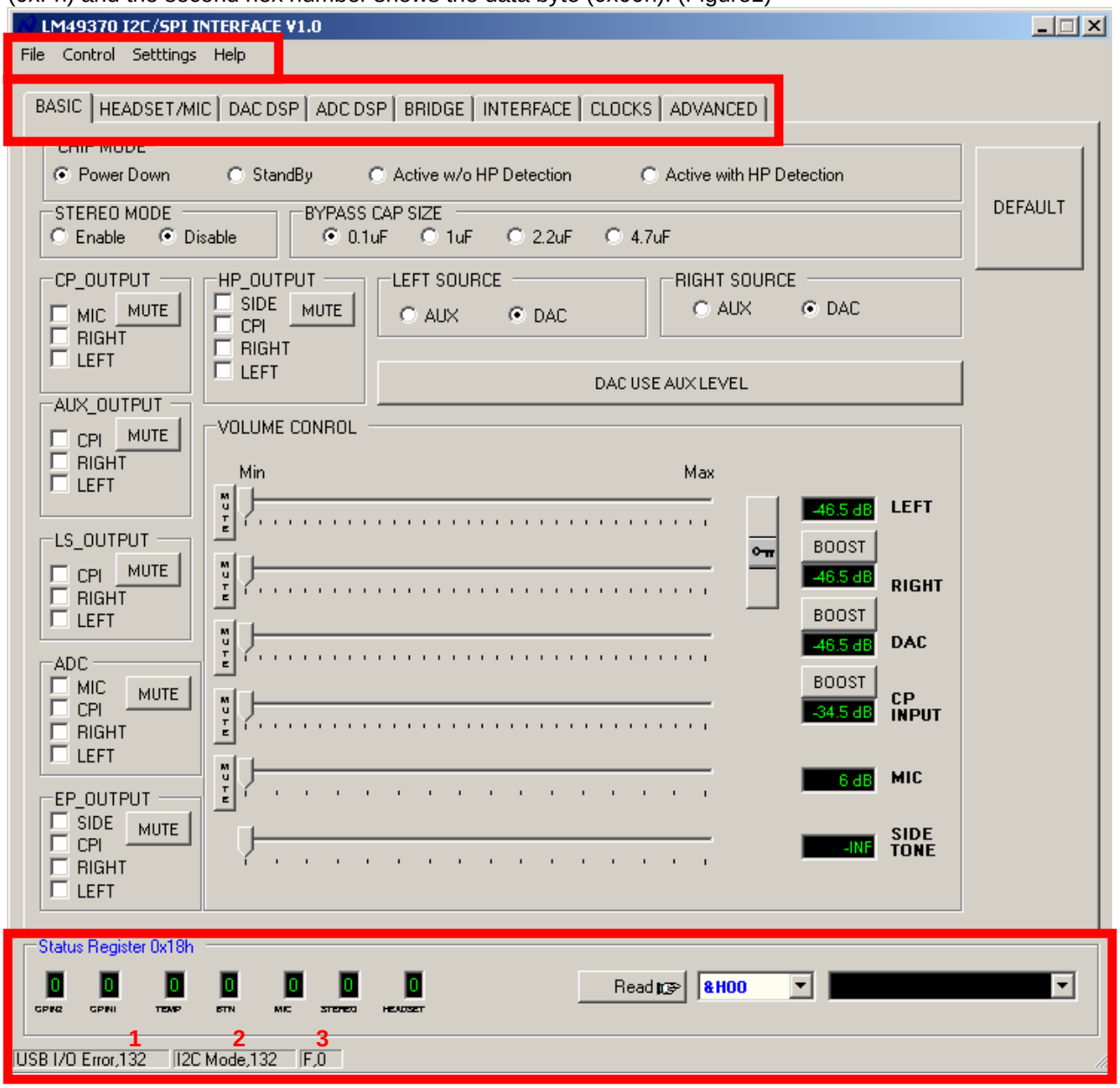


Figure 1: Main view of LM49370 Software (BASIC tab).

DEFAULT BUTTON:

Pressing this button will reset the software back to its default state and will initialize all of the LM49370's data registers back to their default setting of zero.

BASIC TAB:

i) BASIC OPERATIONS:

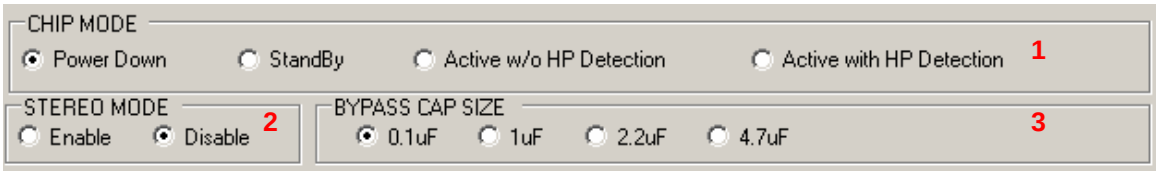


Figure 2: Basic operations

Register (BASIC 0x00h)
1) The LM49370 can be placed in one of four modes which dictate its basic operation.
2) Enabling the Stereo Mode bit reduces the gain of the Left and Right signal by 6dB to allow enough headroom for them to be summed. This may be useful when summing both the Left and Right audio signal to a mono output like the earpiece or loudspeaker.
3) Bypass Cap Size programs the turn-on time of the LM49370 to accommodate the size of the bypass capacitor that is being used.

ii) OUTPUT OPERATIONS:

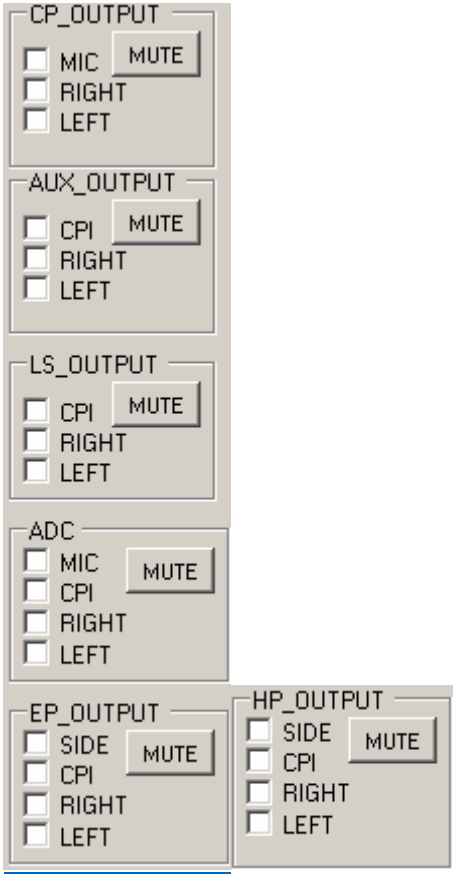


Figure 3: LM49370 outputs

1) CP_OUTPUT: (Register 0x12h). The Microphone, Left, and/or Right inputs can be mixed to the Cell Phone Output by checking the corresponding box(es). Enabling the mute will mute all the inputs.

2) HP_OUTPUT: (Register 0x15h). The Sidetone, Cell Phone, Left, and/or Right inputs can be mixed to the stereo Headphone Output by checking the corresponding box(es). Enabling the mute will mute all the inputs.

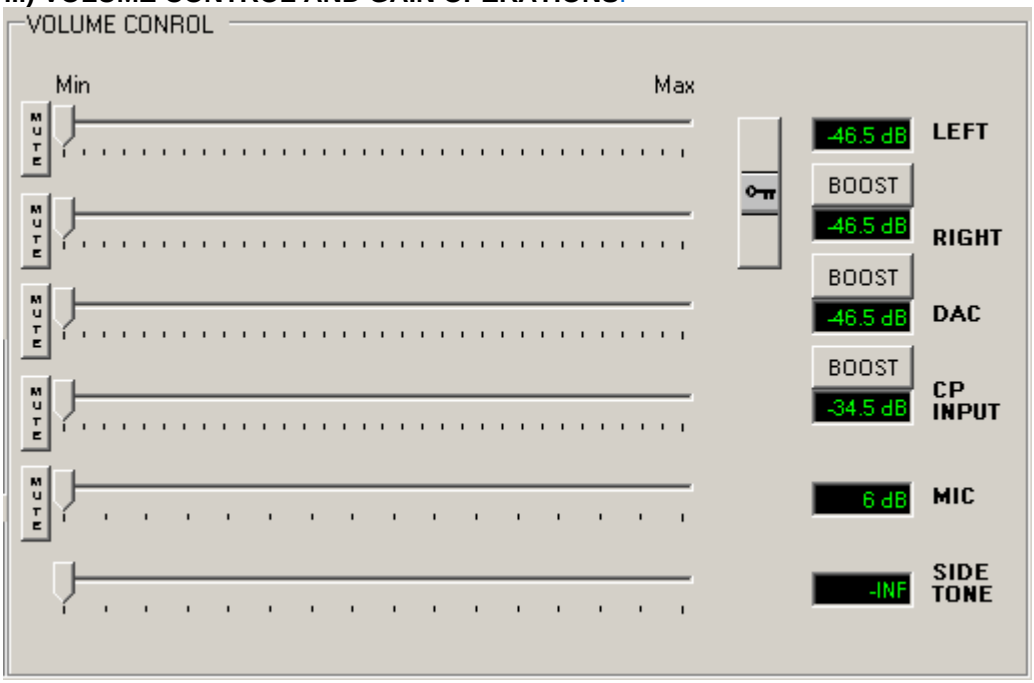
3) AUX_OUTPUT: (Register 0x13h). The Cell Phone, Left, and/or Right inputs can be mixed to the Auxiliary Output by checking the corresponding box(es). Enabling the mute will mute all the inputs.

4) EP_OUTPUT: (Register 0x16h). The Sidetone, Cell Phone, Left, and/or Right inputs can be mixed to the Earpiece Output by checking the corresponding box(es). Enabling the mute will mute all the inputs.

5) LS_OUTPUT: (Register 0x14h). The Cell Phone, Left, and/or Right inputs can be mixed to the Loudspeaker Output by checking the corresponding box(es). Enabling the mute will mute all the inputs.

6) ADC_1: (Register 0x06h). The Microphone, Cell Phone, Left, and/or Right inputs can be mixed to the input of the ADC by checking the corresponding box(es). Enabling the mute will mute all the inputs.

iii) VOLUME CONTROL AND GAIN OPERATIONS:



1) AUX LEFT (0x0Fh). Controls the volume of the AUX Left analog input. Activating **BOOST** increases the gain by 12dB. Enabling **MUTE** will mute the AUX Left analog input.
2) AUX RIGHT (0x10h). Controls the volume of the AUX Right analog input. Activating **BOOST** increases the gain by 12dB. Enabling **MUTE** will mute the AUX Right analog input.
3) DAC (0x11h). Controls the level of the DAC Output. Activating **BOOST** increases the gain by 12dB. Enabling **MUTE** will mute the output of the DAC.
4) CP_INPUT (0x0Eh) Controls the volume of the Cell Phone analog input. Enabling **MUTE** will mute the Cell Phone analog input.
5) MIC_1 (0x0Bh) Controls the volume of the Cell Phone analog input. Enabling **MUTE** will mute the Cell Phone input.

6) SIDETONE (0x0Dh) Controls the analog sidetone volume.

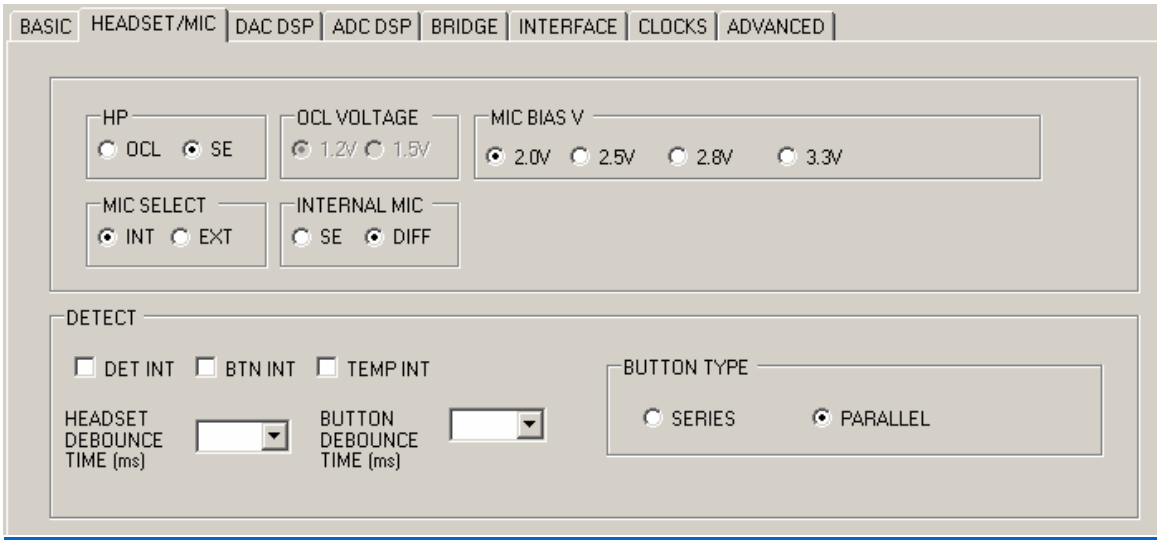
iii) AUX/DAC INPUT SOURCES

Figure 5:

1) If AUX is selected then AUX input is passed to the mixer, the default is for the DAC output to be passed to the mixer.

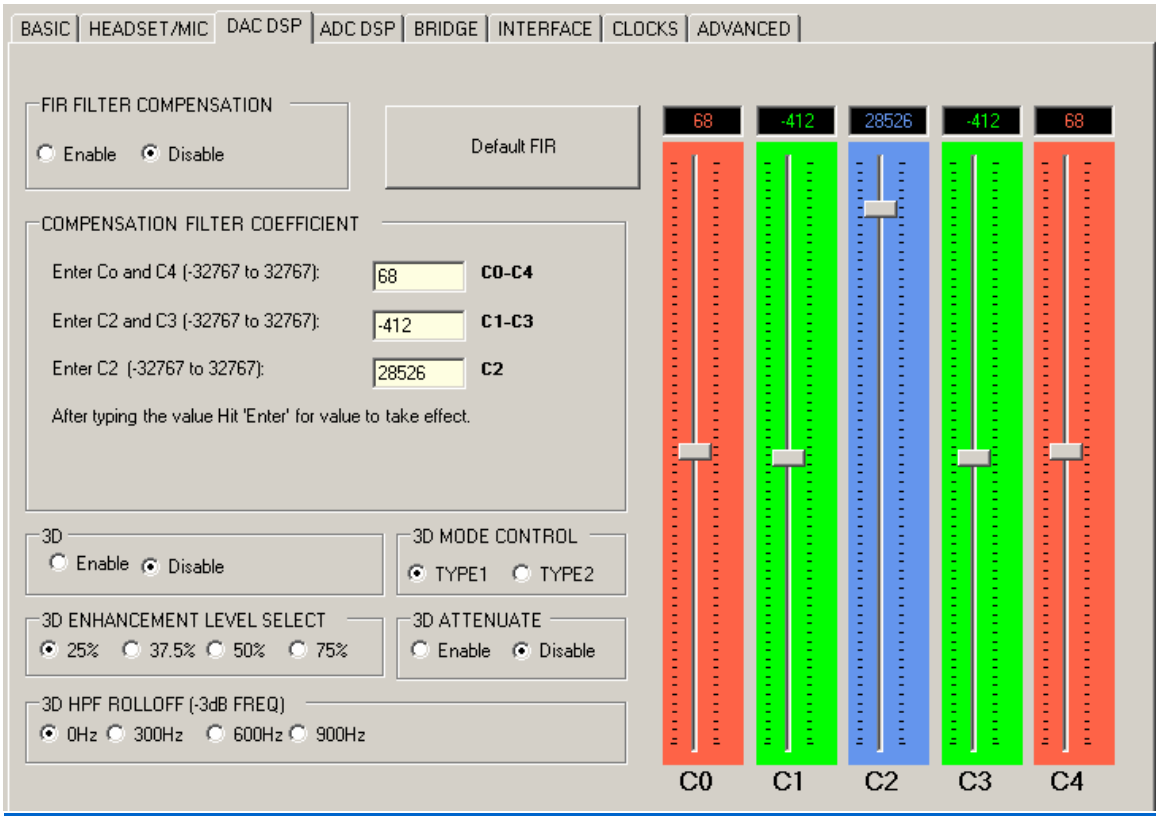
2) If DAC USE AUX LEVEL is enabled then the gain of the DAC inputs is controlled by the AUX_LEFT and AUX_RIGHT registers, allowing a stereo balance to be applied.

HEADSET/MIC TAB:



1) The headphone amplifier can be set to **OCL** or **SE** Mode. Please make sure that the jumper settings of the LM49370 demoboard correspond to the intended headphone mode of operation.
2) When the headphone amplifier is placed in OCL mode, the bias of the headphone amplifier can be programmed to either 1.2V or 1.5V.
3) Internal or external microphone operation is selected here.
4) For internal mic operation, the internal mic inputs can be configured to be either single-ended or fully differential.
5) The bias voltage for either internal or external microphone can be programmed to be 2.0V, 2.5V, 2.8V, or 3.3V.
6) These checkboxes select whether or not a headset detect event, pushbutton event, or temperature event will raise an interrupt on the IRQ pin.
7) The debounce time for the headset detect circuit is set through this pull down menu.
8) The debounce time for the pushbutton is selected through this pull down menu.
9) The type of pushbutton, series or parallel, used by the headset detect circuit is selected here.

DAC DSP TAB:



i) FIR filter Compensation

The DAC DSP tab controls the FIR filter parameters of the LM49370's stereo DAC. The LM49370 features a 5-tap FIR filter that may be used for frequency response modification for digital audio playback through the stereo DAC. The FIR filter is typically used as a digital decimation filter on the DAC output, but it may be used for other high-pass/low-pass/band-pass filter configurations as well.

Since an FIR filter is symmetrical, only three filter coefficients need to be specified. C0 is the same as C4 and C1 is the same as C3. The LM49370's FIR filter coefficients are specified in two's complement and are from -32767 to +32767.

Coefficients may easily be obtained by many filter design or math programs, but will typically be between -1 and 1. In this case, normalizing the coefficients to the -32767 to +32767 baseline is necessary. To do this, simply divide each coefficient value by the largest value of the group and then multiply all by 32767. For example, with a LPF design specifying a 48kHz sample rate, filter cutoff 1 at 10kHz, filter cutoff 2 at 11kHz, 60dB of attenuation and a ripple factor of 0.1 gives the following coefficients (obtained through a standard FIR filter design program):

0.20235500302
0.35188474999
0.42835031296
0.35188474999
0.20235500302

Next, divide all coefficients by 0.42835031296 (the largest value of the group) which gives:

0.47240540487
0.821488252357
1
0.821488252357
0.47240540487

Then multiply these values by 32767 (half the range) which results in the final FIR coefficient values of:

C0 = 15479.3
C1 = 26917.7
C2 = 32767
C3 = 26917.7
C4 = 15479.3

It is important to note that these values may then be linearly scaled up or down by multiplying all values by a constant. Exceeding DAC levels may result in clipping or improper DAC operation, so it is recommended to choose FIR filter coefficients that do not boost certain frequencies above normal clipping levels.

The FIR filter slider bars may also be manipulated manually while the LM49370's stereo DAC is operating to observe the audio effect of the FIR filter coefficients on the audio outputs. FIR filter compensation must be enabled and the stereo DAC must be active to hear the effect of the FIR compensation filter.

i) DAC 3D Enhancement Controls

The LM49370 features a 3D stereo enhancement algorithm for the stereo DAC's digital audio input. The 3D algorithm widens the perceived soundstage of the I2S stereo content which results in a spatialization effect when listening through a pair of headphones or stereo loudspeakers.

1) The 3D effect is enabled or disabled here.
2) This sets the amount of 3D effect applied to the DAC's stereo input.
3) The 3D high-pass filter sets the pole at which the 3D algorithm takes effect. The 3D high-pass filter pole can be set to 0Hz, 300Hz, 600Hz or 900Hz.
4) There are two types of 3D effect. Type1 is recommended for loudspeaker playback. Type2 is recommended for headphone playback.
5) 3D attenuate should be enabled if activating the 3D effect results in audio clipping.

ADC DSP TAB:

The Automatic Gain Control is programmed in this tab.

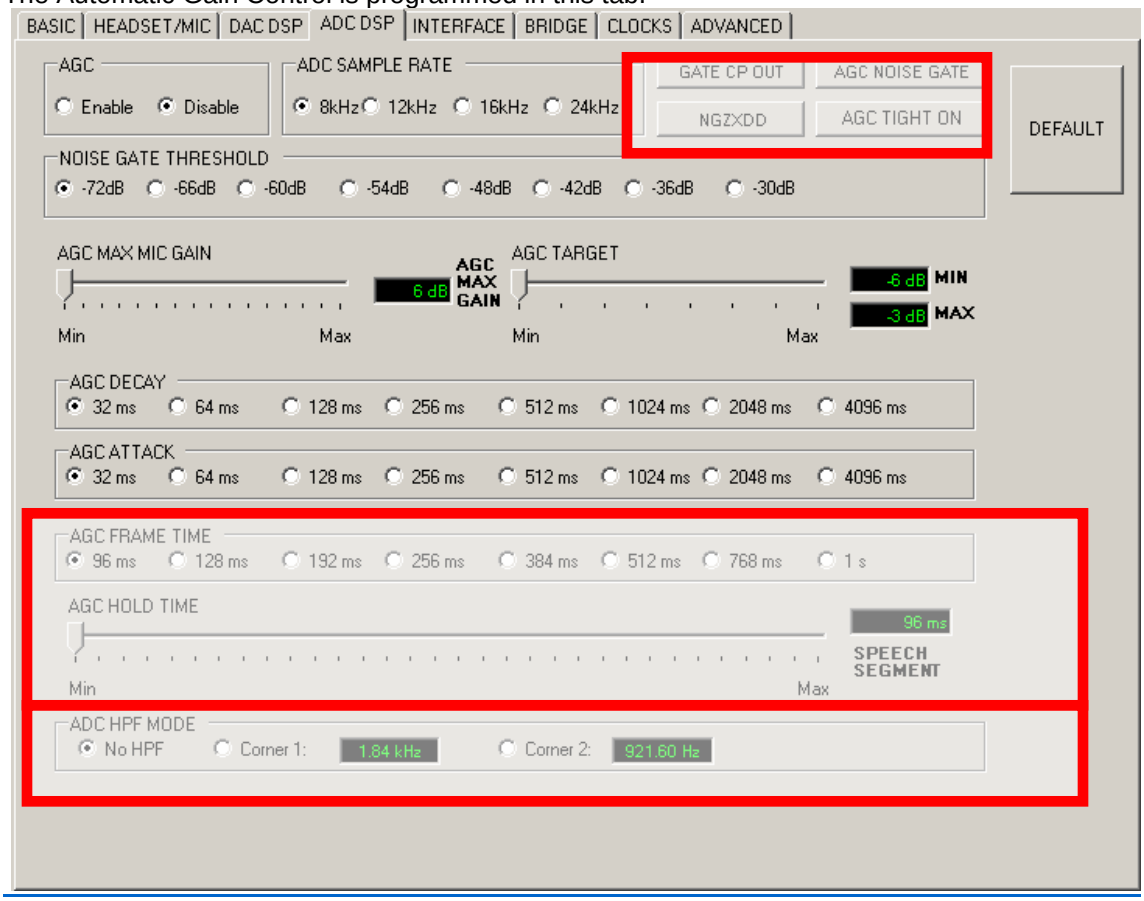


Figure 11: AGC TAB:

1) AGC Enable: This activates the Automatic Gain Control (AGC) circuit

2) AGC MAX MIC GAIN: This programs the maximum gain that the AGC circuit can set the microphone preamplifier to.

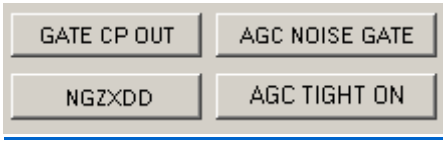
3) AGC TARGET with AGC TIGHT button: This sets the target level of the AGC. Activating AGC TIGHT will narrow the minimum and maximum range of AGC TARGET.

4) ADC SAMPLE RATE: This sets a variable that is required by the AGC algorithm. ADC SAMPLE RATE should be set to the closest expected sample rate of the ADC. This does not set the actual sample rate of the ADC.

5) AGC DECAY: This programs the speed at which the AGC will increase the microphone preamplifier's gain for quiet input signals that are below the AGC TARGET level.

6) AGC ATTACK: This programs the speed at which the AGC will decrease the microphone preamplifier's gain for loud input signals that are above the AGC TARGET level.

Please refer to the AGC_1 (0x08h), AGC_2 (0x09h), AGC_3 (0x0Ah) register pages in the datasheet for further detail.



GATE CP OUT: If enabled and AGC noise is enabled, the MIC to CPO path will be gated if the signal is determined to be noise.
AGC NOISE GATE: If enabled, signals below the noise gate threshold are muted. The noise gate is only activated after a set period of signal absence.
NGZXDD: If enabled, the noise gate will not wait for a zero crossing before mute/unmuting.
AGC TIGHT ON: If enabled, the target level of the AGC will be more precise

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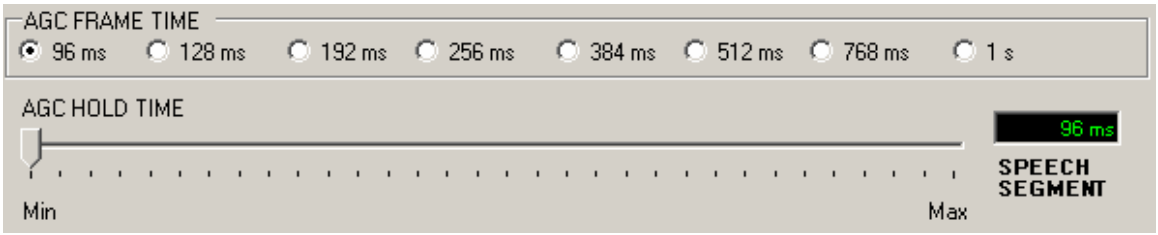
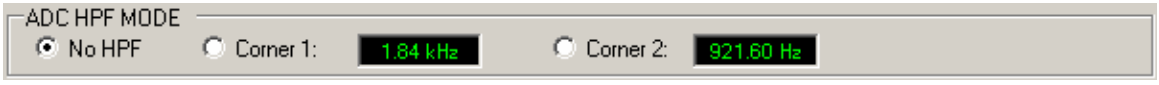


AGC FRAME TIME: This sets the sample rate of the AGC's peak detector.

AGC HOLD TIME: This programs the amount of delay before the AGC begins to adjust the gain of the microphone preamplifier.

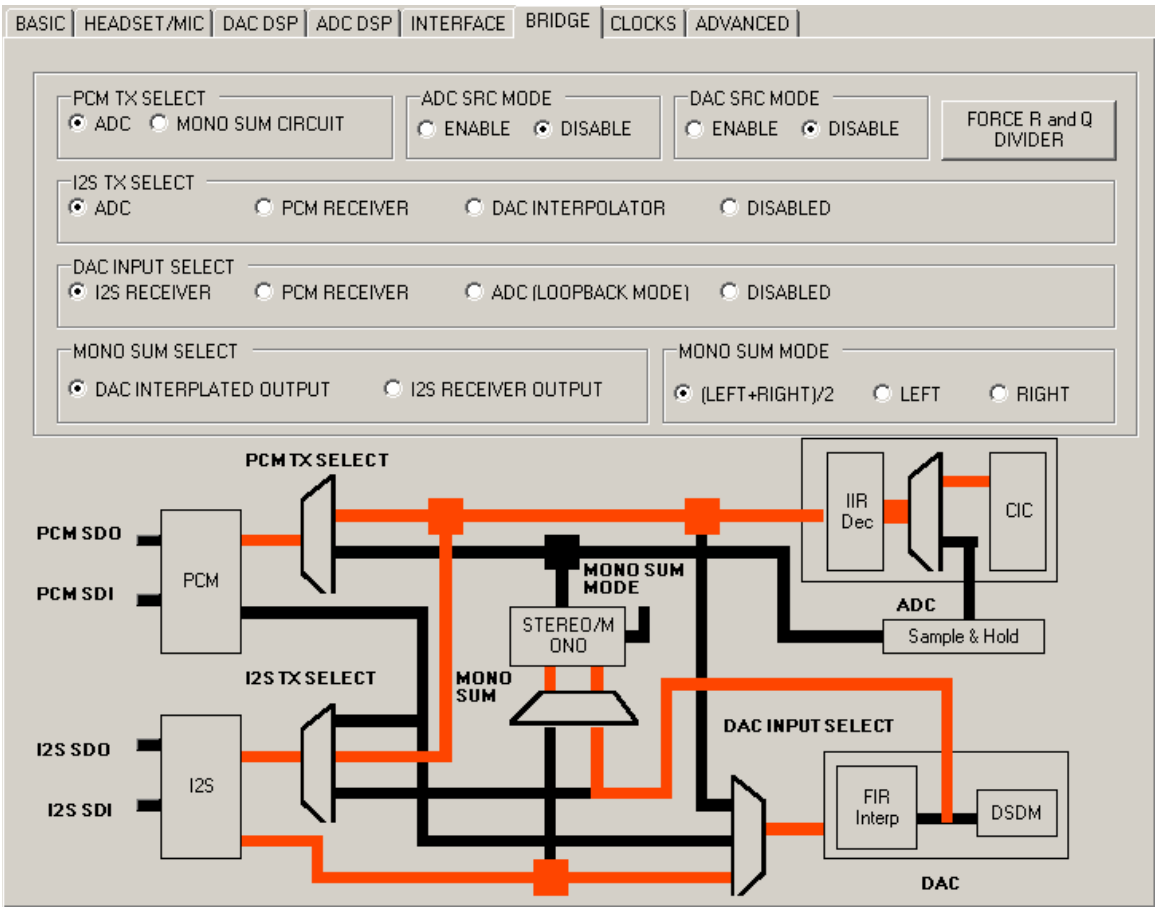
SPEECH SEGMENT is calculated by:
(AGC FRAME TIME) x (AGC HOLD TIME) = SPEECH SEGMENT



ADC_1 HPF_MODE (0x06h). This sets the high pass filter of the ADC.
The corner frequencies are computed as followed:
Corner 1 = ((sample rate of ADC) * 3 / 80)
Corner 2 = (Corner 1) / 2

BRIDGE TAB:

This tab programs the settings of the PCM/I^{2}S Bridge. An interactive schematic of the PCM/I^{2}S Bridge can be used as a visual guide when programming the PCM/I^{2}S bridge.



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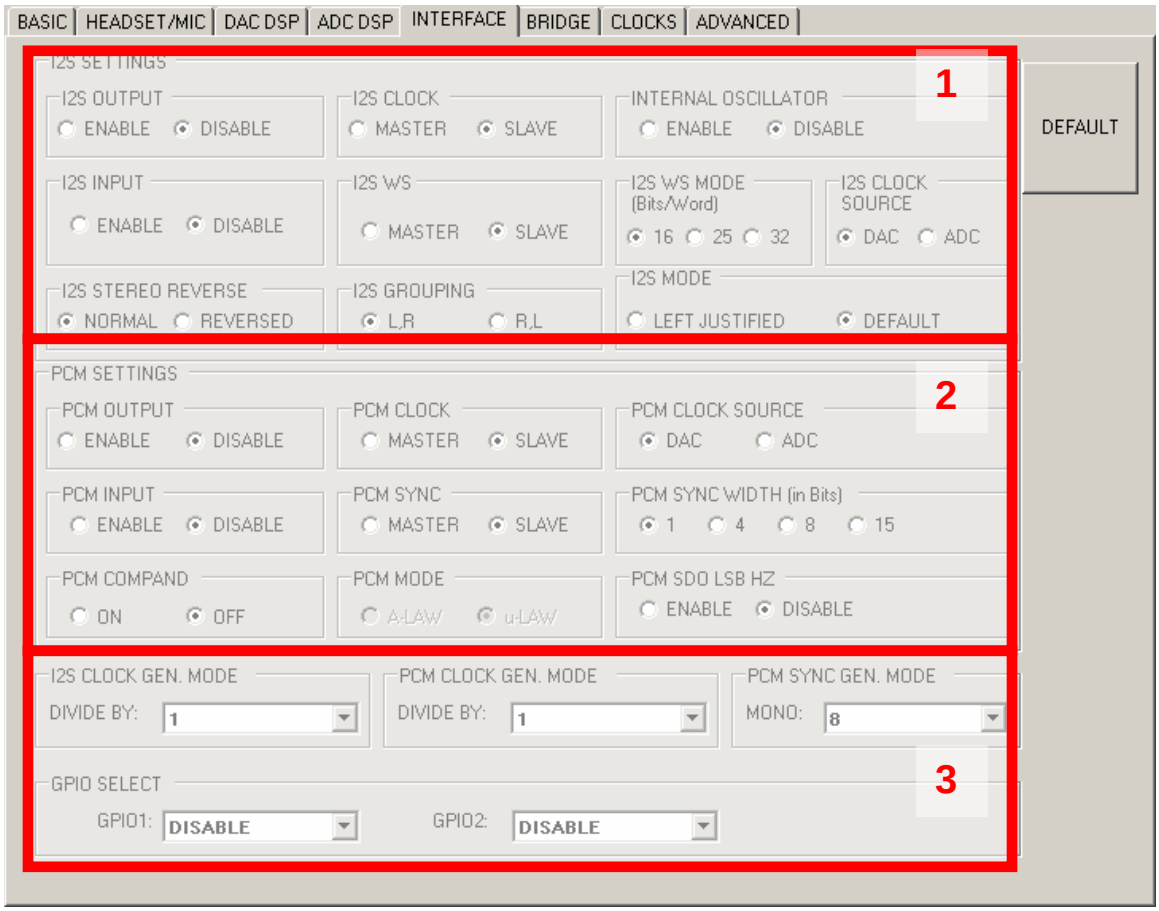
1) PCM TX SELECT: This controls the data sent to the PCM data output.
2) I2S TX SELECT: This controls the data sent to the I^{2}S data output.
3) DAC TX SELECT: This controls the data sent to the DAC input.
4) MONO SUM SELECT: This selects the input to the Mono Sum Circuit.
5) MONO SUM MODE: This controls the operation of the Stereo to Mono Converter.
6) ADC SRC MODE: If enabled, the analog portion of the ADC is disabled. The output of the Sample & Hold block is routed to the ADC instead.
7) DAC SRC MODE: If enabled, the analog portion of the DAC is disabled. This is useful to save power if the analog section of the DAC is not required.
8) FORCE R Q: If set, this enables the R and Q dividers. This should be set whenever the bridge is in use, or if either the PCM or I^{2}S interface is operating as master.

INTERFACE TAB:

This tab programs the settings of the I^2S and PCM interfaces.



1) I^2S Settings:

I2S OUTPUT: This enables the I2S_SDO pin.

I2S INPUT: This enables the I2S_SDI pin.

I2S CLOCK: This sets I2S_CLK to be master or slave.

I2S WS: This sets I2S_WS to be master or slave.

I2S WS MODE: This sets the number of bits per I^2S word.

I2S MODE: This sets the format of the I^2S interface to be standard or left justified.

I2S CLOCK SOURCE: This chooses if the DAC clock or ADC clock is used to drive the I^2S interface. DAC clock is set by the R divider. ADC clock is set by the Q divider.

I2S STEREO REVERSE: This reverses the left and right I^2S channels.

I2S GROUPING: This alters the I^2S receive phasing of the left and right channels. The default status is left channel first and then right.

2) PCM Settings:

PCM OUTPUT: This enables the PCM_SDO pin.

PCM INPUT: This enables the PCM_SDI pin.

PCM CLOCK: This sets PCM_CLK to be master or slave.

PCM SYNC: This sets PCM_SYNC to be master or slave.

PCM SYNC WIDTH: This sets the width of the PCM_SYNC signal.

PCM COMPAND: This sets the PCM data to be either companded or linear. The default mode is for linear PCM data.

PCM MODE: If the PCM data is set to be companded, this chooses the PCM companded format to be either A-law or u-law.

PCM CLOCK SOURCE: This chooses if the DAC clock or ADC clock is used to drive the I2S interface. DAC clock is set by the R divider. ADC clock is set by the Q divider.

PCM SDO LSB HIZ: If set, this will tri-state PCM_SDO after the PCM port has run out of bits to transmit.

3) Clock Generation and GPIO settings

I2S CLOCK GEN MODE: This programs a clock divider that is used to generate I2S_CLK in master mode. The input to this clock divider is either the DAC clock or the ADC clock depending on the status of I2S CLOCK SOURCE.

PCM CLOCK GEN MODE: This programs a clock divider that is used to generate PCM_CLK in master mode. The input to this clock divider is either the DAC clock or the ADC clock depending on the status of PCM CLOCK SOURCE.

PCM SYNC GEN MODE: This programs a clock divider that is used to generate PCM_SYNC in master mode. The input to this clock divider is PCM_CLK.

GPIO1: This pull down menu selects the operation of the GPIO1 pin.

GPIO2: This pull down menu selects the operation of the GPIO2 pin.

CLOCKS TAB:

This tab programs the clock network and PLL settings. This tab also controls the oversampling ratio of the DAC and ADC.

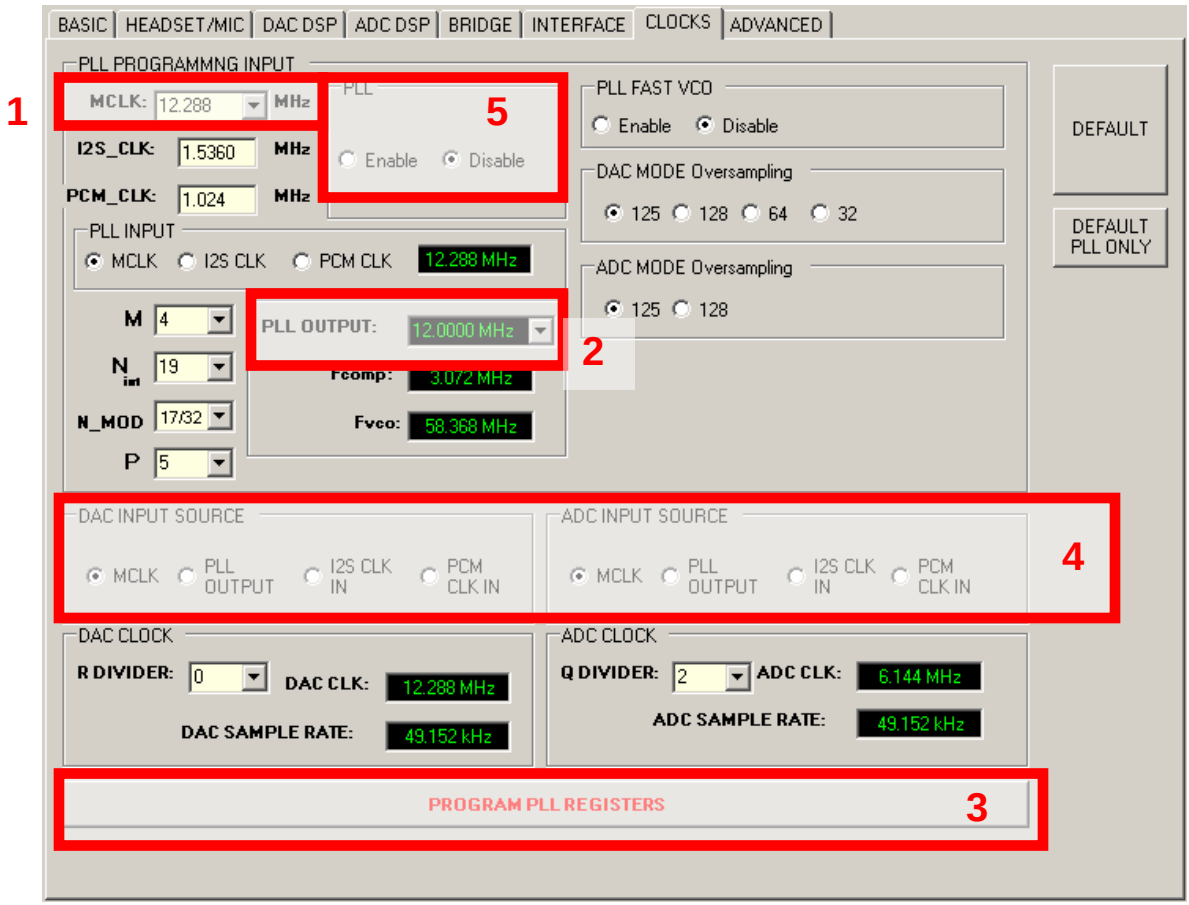


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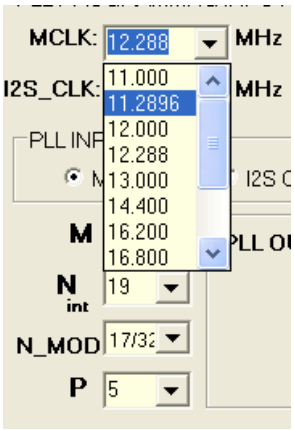
Figure 7: PLL TAB

i) MCLK Drop Down Menu Mode



1) In the MCLK drop down menu (which is based on common system clock values) the user can select from a list of pre-programmed MCLK inputs. Based on the value of MCLK that is chosen from the drop down menu, the LM49370 software will automatically update the M, N, N_MOD and P values according to the MCLK input value and the frequency of the PLL OUTPUT will be calculated in real time.

2) In the PLL_OUTPUT drop down menu, four target values can be selected. For the DAC or ADC operating with an oversampling ratio of 125, a 12 MHz (fs = 48kHz) or 11.0250 MHz (fs = 44.1kHz) target

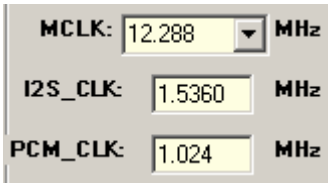
value can be selected. When operating with an oversampling ratio of 128, a 12.288 MHz (fs = 48kHz) or 11.2896 MHz (fs = 44.1kHz) target value can be selected. The M, N, N_MOD and P values will be calculated based on the value chosen in the PLL OUTPUT and MCLK drop down combo boxes.

3) The **Program PLL Registers** button updates the internal PLL registers of the LM49370 when pressed. This button will be highlighted in red to indicate that the LM49370's PLL registers have not been updated.

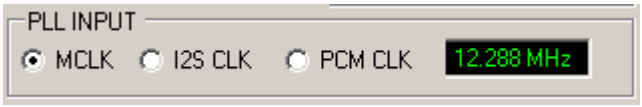
4) The audio DAC and ADC input sources must be set for PLL OUTPUT if the PLL is required to provide the correct clock to the DAC and ADC.

5) If the PLL is required, the PLL is activated through the PLL Enable radio button.

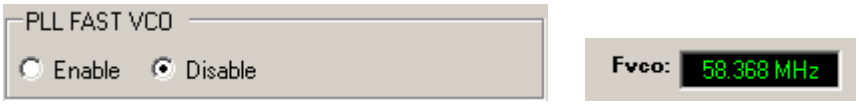
ii) User Defined MCLK or I2S CLK Mode



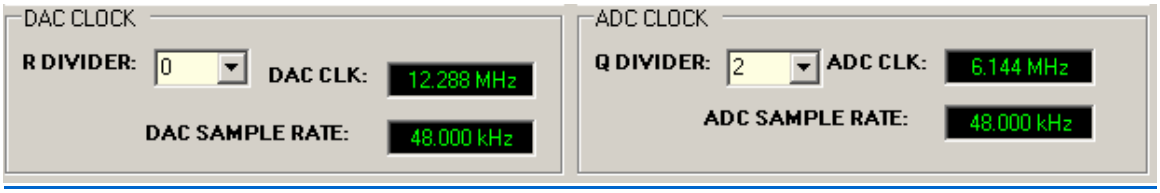
The user can also choose their own MCLK, I2S CLK, or PCM CLK value by simply entering that value into the corresponding input field. The M, N, N_MOD and P values are not automatically updated as they were when using the MCLK Drop Down Menu Mode. The M, N, N_MOD and P should be manually adjusted to achieve the correct PLL OUTPUT target value. The only time that the M, N, N_MOD and P values are automatically calculated is when MCLK is chosen from the pre-programmed list of values on the drop down menu for MCLK.



PLL INPUT: This selects which clock is used to drive the input of the PLL. The frequency of the PLL input clock is displayed in the text box.



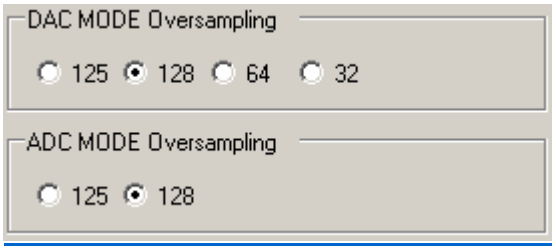
PLL FAST VCO: This sets the mode of operation of the PLL. If the PLL VCO frequency (indicated by Fvco) is greater than 60MHz, then PLL FAST VCO should be enabled.



R DIVIDER: This pull down menu programs the R divider. The R divider generates the clock required by the DAC for sampling. The resulting DAC clock and DAC sample rate are displayed in their corresponding text boxes.

Q DIVIDER: This pull down menu programs the Q divider. The Q divider generates the clock required by the ADC for sampling. The resulting ADC clock and ADC sample rate are displayed in their corresponding text boxes.

iv) Setting the oversampling ratio

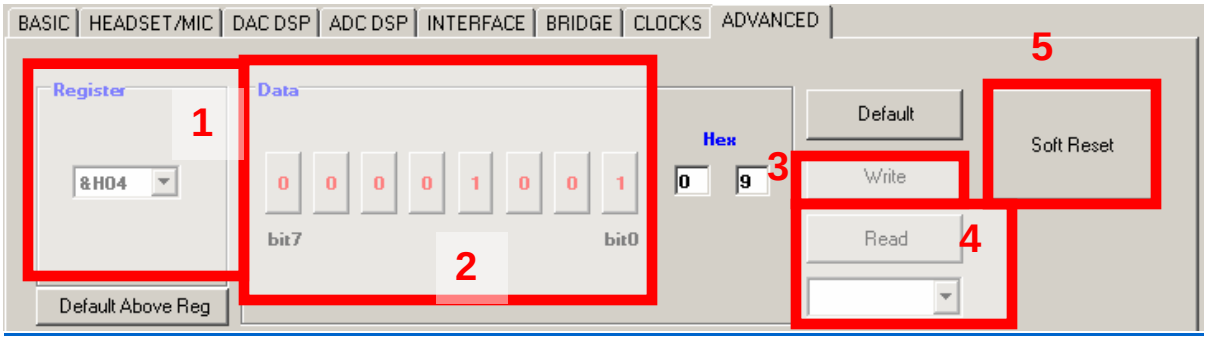


DAC MODE OVERSAMPLING: The oversampling ratio of the DAC can be set to one of four values: 125, 128, 64, and 32.

ADC MODE OVERSAMPLING: The oversampling ratio of the ADC can be set to either 125 or 128.

ADVANCED TAB:

This tab allows the user to directly program a specific data register. This tab is useful for system debug.



1) The Register drop down menu allows the user to select a specific data register to read/write to.

2) This row of 8 buttons sets the bit7 to bit0 data of the specified register. Each button press will trigger an I2C/SPI write.

3) This will write the current data field to the specified register.

4) Pressing the Read button will read the contents of the specified data register into the text box below the button.

5) Pressing the SOFT RESET button will reset the LM49370.

References:

1) Microsoft framework .net 1.1 Direct download link
http://www.microsoft.com/downloads/details.aspx?FamilyId=9B3A2CA6-3647-4070-9F41-A333C6B9181D&displaylang=en