

# BIG3GIG EVALUATION BOARD

## ADC083000, ADC08B3000

## MANUFACTURING KIT / REFERENCE DESIGN

National Semiconductor GHz 8 bit ADC + XILINX Virtex 4

### SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.

**Print Instructions:**

- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.


### SYSTEM CONFIGURATION

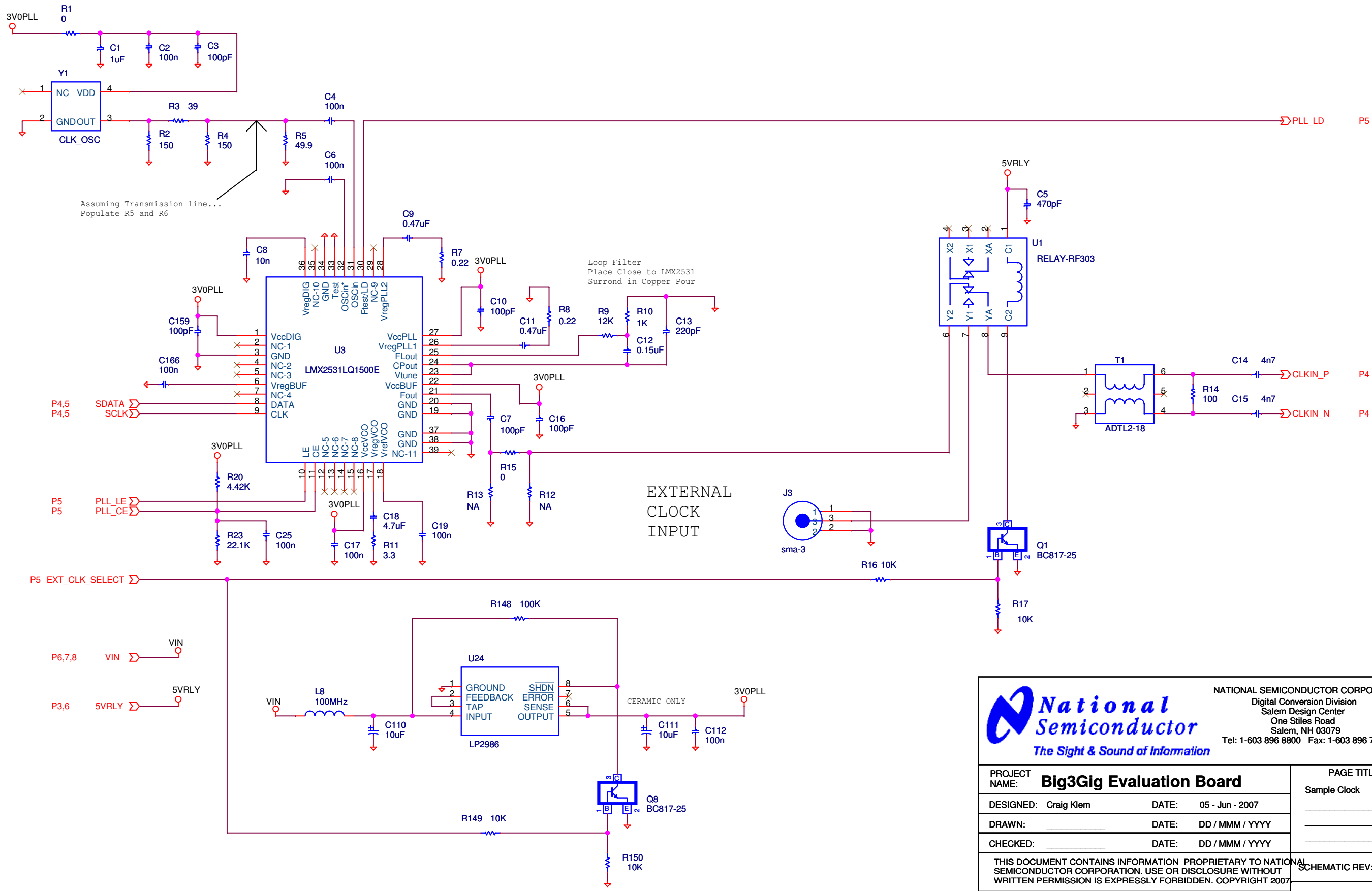
Module	Configuration	Description
FRONT END	1 channel DIFF. / SINGLE ENDED	AC AND DC COUPLING OF SIGNAL PATH
CLOCK SOURCE	SINGLE ENDED	LMX2531LQ1500E
FPGA		XC4VLX15-10SFG363C - 363 PIN BGA
USB I/F		CY7C68013A EZ USB


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## PRELIMINARY

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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		
DESIGNED: Craig Klem	DATE: 05-Jun-2007	LAYOUT JOB#: _____
DRAWN: _____	DATE: DD/MMM/YYYY	LAYOUT REV: _____
CHECKED: _____	DATE: DD/MMM/YYYY	ASSEMBLY REV: _____
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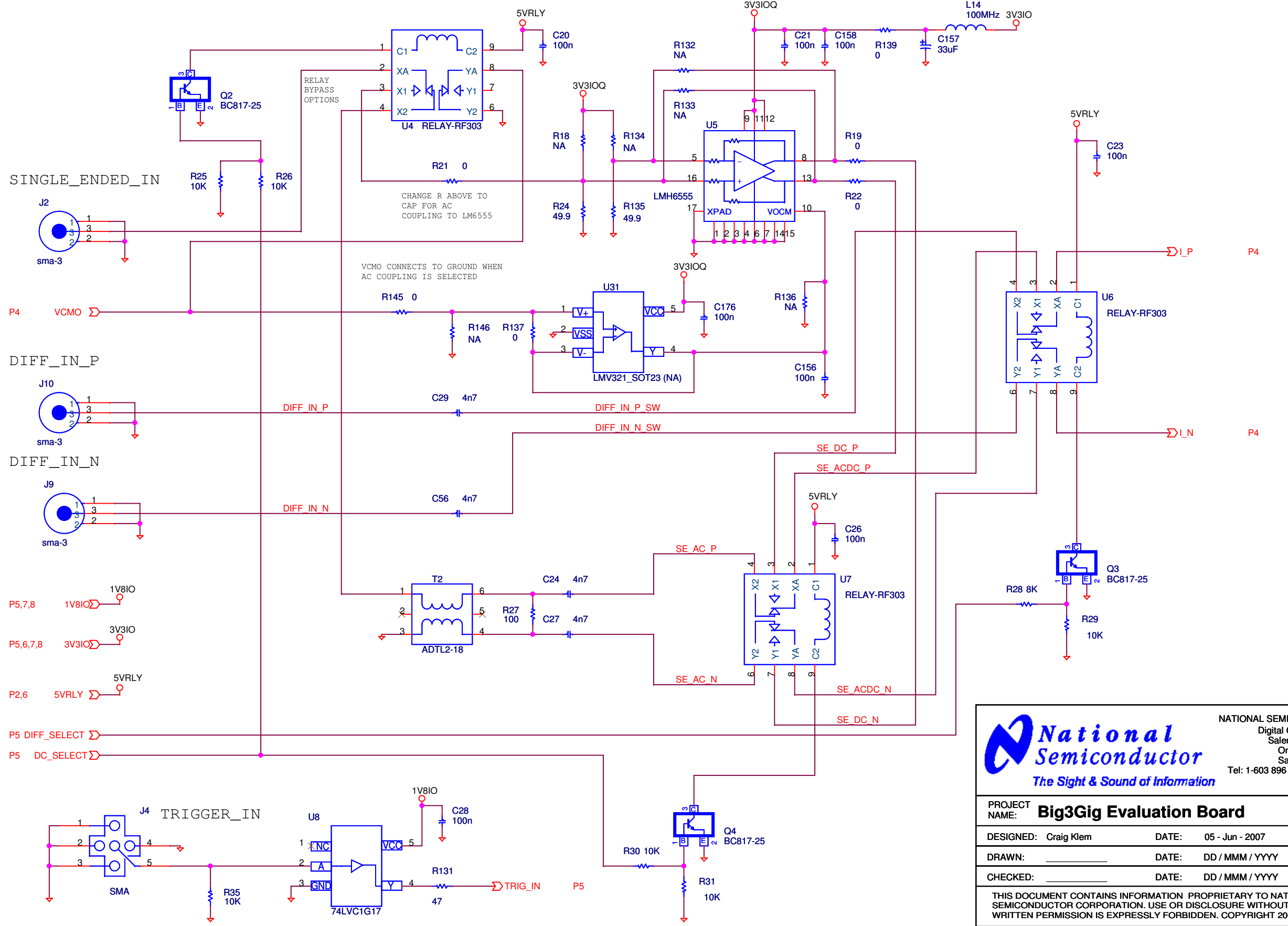





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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE: Sample Clock
DESIGNED: Craig Klem	DATE: 05 - Jun - 2007	
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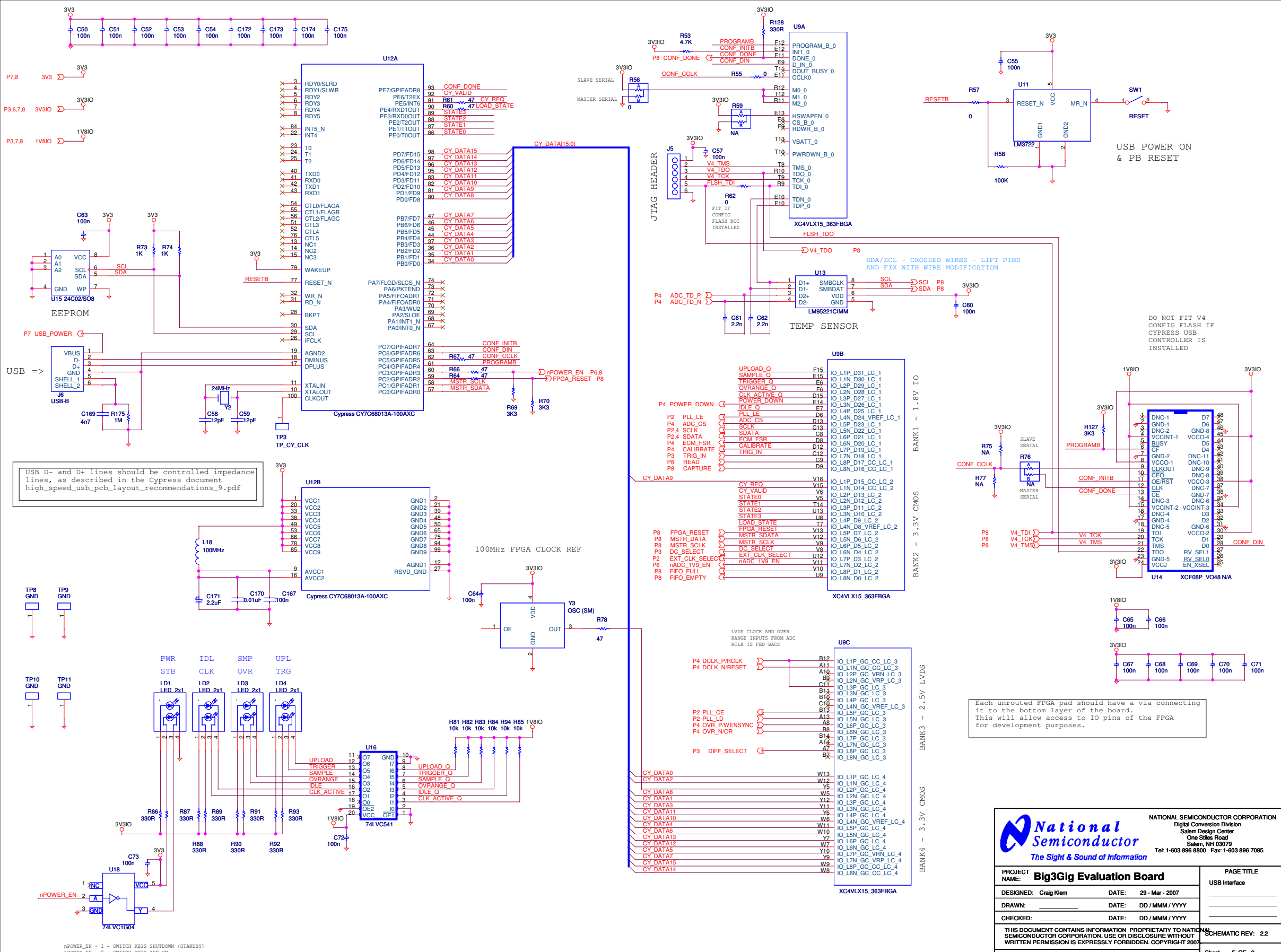


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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE
DESIGNED: Craig Klem	DATE: 05 - Jun - 2007	Analog Inputs
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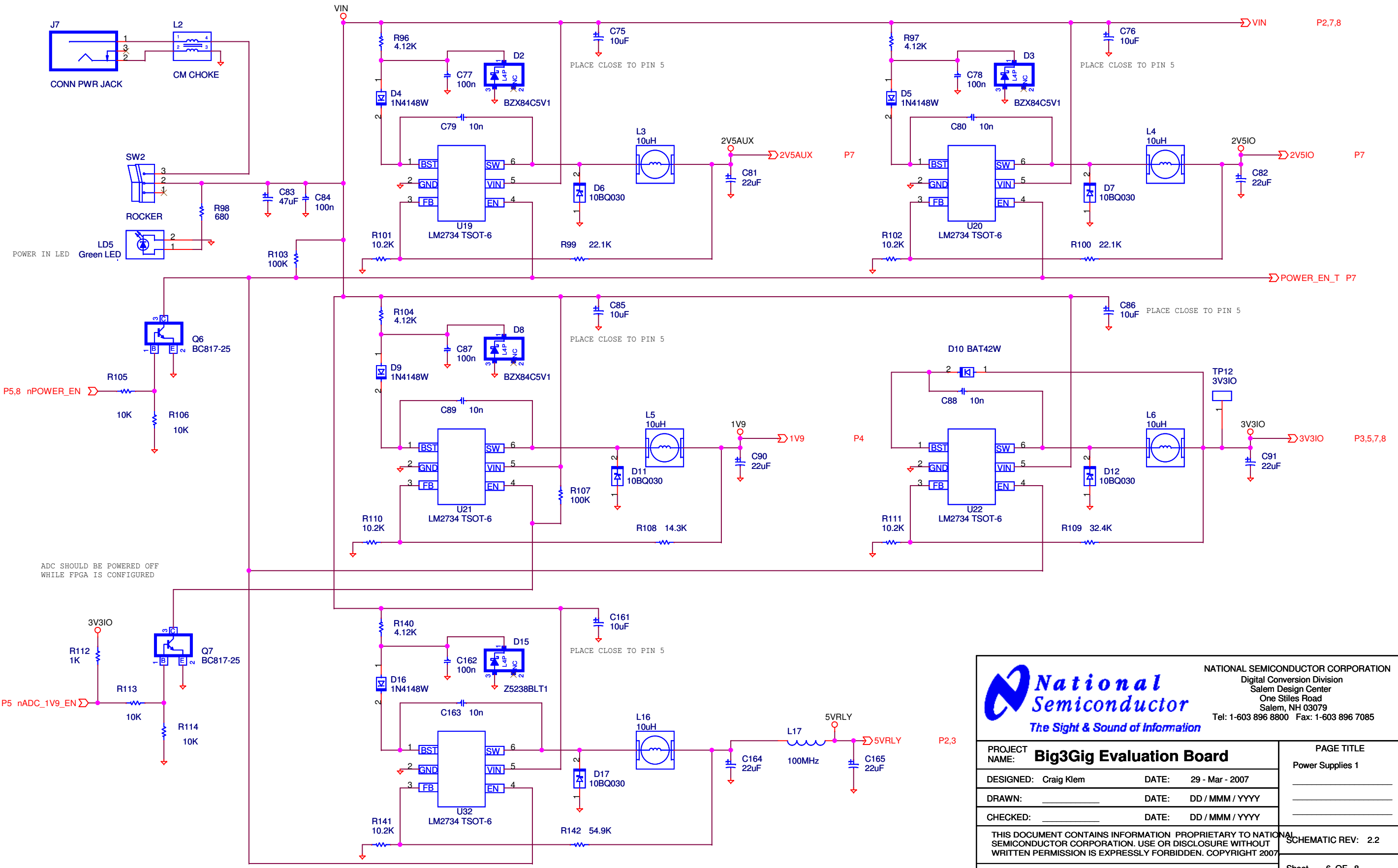





Each unrouted FPGA pad should have a via connecting it to the bottom layer of the board. This will allow access to IO pins of the FPGA for development purposes.

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PROJECT NAME: <b>Big3Gig Evaluation Board</b>	PAGE TITLE: USB Interface
DESIGNED: Craig Klem DATE: 29-Mar-2007	
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	Sheet 5 OF 8

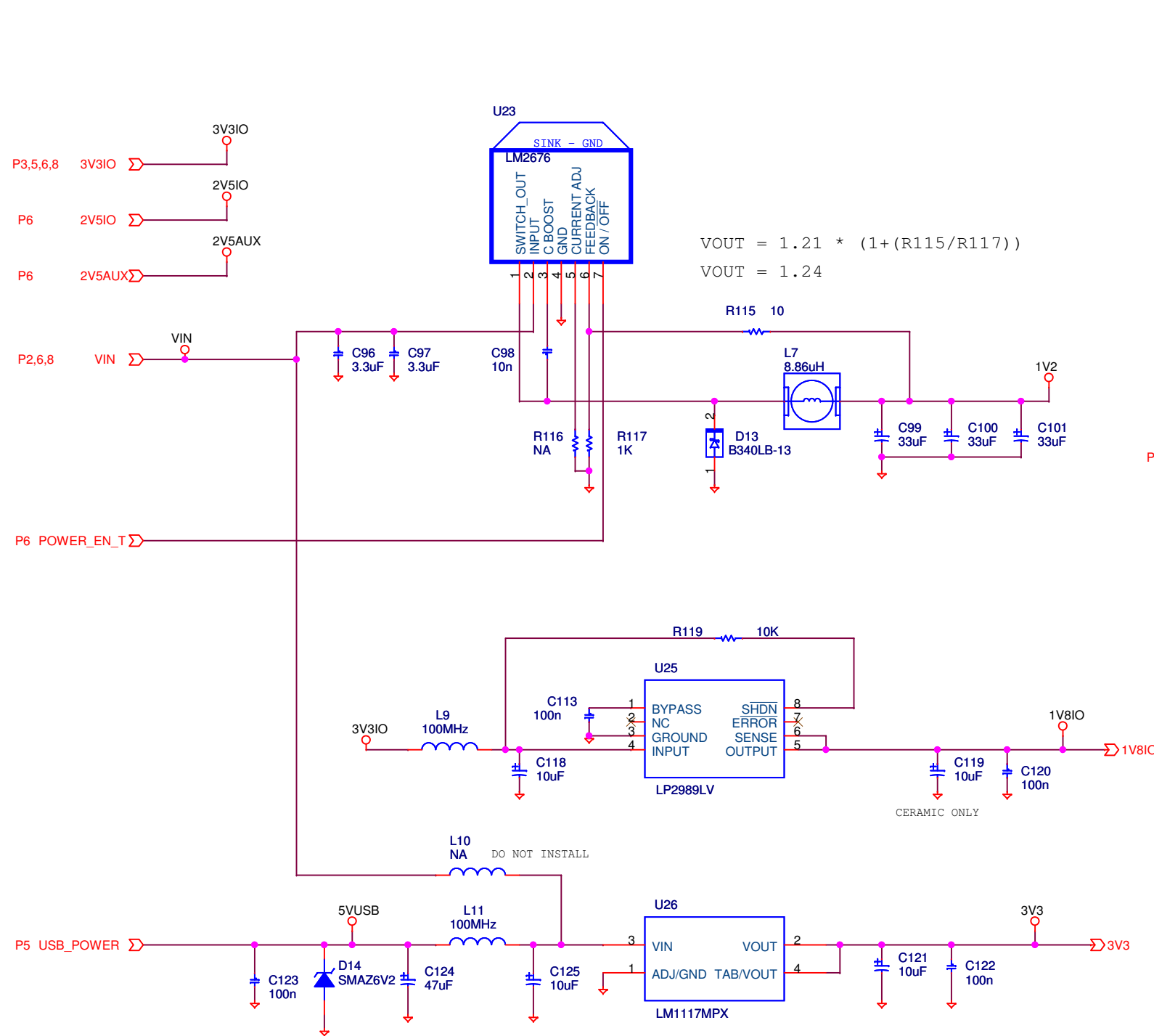




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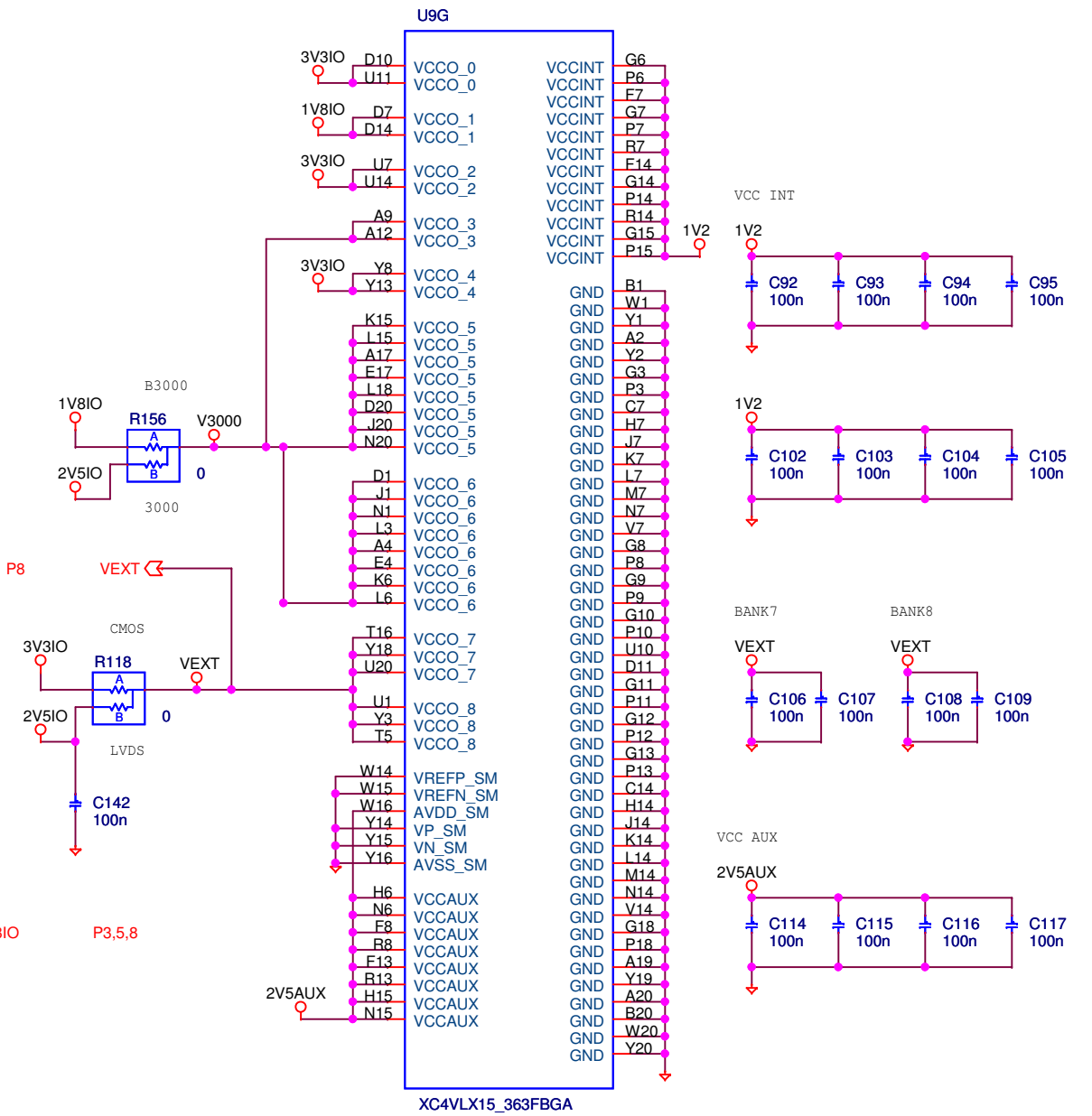
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE
DESIGNED: Craig Klem	DATE: 29 - Mar - 2007	Power Supplies 1
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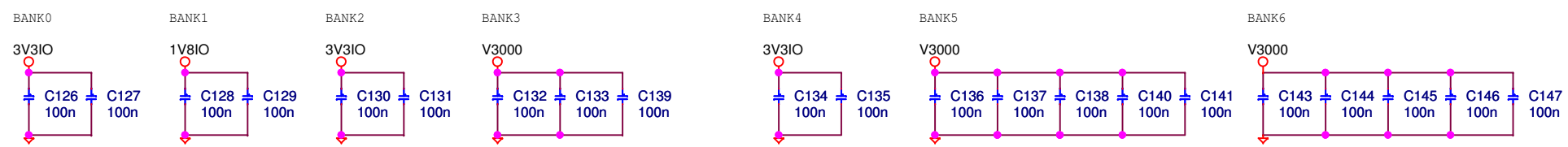



$$V_{OUT} = 1.21 * (1 + (R_{115}/R_{117}))$$

$$V_{OUT} = 1.24$$



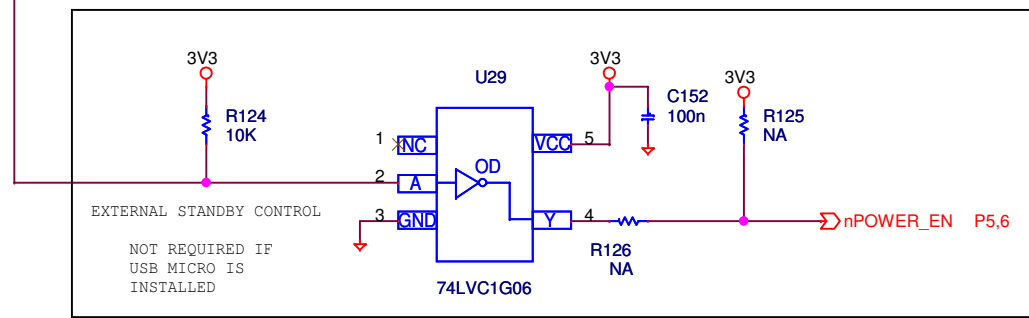
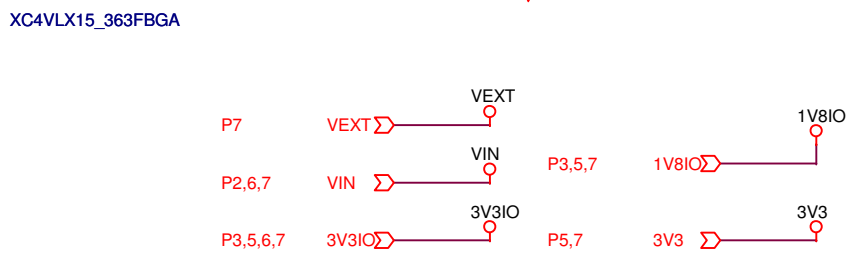
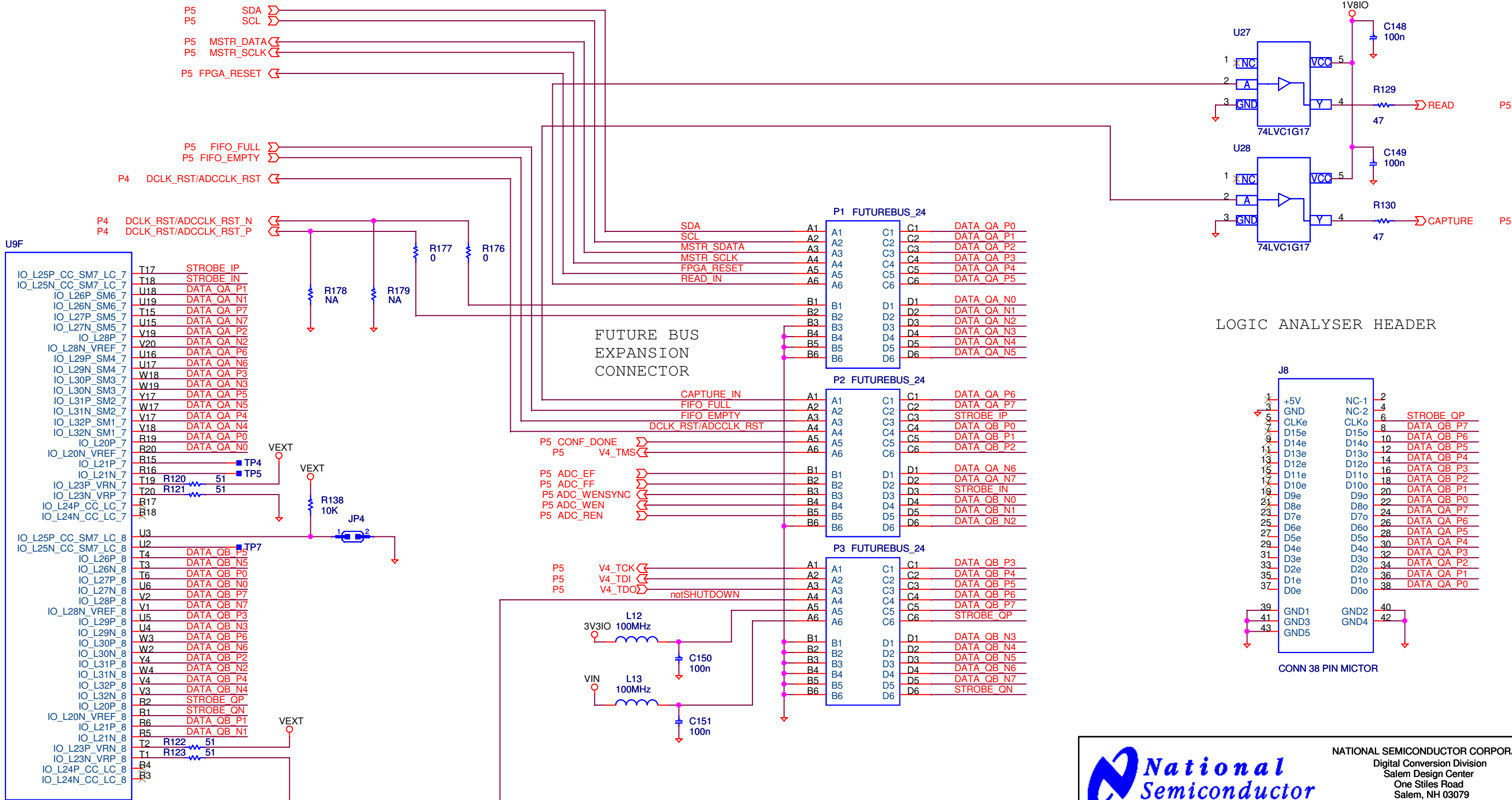
0402 FPGA Decouplers






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<b>PROJECT NAME: Big3Gig Evaluation Board</b>		<b>PAGE TITLE</b>
DESIGNED: Craig Klem	DATE: 29 - Mar - 2007	Expansion Port
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