Sometimes, one capacitor is better that two

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Many A/D converters use an internal resistor ladder as a two-point differential voltage reference in the conversion. This method demands that these two nodes remain steady. The higher the resolution, the stronger the demand for quiet voltages. **Figure 1** depicts a simplified schematic of the LM985XX reference ladder. **Figure 1a** shows the traditional decoupling scheme; **Figure 1b** shows a proposed scheme. Typically, designers use two capacitors to decouple each reference node—one low-value capacitorand one of higher value because the effective series inductance (ESL) of the smaller capacitor is much lower than that of the larger one. Contrary to tradition, you can eliminate these larger capacitors and replace them with one differential capacitor if you choose the values wisely. Because the difference in the reference voltages, DV_{REF}, is important in conversion, this is the delta that is of interest.

Figure 1b shows two common-mode decoupling capacitors, C_1 and C_2, and the differential capacitor, C_3. The current sources, I_1 and I_2, represent the average currents pushing or pulling on the lad-der. These currents are generally proportional to the input voltage, V_{IN}, and the sampling frequency, f. If the input voltage is periodic or at least quasiperiodic, then you can choose the decoupling capacitors on the basis of the maximum ripple voltage allowed to appear differentially on the nodes. This ripple specification is based on the permissible output error. The poles and zero of the transfer function are, respectively,

$$\text{pole}_1 = \frac{(C_2 \bullet R_{P3} \bullet R_{P1} + C_3 \bullet R_{P2} \bullet R_{P1} + C_1 \bullet R_{P2} \bullet R_{P3})}{[(C_2 \bullet C_3 + C_1 \bullet C_3 + C_1 \bullet C_2) \bullet R_{P2} \bullet R_{P3} \bullet R_{P1}]} \bullet \delta;$$

$$\text{pole}_2 = \frac{1}{2} \bullet \frac{(C_2 \bullet R_{P3} \bullet R_{P1} + C_3 \bullet R_{P2} \bullet R_{P1} + C_1 \bullet R_{P2} \bullet R_{P3})}{[(C_2 \bullet C_3 + C_1 \bullet C_3 + C_1 \bullet C_2) \bullet R_{P2} \bullet R_{P3} \bullet R_{P1}]} \bullet$$

$$(\delta - 2):$$

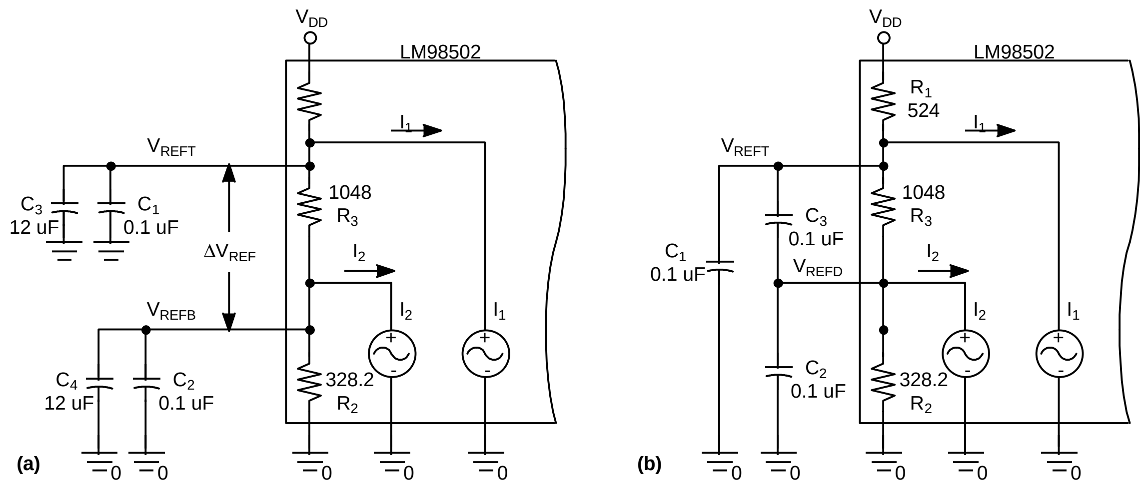
$$(\delta << 1)$$

$$\text{ZERO} = \frac{R_2 + R_1}{R_2 \bullet R_1 (C_1 + C_2)}, \text{ and } R_{PK} = \frac{R_n \bullet R_m}{R_n + R_m}$$

where k, n, and m are cyclic permutations of 1, 2, and 3. You can easily see that the pole in the first equation is the dominant pole. As long as the zero is sufficiently far from pole1, then this pole (hence, C3) determines the roll-off. If C1 and C2 are small enough, the zero finds itself well away from pole1. Using the values in **Figure 1b**, the poles and zero become pole_1=–28.50 Hz; pole_2=–3.948×104 Hz; and zero=2.48×105 Hz.

Typically, the current sources have a fundamental frequency equal to the frequency of the analog clamp. The most pessimistic assumption is that the input signal contains all white pixels. This scenario causes the maximum swing in the current sources and the smallest duty cycle. Using this assumption and a current amplitude of 0.6 mA, the capacitor values shown in **Figure 1b** would produce DV_{REF} = 1.989 mV. Instead, if you used a pair of 12-µF decoupling capacitors, as in **Figure 1a**, the circuit would produce DV_{REF} = 3.975 mV. (DI #2543)

Figure 1



More is not always better; the circuit in b provides better decoupling than the one in a.