

MPL in cell Phones makes smaller, smarter serial links

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(Original printed on PlanetAnalog February 23, 2005)*

Mobile Pixel Link (MPL) provides cell phone architects with a new low power, low-EMI serialized interface alternative to replace the high-power, non-standard, pin-consuming wide parallel interfaces commonly used in the video paths today. The interface challenge get more difficult as color depth increases or display resolution increases, as the pixel bandwidth demand greatly increases.

Today's portable applications are QCIF+ to QVGA mainly, with a few VGA display products available. As VGA becomes more prevalent and high-end applications go to even higher resolution displays, the bandwidth demand greatly increases from today's benchmark. Making the parallel buses simply wider or faster is not a feasible solution anymore. Figure 1 shows the color bandwidth demand assuming 18-bit color and 60 fps refresh for common display sizes. It does not include control or any transmission overhead, thus is conservative. Portable display systems requiring >500 Mbps bandwidth are just around the corner.

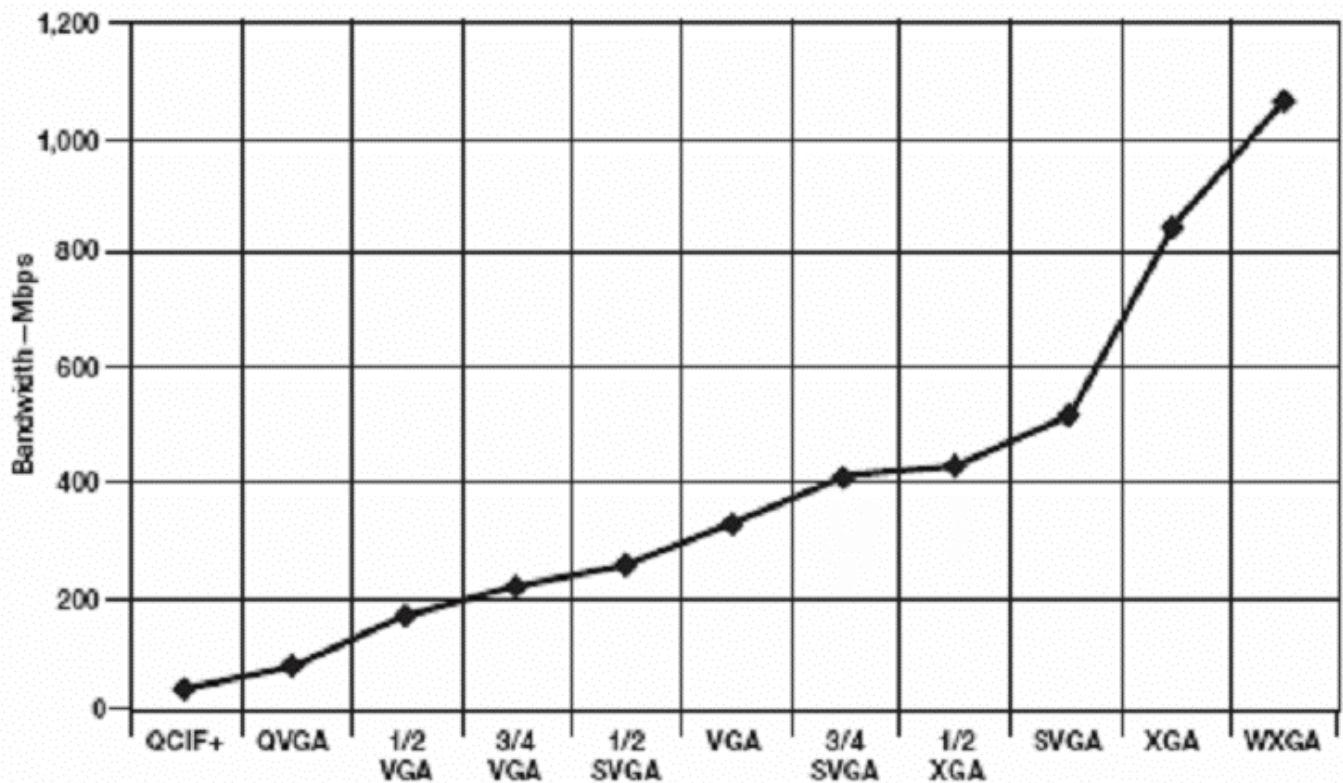


Figure 1: A display color bandwidth vs. display resolution curve shows the ever increasing interface throughput demand.

One solution to the bandwidth problem that addresses several system constraints is the MPL SERDES solution. This provides the system with a smaller interconnect (less connector pins, smaller connector

footprint, smaller interconnect, and lower interconnect costs), low EMI, and also intrinsic level translation. A common dual display application diagram is shown in figure 2 and is explained in detail next.

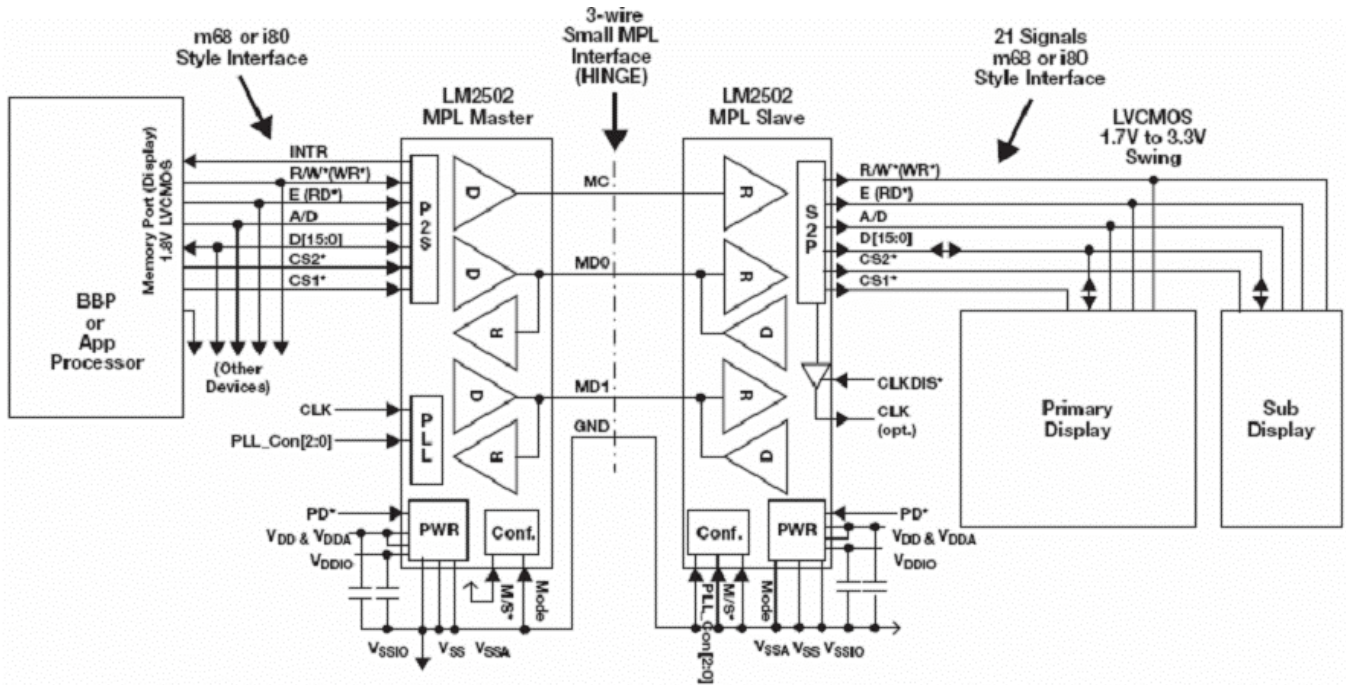


Figure 2: The MPL SERDES chipset saves 85% of the signal lines while supporting two displays.

On the Host side, the LM2502 is configured as a Master, and connects to a memory CPU interface which can be m68 or i80 style. Two chip select signals are supported to be able to address the main and sub displays utilized in the popular flip phone application. The primary role of the Master is to serialize and transmit the words (WRITE transaction) that are sent to the displays. The MPL link can also support READ transactions to check display register contents if required. The interconnect savings are tremendous! Twenty one signals (16 data + AD + E + R/W + CS1 + CS2) are serialized down to just three active signal lines. This yields an impressive 85% reduction in the interconnect! The smaller interconnect frees up routing channels for other signals or additional isolation. It also makes the interconnect physically smaller, and eases the mechanical design challenges in the hinge or swivel area.

Over on the Display side, the LM2502 is configured for a Slave device. Its primary function is to deserialize the data and convert it back into a parallel form. It can also provide an optional clock signal out if needed. This can be used to provide a frequency reference to the display or perhaps an imager device. Notice also that the two parallel buses are now separate voltage domains. This provides level translation between the host and the display device. The signals on the Host side from the baseband or graphic processor tend to be lower voltage CMOS (i.e. 1.8V or less), while the parallel bus tends to be higher voltage on the Display side (i.e. 2.4V or even 3.0V). With the separate VDDIO biasing on the Master and Slave, the level translation problem between baseband and display is solved.

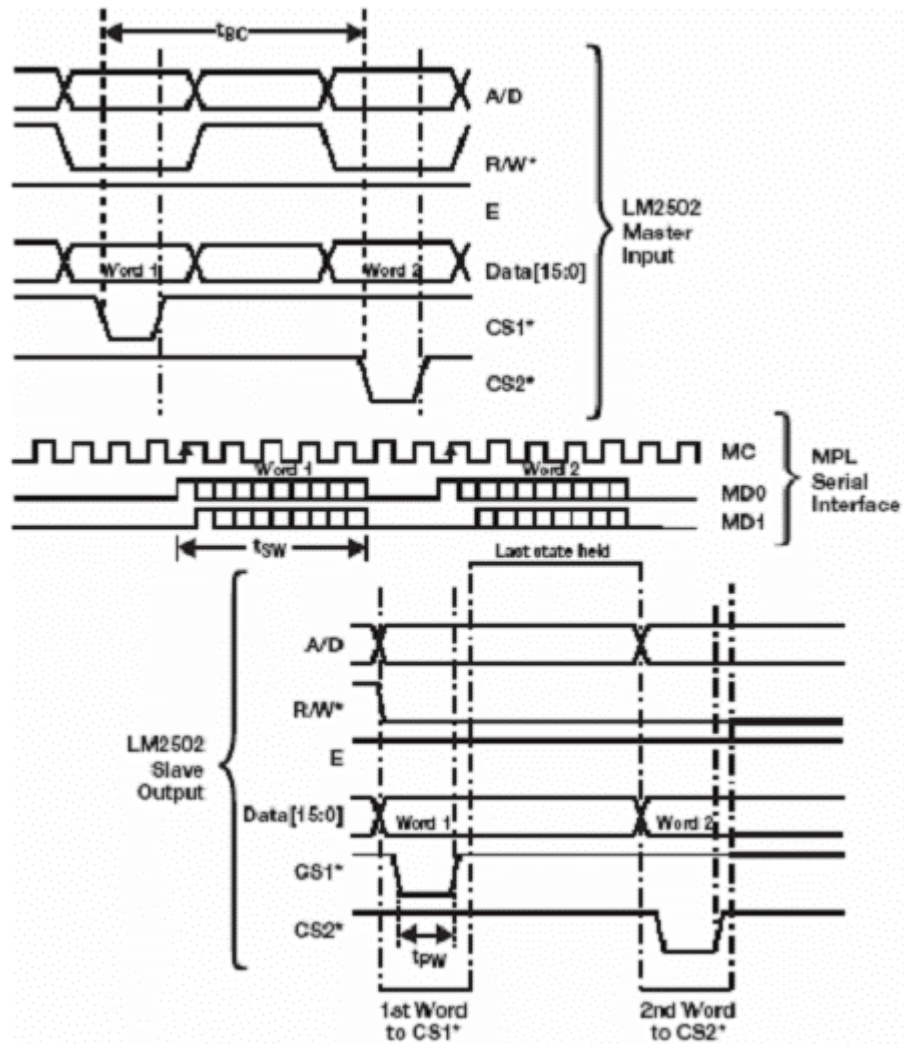


Figure 3: The dual write timing diagram illustrates the serialization and re-parallelization.

When a word and its control signals are sent to the display, the master serializes the information and sends it out in serial form as shown in figure 3. Between transmissions the MPL clock remains on, however the data lines are held at a static level. The serial transmission includes a start bit for bit synchronization, the command information (read or write, address or data, chip select one or two) and the data. The DES receives the serialized word and recreates the parallel bus formatted information for the displays. There are three important timing parameters to be aware of at the system level. The first is the length of the serial word. This depends upon the MPL device configuration, Master CLK input frequency, and also the PLL multiplier. The CLK rate and the multiplier will determine the MC (MPL Clock) rate, and in the 16-bit CPU mode, it takes 6 MC cycles to send a word. Thus, if the clock is 5MHz, and a 6X multiplier, the MC rate is 30MHz. The t_{sw} parameter is $6 \times 1/30\text{MHz}$, which is 200ns. This, we will see, is important to compare to the Master input bus cycle rate. TBC is how fast the host sends words (bus cycle) to the displays. You don't want to load the Master faster than it can send them out in order not to drop any information. In this example, the host should load the Master at 5MT/s or slower. The last important parameter is on the Slave output to the display. The correct information is driven to the display, but the actual timing is slightly modified by the serial transmission. The active pulse width (see Slave output CS

signal in figure 3) is 3 MC cycles wide regardless of the CS pulse width that was on the Master input. Thus, in our example, t_{pw} is 100ns. This pulse width needs to be checked against the display input requirements to make sure the display can support it. Some displays may require a longer pulse width. If this is the case, a lower multiplier can be used, or a slower clock rate applied. The timing diagram shows two writes to the displays, first to CS1 and then to CS2.

MPL employs a unique single-ended current mode interface; the large swing LVCMOS signals are translated to very small current levels. The two logic states are I_{data} and $5I_{data}$. On the LM2502, I_{data} is $150\mu A$. The driver is basically a 2 state current sink. The resulting voltage swing on the line is very small at $<50mV$ (36 times smaller than a 1.8V swing). Not only does this save power in charging up and down the interconnect capacitance, but it also generate little noise. With the higher speed serial signals it is important to keep RFI down to not impact the radio's sensitivity. The receiver provides line termination and converts the current signal back to a logic swing that is adjustable by the Slave's VDDIO magnitude. Figure 4 shows a block diagram for the MC (MPL Clock) line.

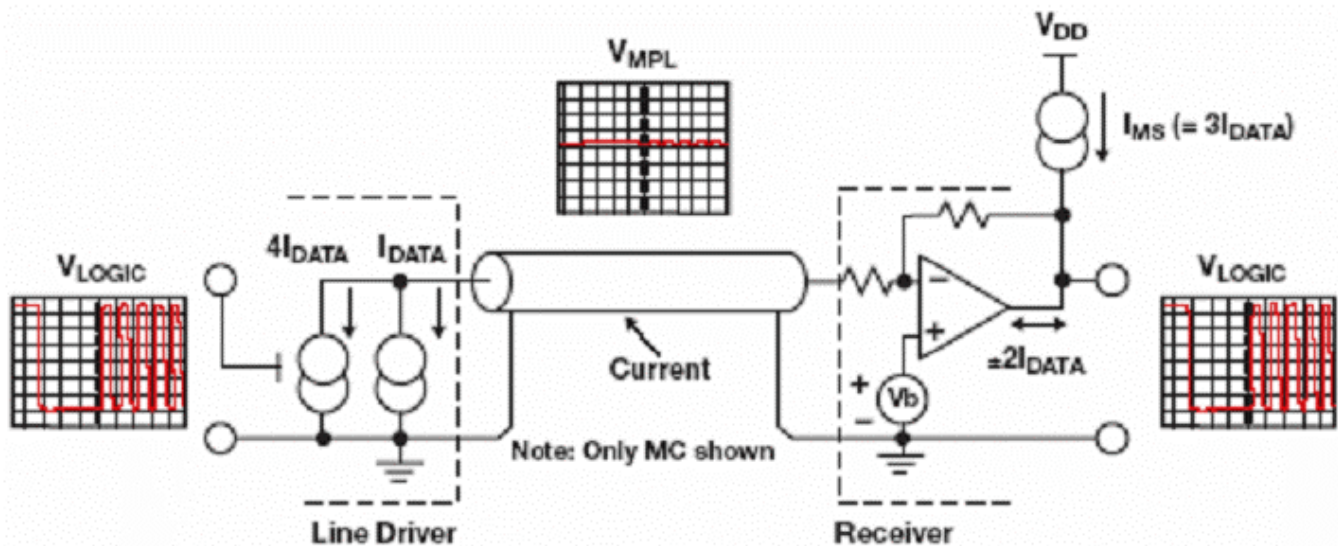


Figure 4: The MPL PHY block diagram highlights how power is saved and EMI is minimized.

Due to the small swing and small current transitions, MPL generates extremely low EMI. Figure 5 shows two plots of EMI from a single layer flex interconnect using a near-field array probe table. An 80MHz clock signal is driven across the flex line (Ground " Signal " Ground pinout) and the scan shows the detected noise. The strongest signal is in the 2nd harmonic range and quickly rolls off for MPL. It is especially important to be low noise in the radio frequency band. Back ground noise tends to be in the $10dB\mu V$ range, thus MPL generates little noise. Next a 3V LVCMOS signal (also with a G-S-G pinout) was measured. The resulting frequency spectrum showed greater magnitude spikes and harmonics to greater than 1.8GHz. No electrical signaling is EMI free (including differential schemes due to signal imbalance and in-pair skew), but starting with the lowest noise signal makes the shielding job much easier.

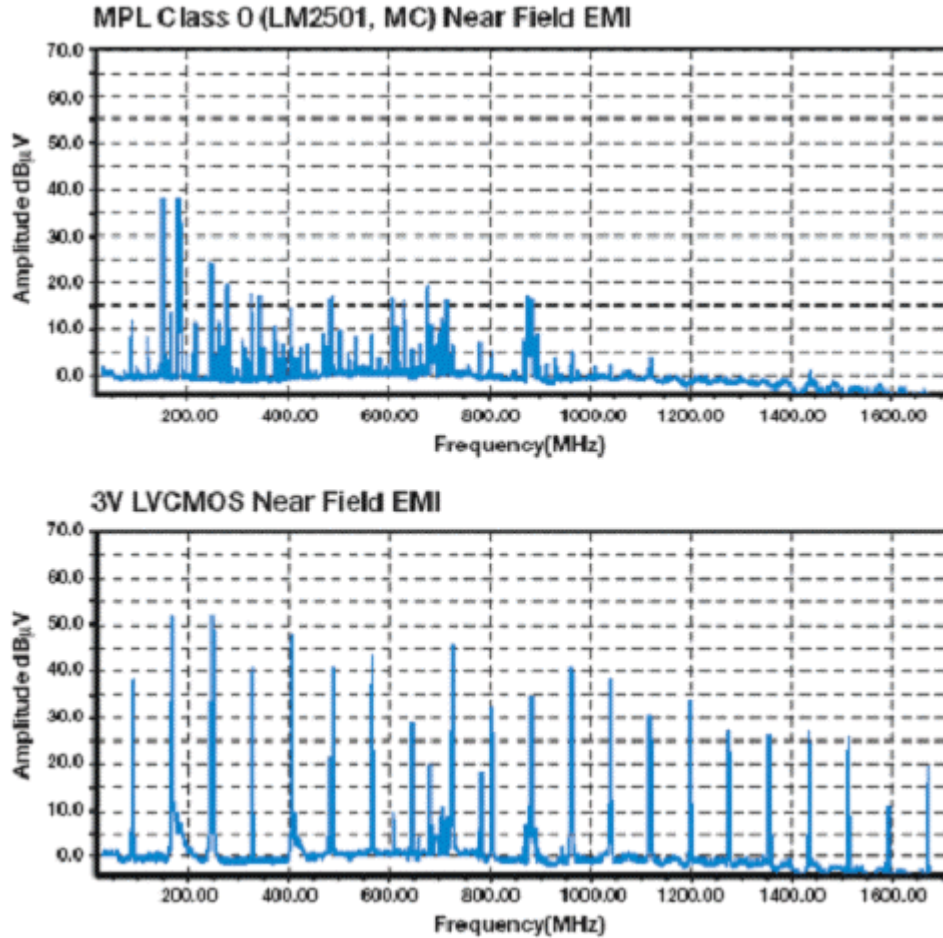


Figure 5: LVC MOS (3V) vs. MPL Class 0 (<50mV) near field EMI plots from a single layer flex interconnect.

What sets MPL Level-0 apart from other interfaces is its focus and optimization for portable video applications. Its notable physical layer features are: few wires, low power, low EMI, robust, level / bus translation, simple transmission scheme, and a video focused bi-directional point-to-point link. By saving space (and costs) MPL enables higher resolution displays into today's form factors for portable applications.